

**Phase-out/Discontinued**

**SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

**DESCRIPTION**

The 2SK2275 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

**FEATURES**

- Low On-state Resistance  
 $R_{DS(on)} = 2.8 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2.0 \text{ A)}$
- LOW  $C_{iss}$   $C_{iss} = 1\ 000 \text{ pF TYP.}$
- High Avalanche Capability Ratings

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)**

Drain to Source Voltage	V <sub>DSS</sub>	900	V
Gate to Source Voltage	V <sub>GSS</sub>	±30	V
Drain Current (DC)	I <sub>D (DC)</sub>	±3.5	A
Drain Current (pulse)	I <sub>D (pulse)*</sub>	±14	A
Total Power Dissipation (T <sub>c</sub> = 25 °C)	P <sub>T1</sub>	35	W
Total Power Dissipation (T <sub>a</sub> = 25 °C)	P <sub>T2</sub>	2.0	W
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Channel Temperature	T <sub>ch</sub>	150	°C
Single Avalanche Current	I <sub>AS**</sub>	3.5	A
Single Avalanche Energy	E <sub>AS**</sub>	22	mJ

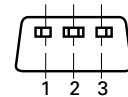
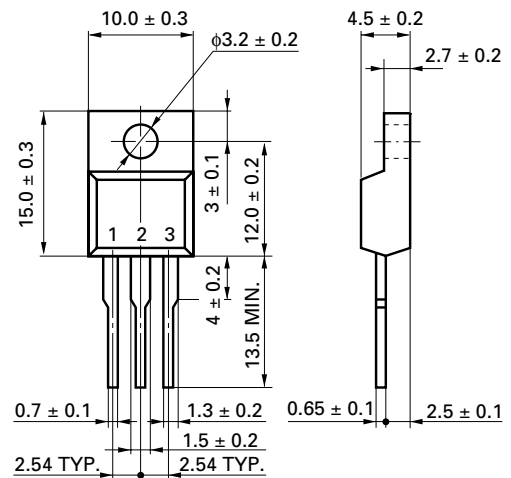
\*PW ≤ 10 μs, Duty Cycle ≤ 1%

\*\*Starting T<sub>ch</sub> = 25 °C, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 V → 0

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

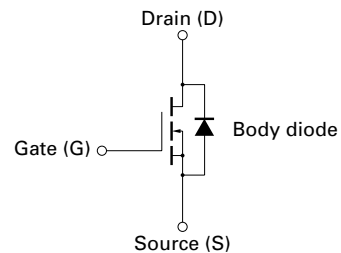
**PACKAGE DIMENSIONS**

(in millimeters)



- 1. Gate
- 2. Drain
- 3. Source

**MP-45F (ISOLATED TO-220)**

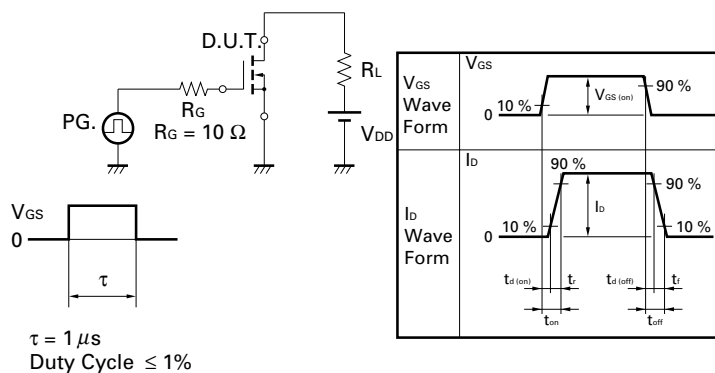
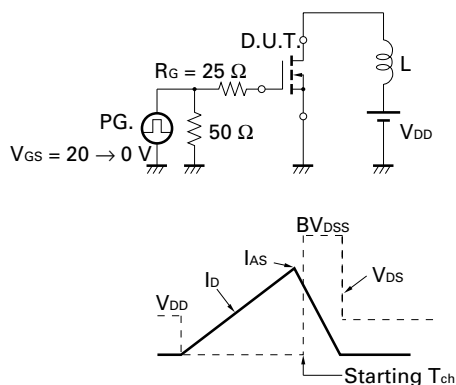


**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

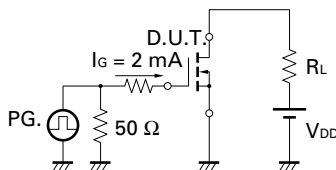
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		2.2	2.8	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	1.0			S	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 2 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 900 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 000		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		170		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		60		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		20		ns	V <sub>GS</sub> = 10 V
Rise Time	t <sub>r</sub>		20		ns	V <sub>DD</sub> = 150 V
Turn-Off Delay Time	t <sub>d(off)</sub>		90		ns	I <sub>D</sub> = 2 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		20		ns	R <sub>L</sub> = 75 Ω
Total Gate Charge	Q <sub>G</sub>		42		nC	V <sub>GS</sub> = 10 V
Gate to Source Charge	Q <sub>GS</sub>		6.0		nC	I <sub>D</sub> = 3.5 A
Gate to Drain Charge	Q <sub>GD</sub>		20		nC	V <sub>DD</sub> = 450 V
Diode Forward Voltage	V <sub>F(S-D)</sub>		0.9		V	I <sub>F</sub> = 3.5 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		480		ns	I <sub>F</sub> = 3.5 A
Reverse Recovery Charge	Q <sub>rr</sub>		2.5		μC	di/dt = 50 A/μs

**Test Circuit 1: Avalanche Capability**

**Test Circuit 2: Switching Time**



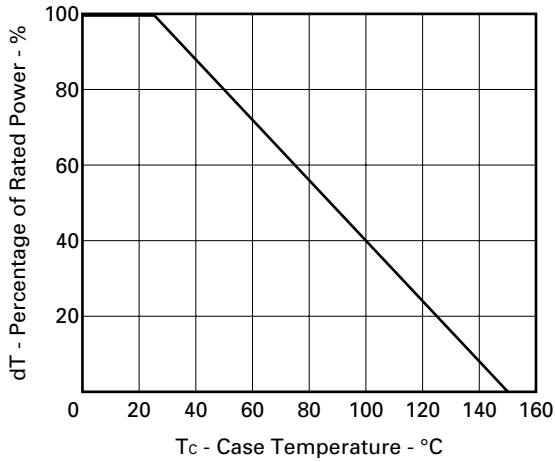
**Test Circuit 3: Gate Charge**



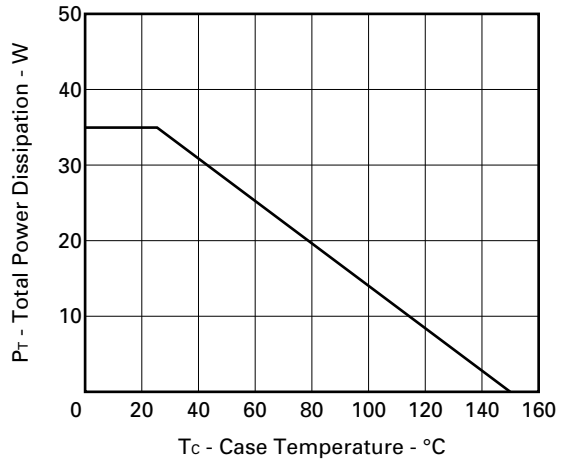
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)

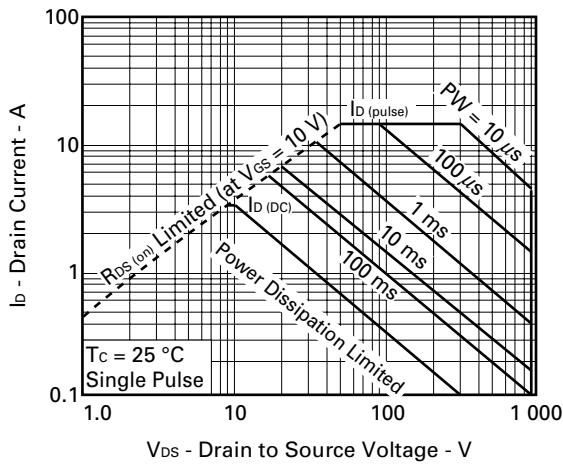
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



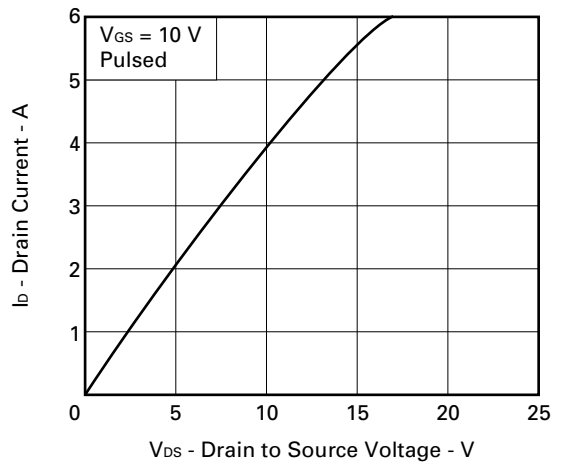
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



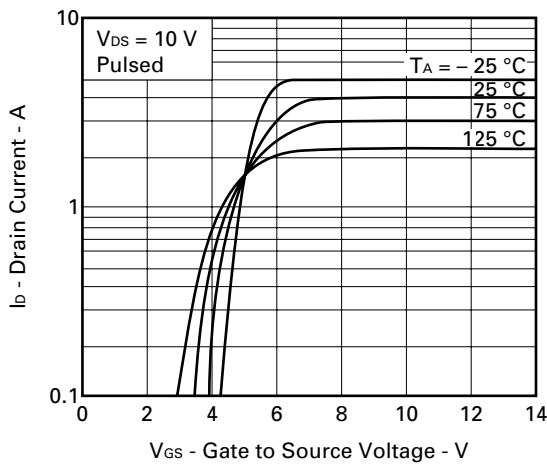
FORWARD BIAS SAFE OPERATING AREA



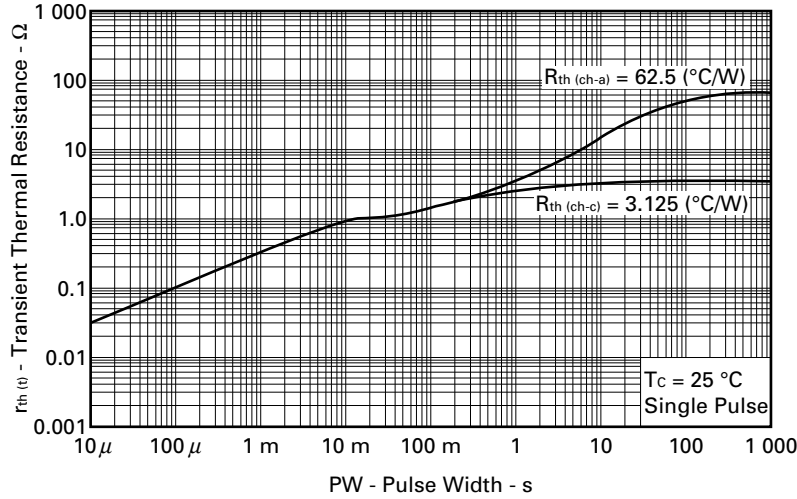
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



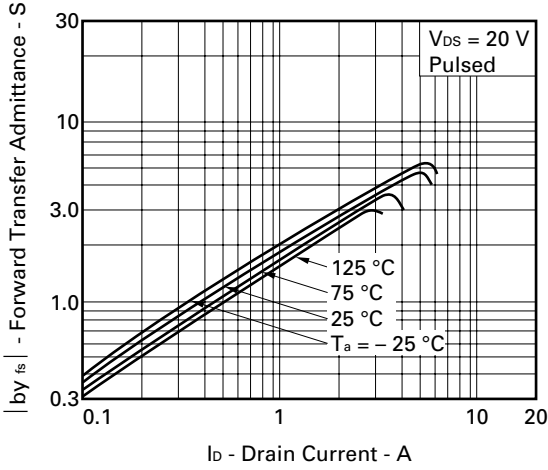
TRANSFER CHARACTERISTICS



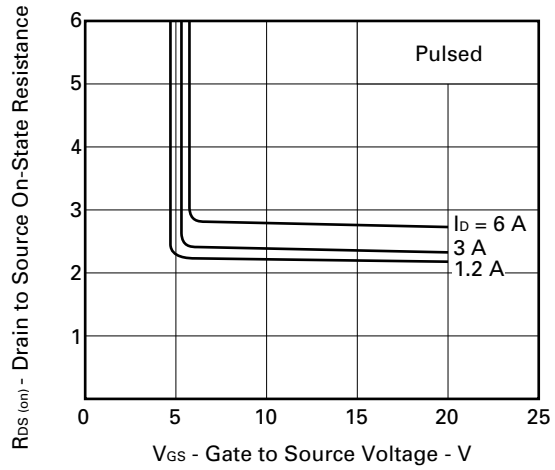
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



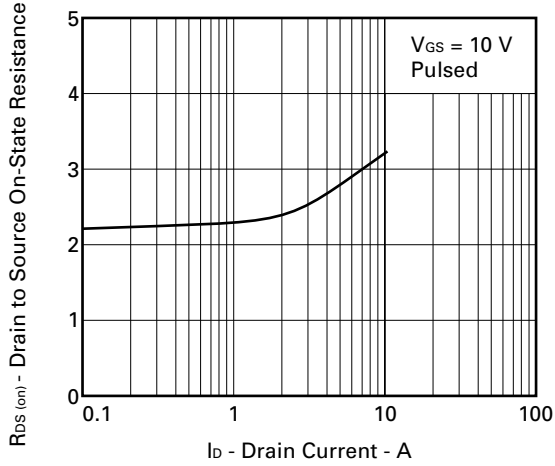
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



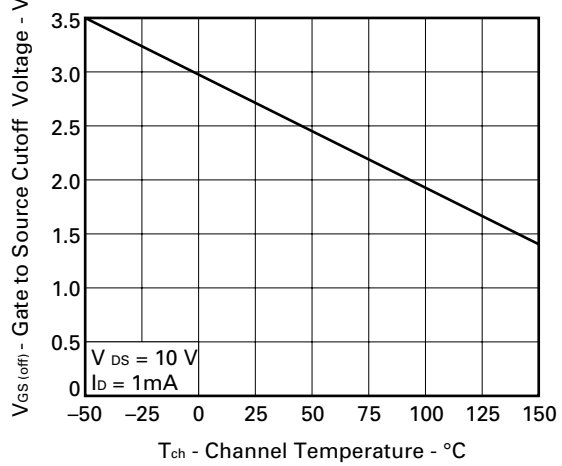
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

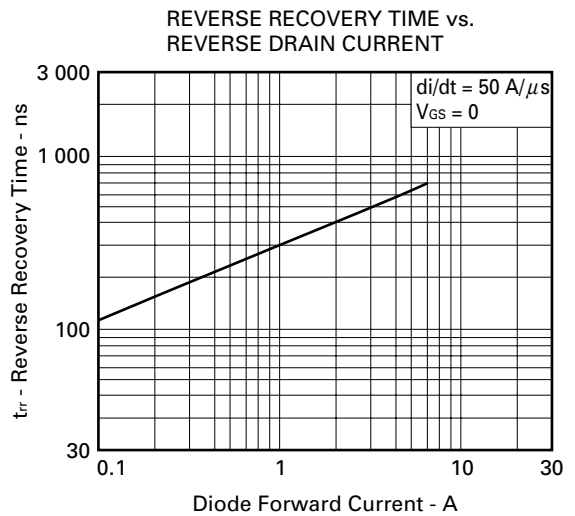
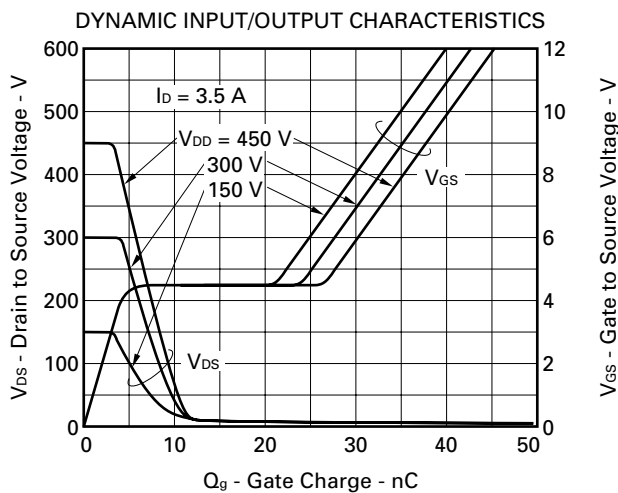
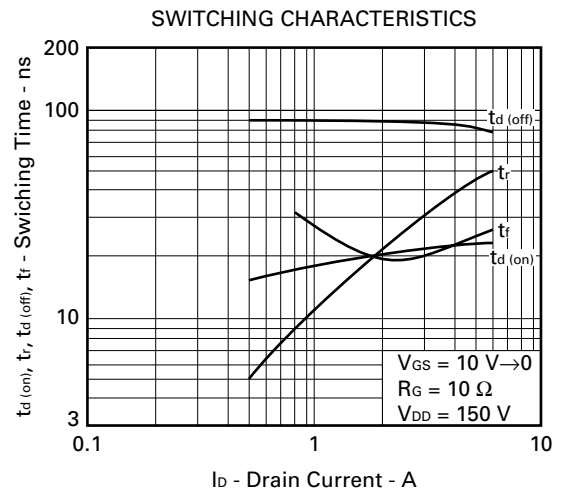
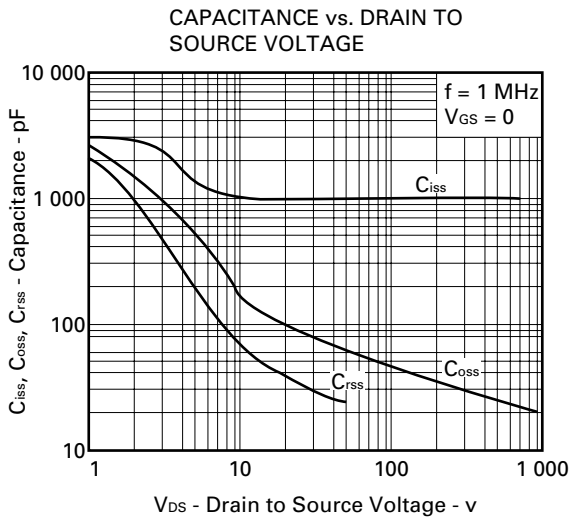
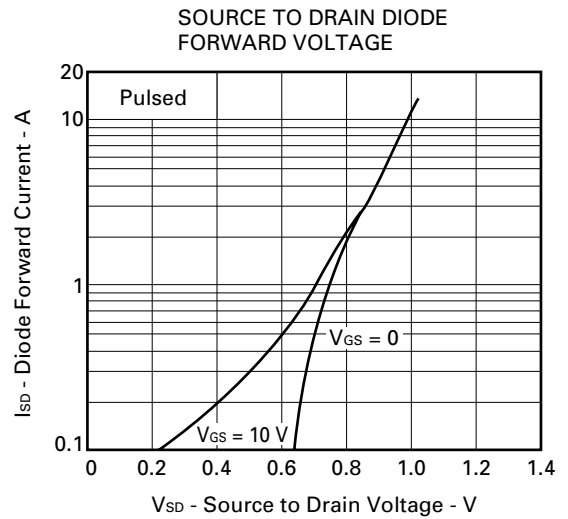
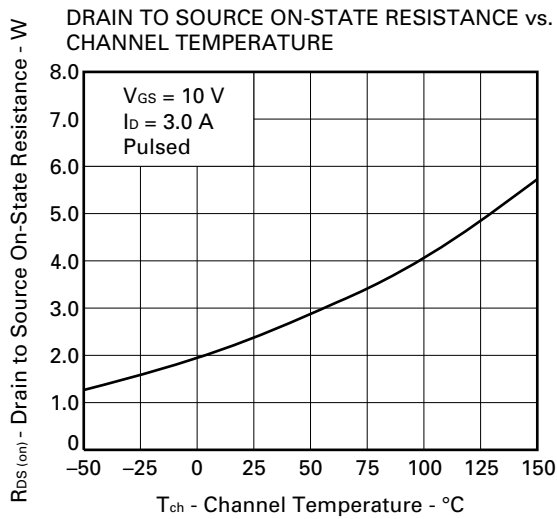


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

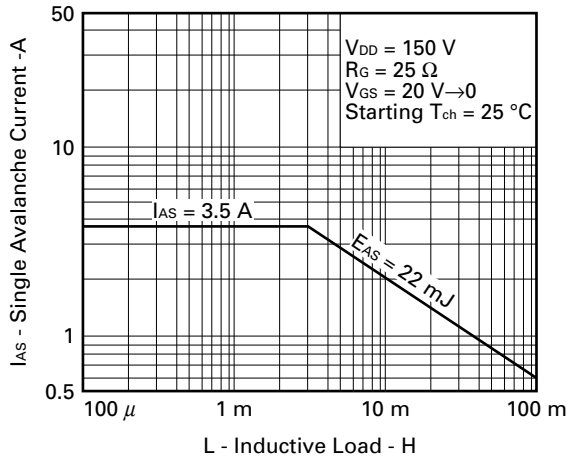


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

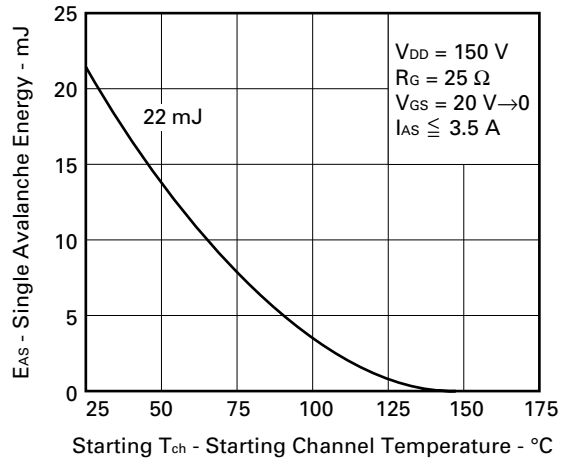




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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