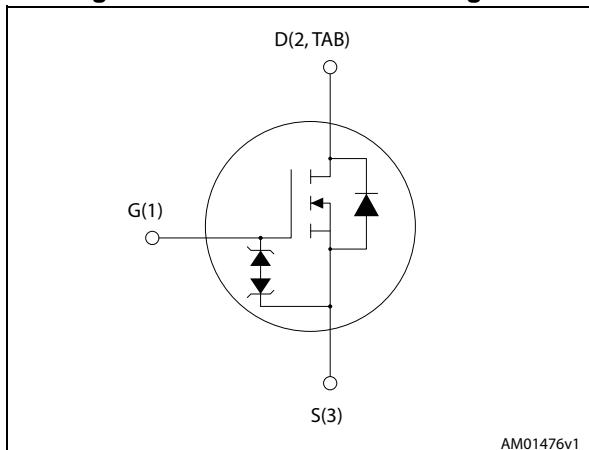


**Figure 1. Internal schematic diagram**



## Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)max</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STB6N80K5	800 V	1.6 Ω	4.5 A	110 W
STD6N80K5				
STI6N80K5				
STP6N80K5				

- TO-220 worldwide best R<sub>DS(on)</sub>
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These devices are N-channel Zener-protected Power MOSFETs realized in SuperMESH™5, a revolutionary avalanche-rugged very high voltage Power MOSFET technology based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

**Table 1. Device summary**

Order code	Marking	Package	Packaging
STB6N80K5	6N80K5	D <sup>2</sup> PAK	Tape and reel
STD6N80K5		DPAK	
STI6N80K5		I <sup>2</sup> PAK	Tube
STP6N80K5		TO-220	

## Contents

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4	<b>Package mechanical data</b>	7
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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	30	V
$I_D$	Drain current (continuous) at $T_C=25\text{ }^\circ\text{C}$	4.5	A
$I_D$	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	2.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	18	A
$P_{TOT}$	Total dissipation at $T_C=25\text{ }^\circ\text{C}$	110	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax}$ )	1.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	150	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 4.5\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ , peak  $V_{DS} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		D <sup>2</sup> PAK	DPAK	I <sup>2</sup> PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	1.14				$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-amb			62.50	62.50	
$R_{thj-pcb}$	Thermal resistance junction-pcb minimum footprint	30	50			

## 2 Electrical characteristics

( $T_{CASE} = 25^\circ\text{C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1 \text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 800 \text{ V}$ $V_{DS} = 800 \text{ V}$ $T_j = 125^\circ\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100 \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 2 \text{ A}$		1.3	1.6	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$	-	255	-	pF
$C_{oss}$	Output capacitance		-	20	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.8	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0$	-	TBD	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	TBD	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz}$ , $I_D = 0$	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640 \text{ V}$ , $I_D = 4.5 \text{ A}$ $V_{GS} = 10 \text{ V}$	-	7.5	-	nC
$Q_{gs}$	Gate-source charge		-	TBD	-	nC
$Q_{gd}$	Gate-drain charge		-	TBD	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=400\text{ V}$ , $I_D=2\text{ A}$ , $R_G=4.7\text{ }\Omega$ , $V_{GS}=10\text{ V}$	-	TBD	-	ns
$t_r$	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
$t_f$	Fall time		-	TBD	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		18	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=4.5\text{ A}$ , $V_{GS}=0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=4.5\text{ A}$ , $V_{DD}=60\text{ V}$ $di/dt =100\text{ A}/\mu\text{s}$ ,	-	445		ns
$Q_{rr}$	Reverse recovery charge		-	8.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	37		A
$t_{rr}$	Reverse recovery time	$I_{SD}=4.5\text{ A}$ , $V_{DD}=60\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$ , $T_j=150\text{ }^\circ\text{C}$	-	580		ns
$Q_{rr}$	Reverse recovery charge		-	10		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	35		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

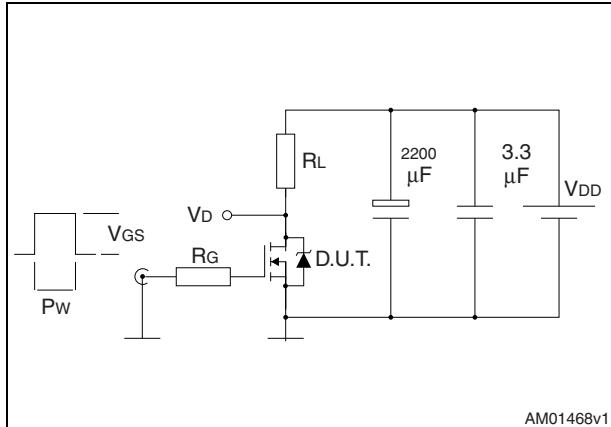
**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{ mA}$ , $I_D=0$	30	-	-	V

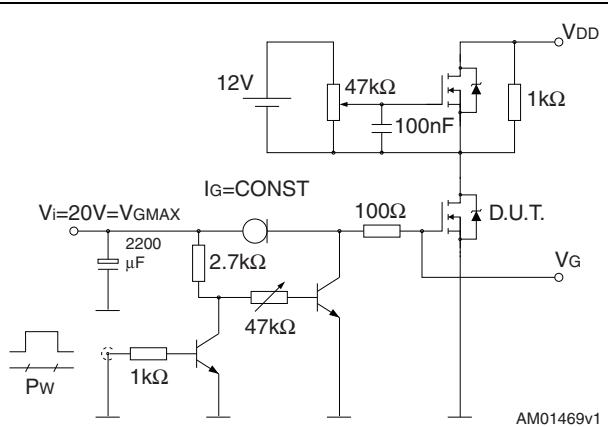
The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

### 3 Test circuits

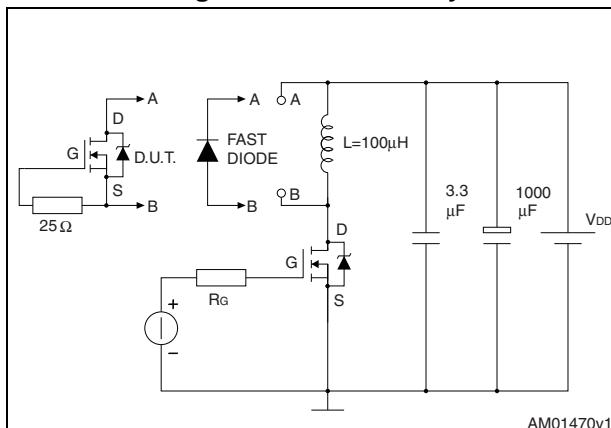
**Figure 2. Switching times test circuit for resistive load**



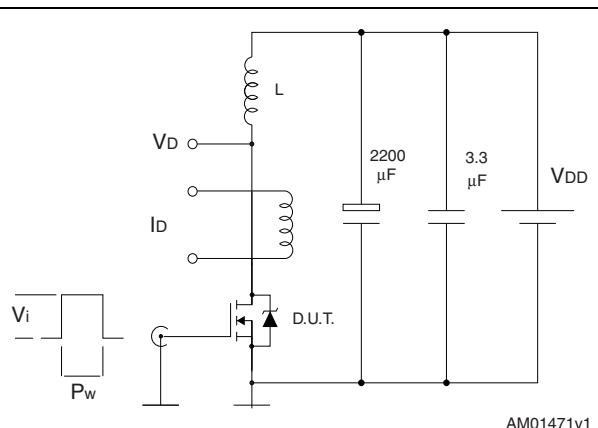
**Figure 3. Gate charge test circuit**



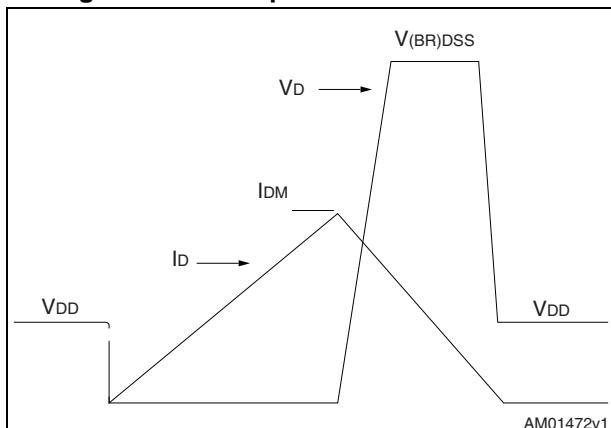
**Figure 4. Test circuit for inductive load switching and diode recovery times**



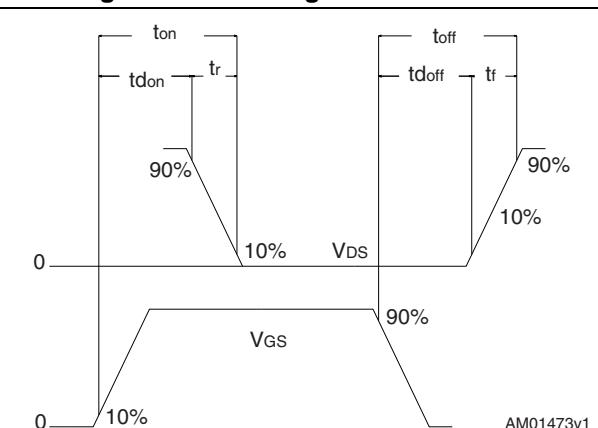
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**

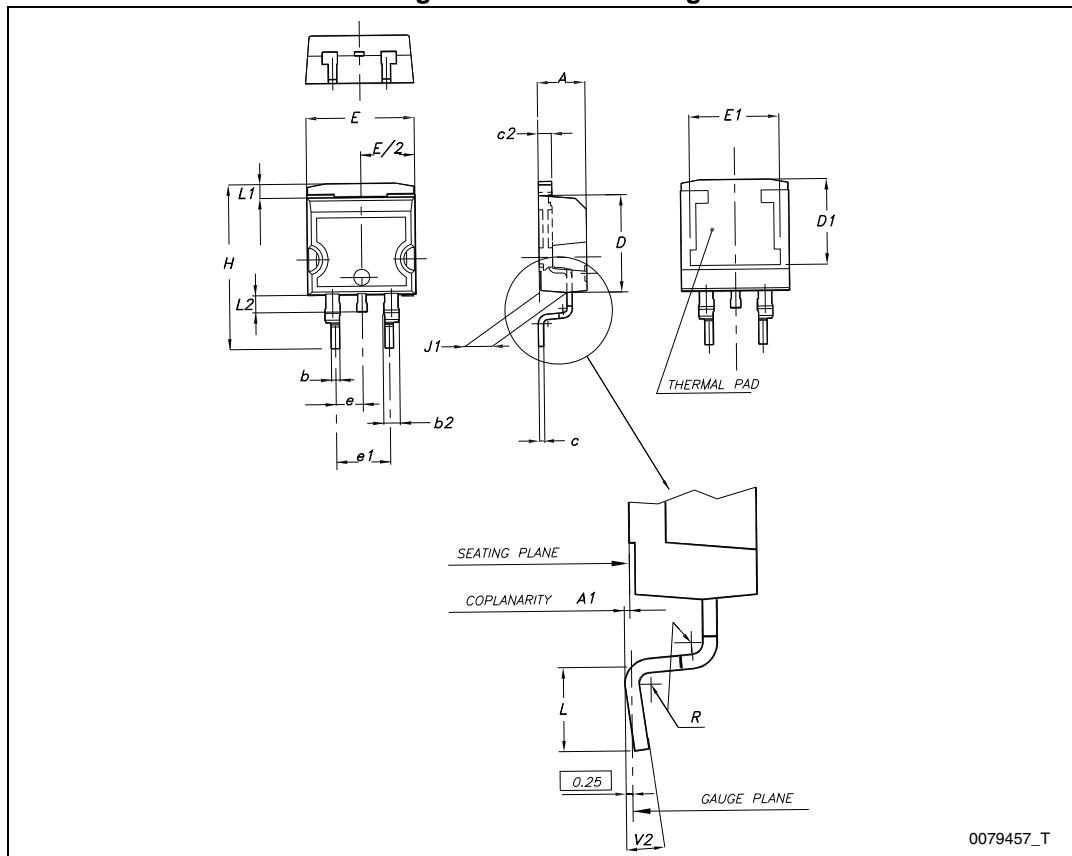
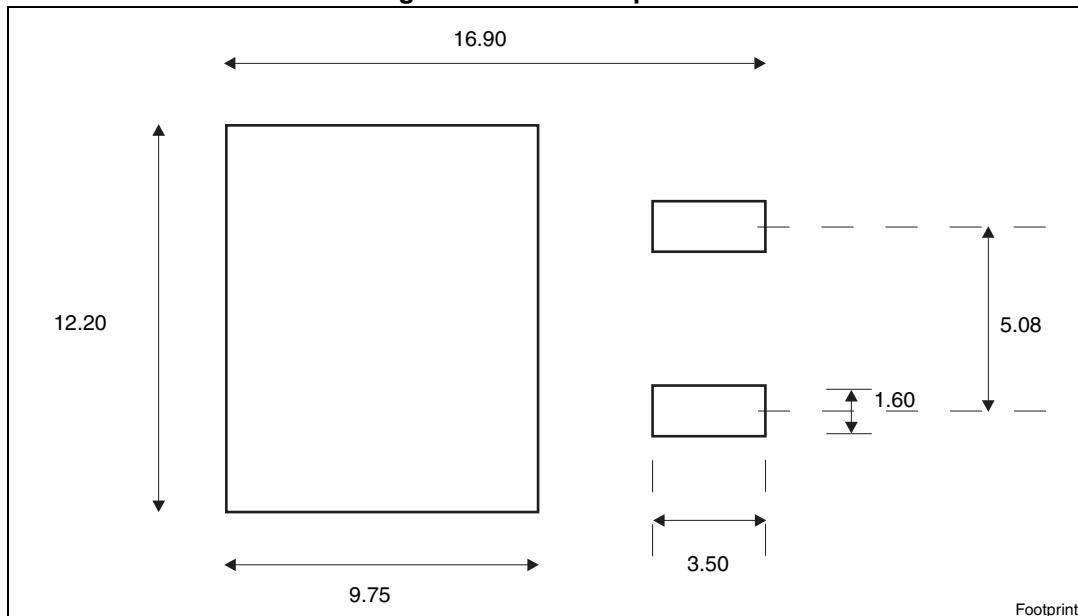


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
ECOPACK® is an ST trademark.

**Table 9. D<sup>2</sup>PAK mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

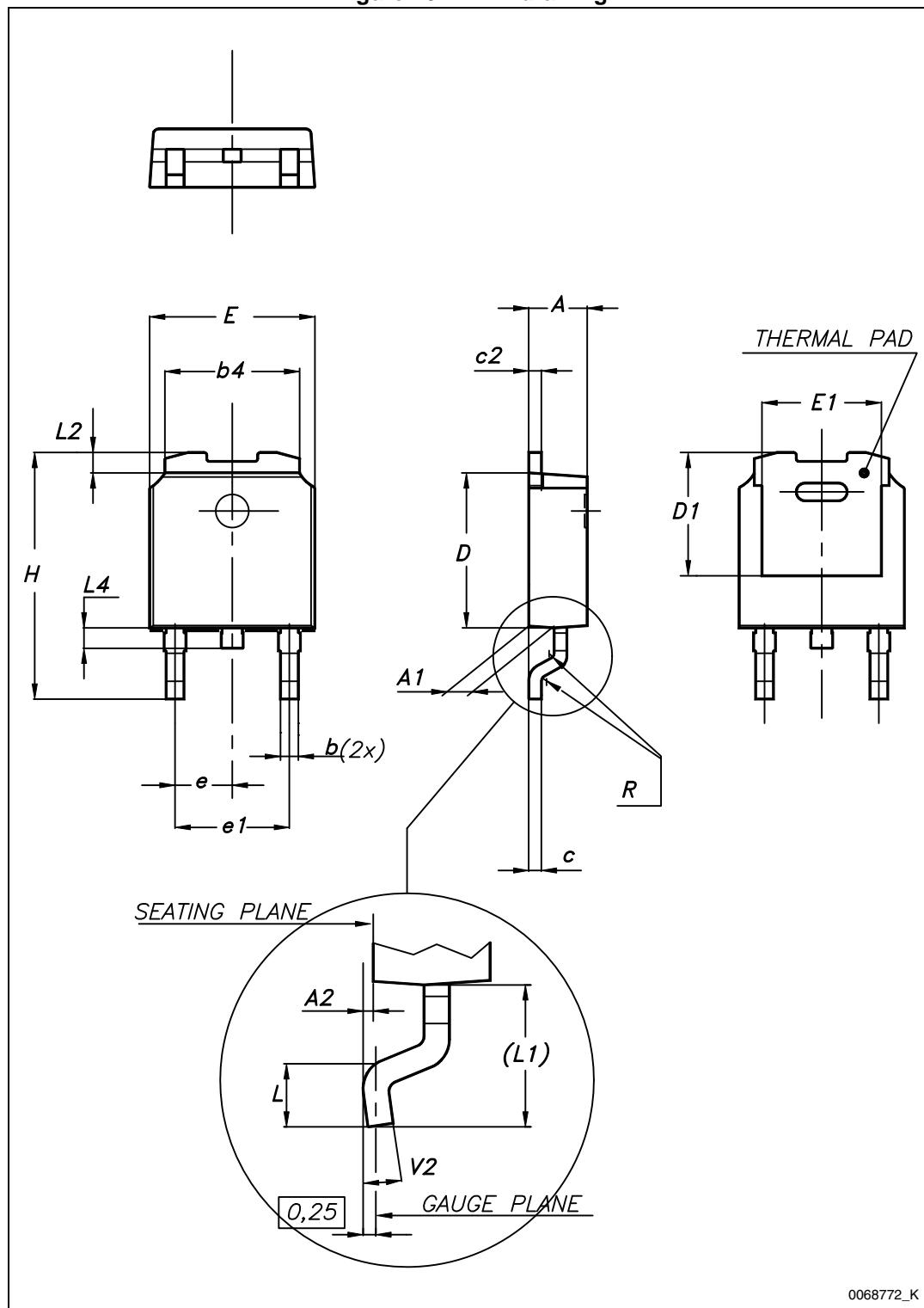
**Figure 8. D<sup>2</sup>PAK drawing****Figure 9. D<sup>2</sup>PAK footprint<sup>(a)</sup>**

a. All dimension are in millimeters

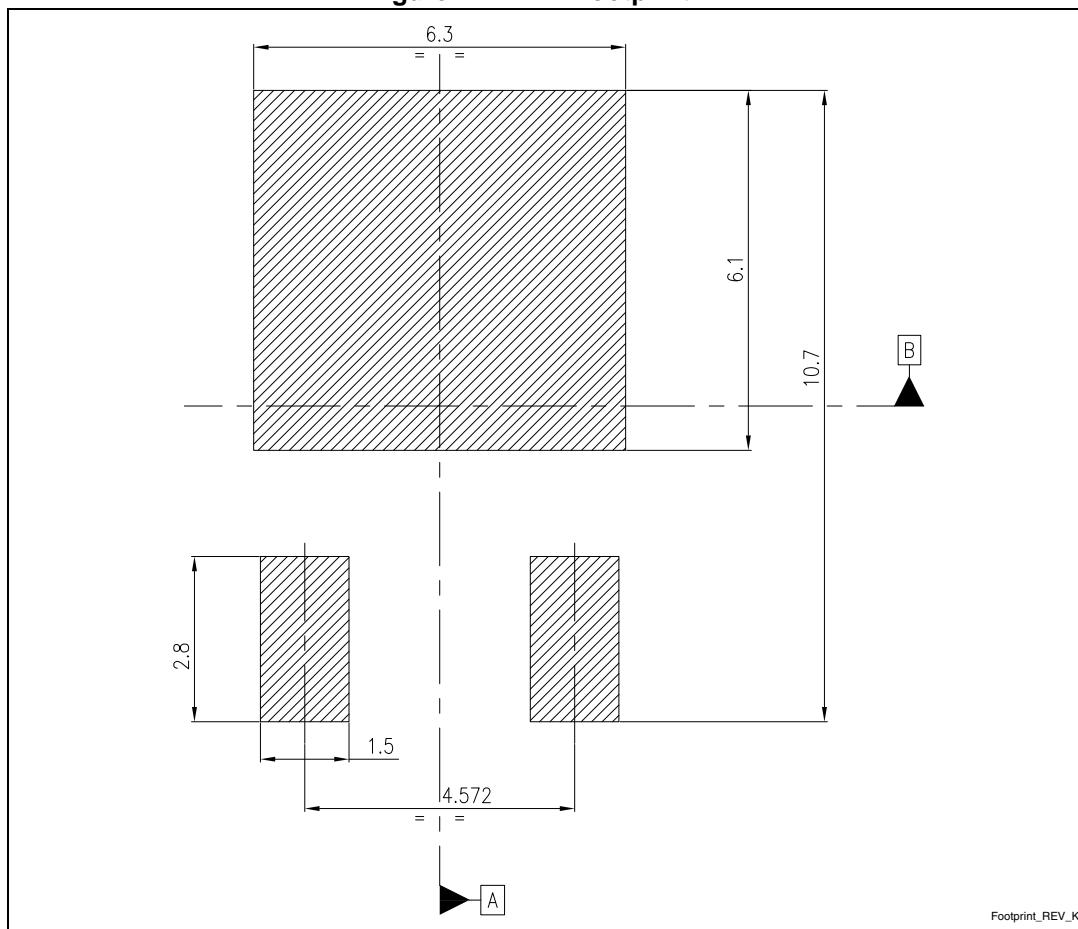
**Table 10. DPAK mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 10. DPAK drawing



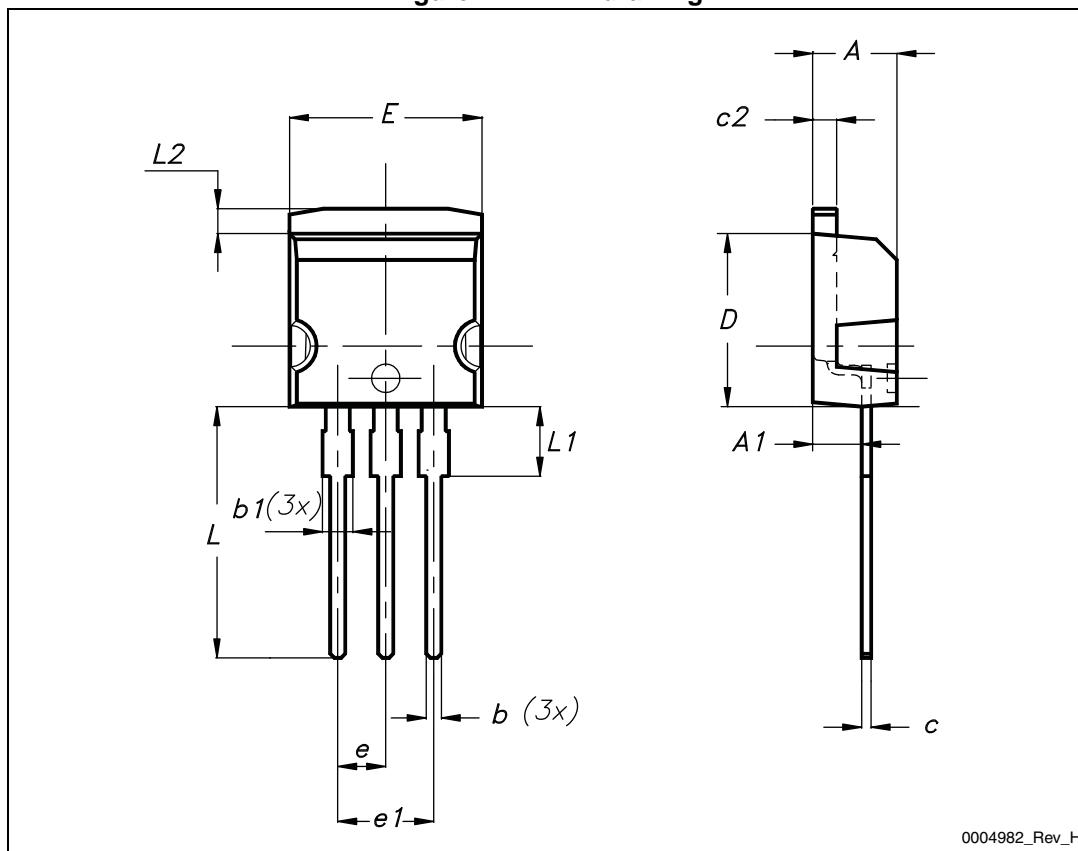
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**Figure 11. DPAK footprint <sup>(b)</sup>**

b. All dimensions are in millimeters

**Table 11. I<sup>2</sup>PAK mechanical data**

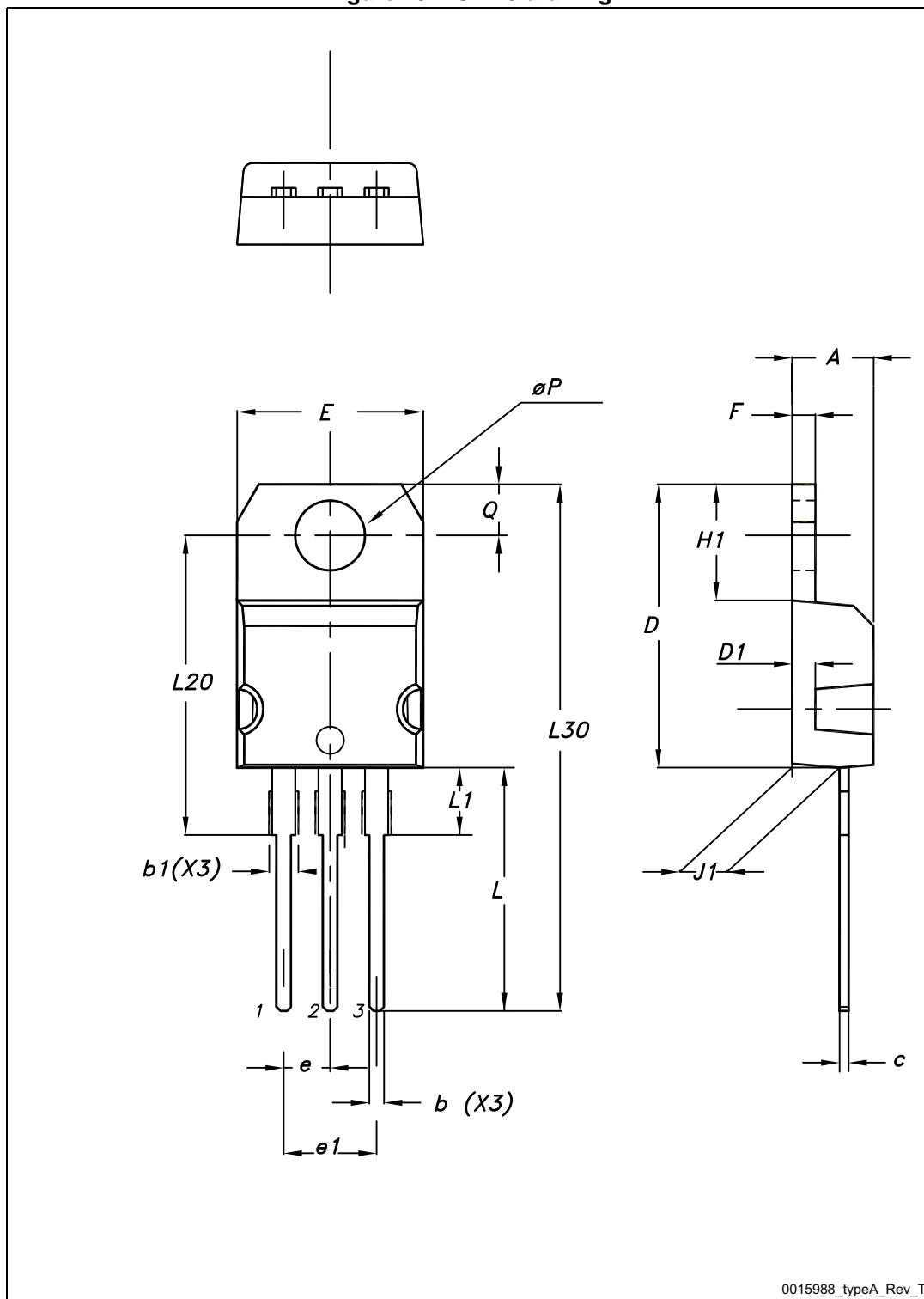
DIM.	mm.		
	min.	typ.	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 12. I<sup>2</sup>PAK drawing

**Table 12. TO-220 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
$\emptyset P$	3.75		3.85
Q	2.65		2.95

Figure 13. TO-220 drawing



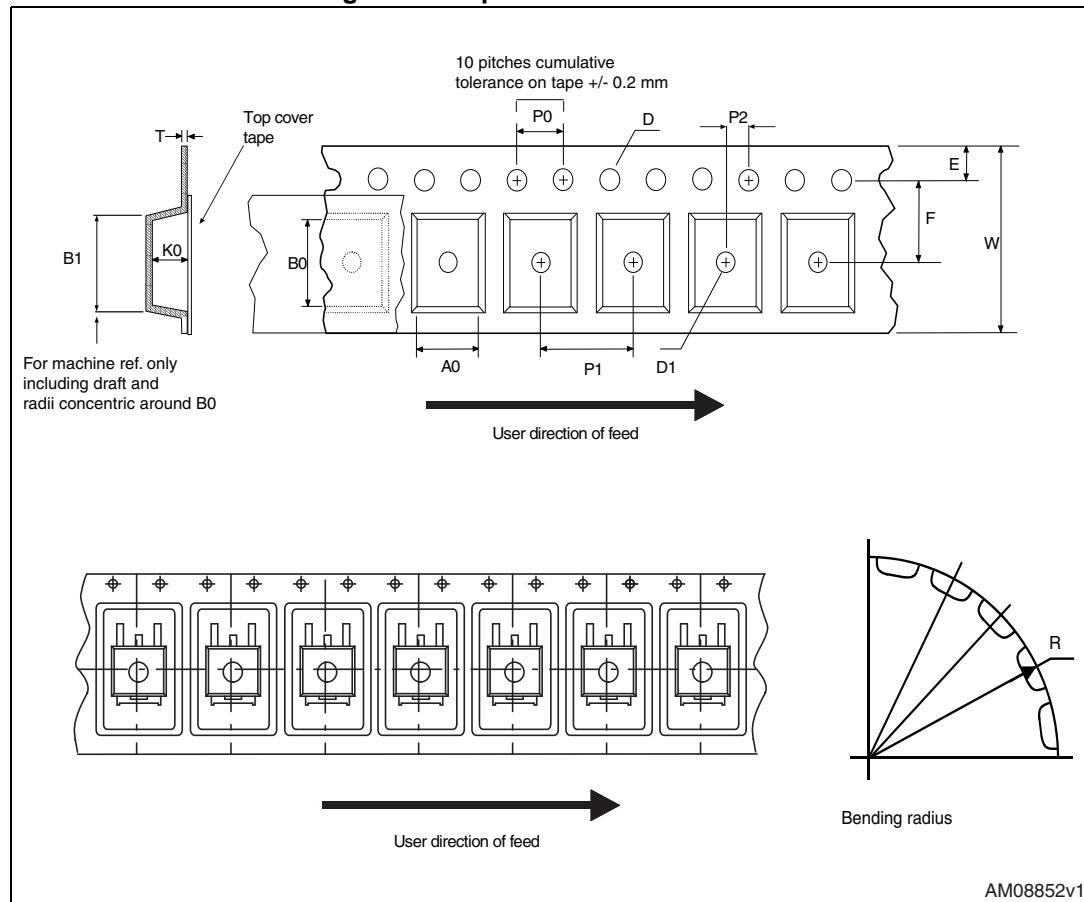
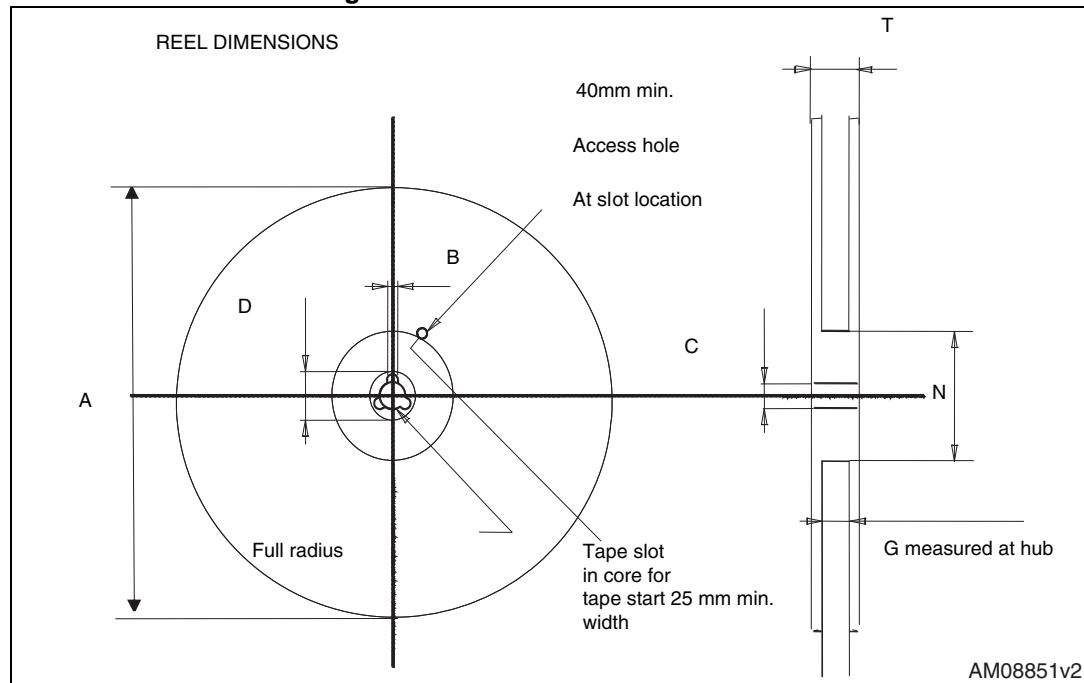
## 5 Packaging information

**Table 13. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

**Table 14. DPAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 14. Tape for D<sup>2</sup>PAK and DPAKFigure 15. Reel for D<sup>2</sup>PAK and DPAK

## 6 Revision history

**Table 15. Document revision history**

Date	Revision	Changes
28-May-2013	1	First release.

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