AN3810K

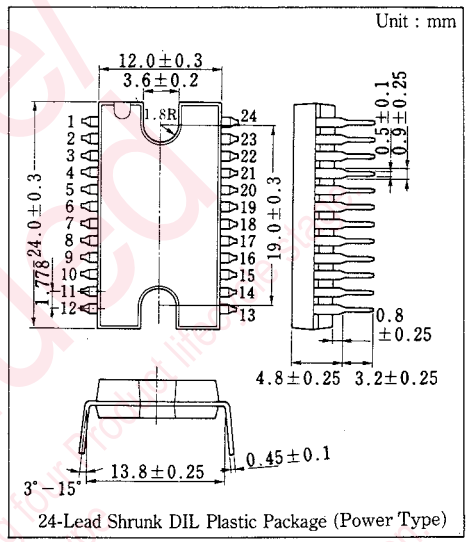
VTR Cylinder Motor Drive Circuit

■ Outline

The AN3810K is an integrated circuit designed for a VCR cylinder direct-drive motor drive circuit.

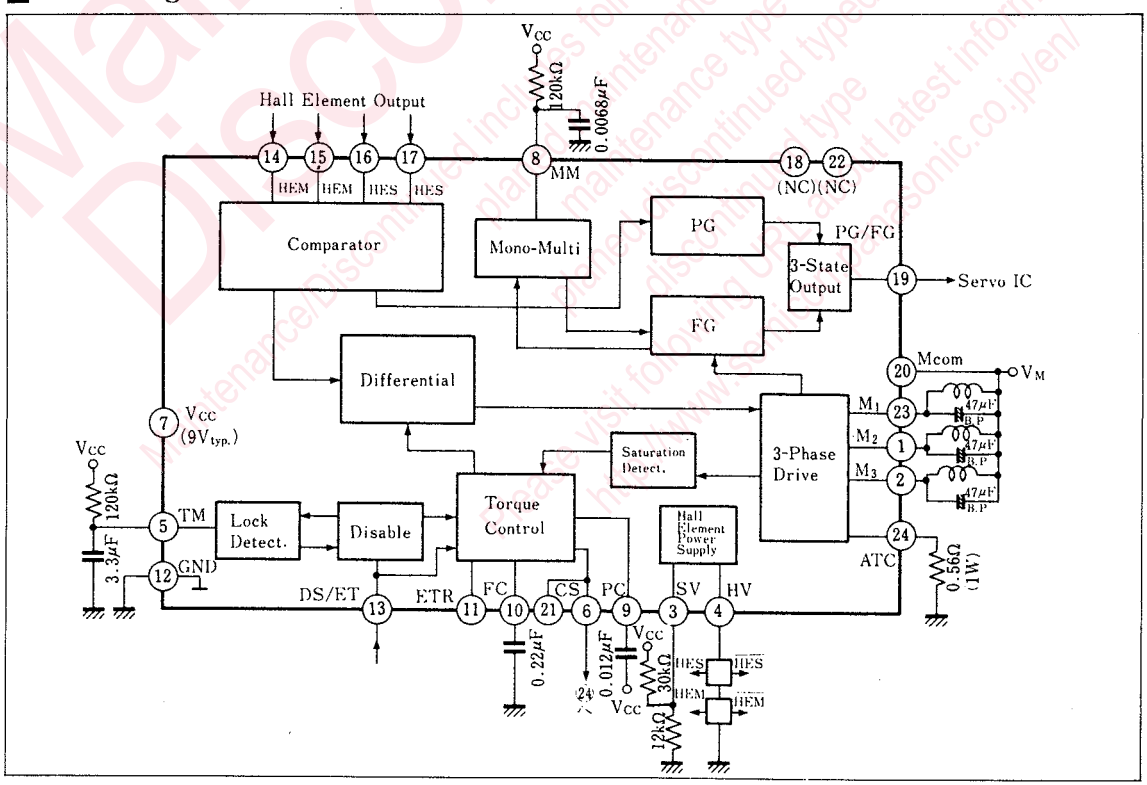
■ Features

- Built-in 3-phase motor drive circuit
- Built-in PG and FG generator circuit
- Built-in motor lock detector circuit
- Built-in hall element circuit



24-Lead Shrunk DIL Plastic Package (Power Type)

■ Block Diagram



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■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Drive Output 2	13	Torque. Control/Disable
2	Drive Output 3	14	H.E. Input
3	H.E. Power Supply Control	15	H.E. Input
4	H.E. Power Supply	16	H.E. Input
5	Mono-Multi Cap.	17	H.E. Input
6	Current Detection	18	NC
7	V_{CC}	19	PG/FG Output
8	Mono-Multi	20	Voltage Supply for Motor
9	Phase Compensation	21	Current Detection
10	Soft Shart	22	NC
11	Reference Voltage Input	23	Drive Output
12	GND	24	ATC

■ Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating		Unit	Note
Supply voltage	V_{CC}	14.4		V	
Circuit Voltage	$V_{n\text{-}12}$	0	40	V	n=1, 2, 23
	$V_{20\text{-}12}$	0	24	V	
Circuit Current	I_n	0	1500	mA	n=1, 2, 23
Power Dissipation	P_D	2000		mW	
Operating Ambient Temperature	T_{opr}	−20~+75		℃	
Storage Temperature	T_{stg}	−55~+150		℃	

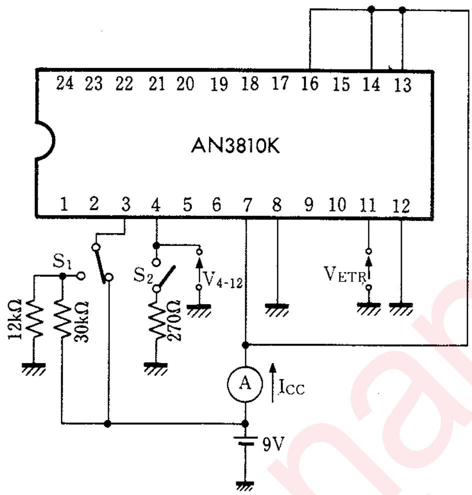
■ Electrical Characteristics (V_{CC}=9V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Total Current	I_{CC}*	1		6		16	mA
Output Saturation Temperature	$V_{O(sat)}$	2	I_O=1A			1	V
ATC Limit Voltage	V_{lim}	2	V_{ET}=0V (in Full Torque Command)	0.41		0.53	V
Input/Output Transfer Gain	A_V	2	R_s=0.47Ω	0.9		1.4	
Saturation Detection Gain	A_d	3		0.5		1.5	
HV Output Voltage	V_{HV}	1	V_{SV}=2.6V, R_{HV}=270Ω	2.2		2.6	V
HV Protection Voltage	V_{prot}	1	V_{SV}=V_{CC}	3.3		4.3	V
DS Input Level Voltage	V_{DS}	2		3.1		4.1	V
ETR Voltage	V_{ETR}	1		2.1		2.9	V
ET Offset Voltage	V_{offET}	2		−30		30	mV
HEM-$\overline{\text{HEM}}$ Comparator Offset Voltage	V_{offM}	4		−6		6	mV
HES-$\overline{\text{HES}}$ Comparator Offset Voltage	V_{offS}	4		−6		6	mV
PG/FG 3-Value Output Voltage(1)	V_{OH}	4	I_{19}=±10μA	4.2			V
PG/FG 3-Value Output Voltage(2)	V_{OM}	4	I_{19}=±10μA	2.1		2.9	V
PG/FG 3-Value Output Voltage(3)	V_{OL}		I_{19}=±10μA			1	V
MM Threshold Voltage	V_{MM}	5		3.8		4.6	V
BFG Fetch Voltage	V_{BFG}	4	V_M=9V	0.5		1.2	V
TM Threshold Voltage	V_{TM}	5		4.1		4.9	V
ATC Residual Voltage	V_{idle}	2		0		5	mV
ET Input Bias Current	I_{ET}					−10	μA
HEM, $\overline{\text{HEM}}$, HES, and $\overline{\text{HES}}$ Input Bias Voltage	I_H					−10	μA

Note) Range of the Operating Supply Voltage : $V_{CC(opr)}$= 8 ~13V

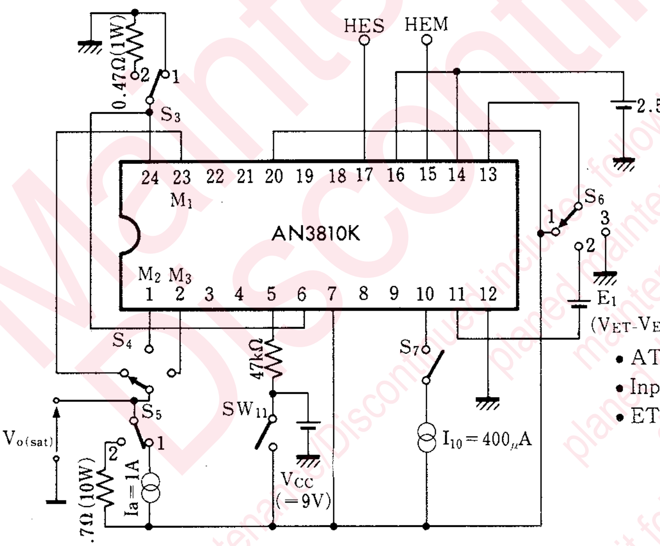
*The Supply Current to the Hall element is not included.

Test Circuit 1 (I_{CC})



- Total current (I_{cc}): S_1—on the ① side, S_2 Open I_{cc} is measured.
- HV output voltage (V_{HV}): S_1—on the ② side, S_2 Short V_{4-12} is measured.
- HV protection voltage (Vprot): S_1—on the ① side, S_2 Open V_{4-12} is measured.
- ETR voltage (V_{ETR}): V_{ETR} is measured.

Test Circuit 2 ($V_{O(set)}$, V_{lim}, A_v, V_{DS}, V_{OFFET}, V_{idle})

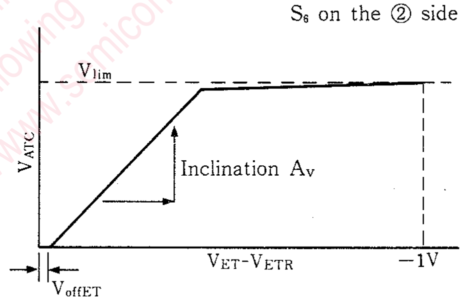


- Output saturation voltage ($V_{o(sat)}$): S3—on the①side, S5—on the①side, S6—on the①side, S7—ON
  Three—phase output modes are set at Pin⑭, Pin⑮, Pin⑯, and Pin⑰ and a measuring terminal is switched to another at S_4.

Measuring Terminal \ Mode Set	HEM (Pin⑮)	HES (Pin⑰)
M1 (Pin㉓)	H	H. L
M2 (Pin①)	L	H
M3 (Pin②)	L	L

H:3V
L:2V

- ATC limiting voltage (V_{lim}): S_3 on the ② side
- Input／Output transfer gain (Av): S_5 on the ② side
- ET offset voltage ($Voff_{ET}$): S_7 open, S_6 on the ② side



- DS input level voltage (V_{DC}): HEM(Pin⑮) "H" one phase(M1)ON STEP1. Vcc SW1L.OFF→ON
  V_{13-12} is measured when V_{5-12} changes from "H" to "L" by increasing V_{13-12} from 0F.
- ATC residual voltage (V_{idec}): S_3 on the 2 side, S_5 on the 2 side, S_7 open, S_6 on the 1 side
  V_{24-12} is measured when V_{ET} is in the disable condition.

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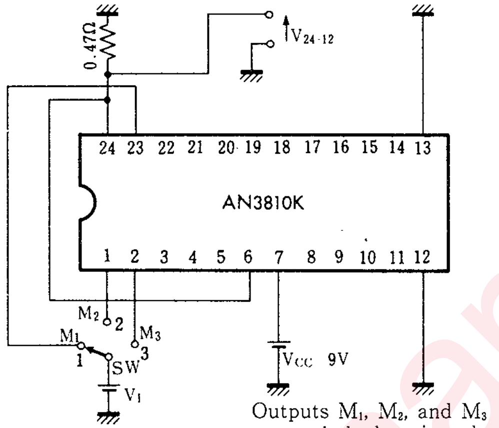
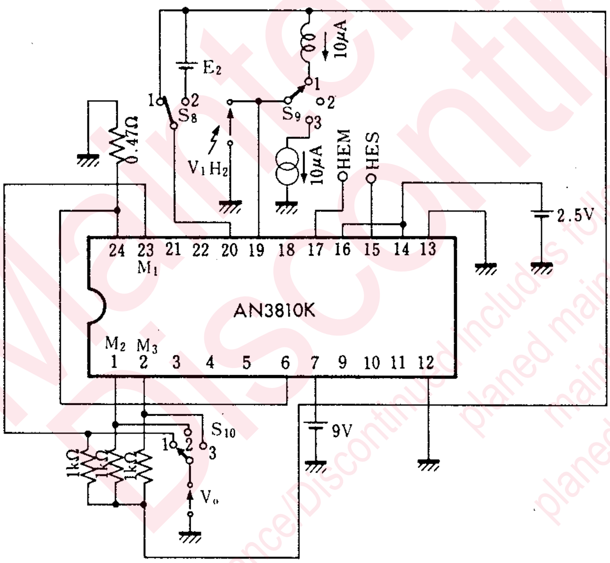
Test Circuit 3 (A_d)



Outputs M_1, M_2, and M_3 are switched on in order

Test Circuit 4 (V_{offM}, V_{offS}, V_{OH}, V_{OM}, V_{OL}, V_{BFG})



- $HEM-\overline{HEM}$
  Comparator offset voltage (V_{offM}): S_8 on the ①side
- $HES-\overline{HES}$
  Comparator offset voltage (V_{offS}): S_8 on the ①side HEM:L (2V)

Confirmed that Vo factuares as the HES and HEM terminal voltage vary by±5mV

V_{offM}	HEM	H(2.5V+5mV)	←→	L(2.5V−5mV)
	S_{10}-on the 1 side (M1)	L	←→	H
V_{offS}	HES	H(2.5V+5mV)	←→	L(2.5V−5mV)
	S_{10}-on the 2 side (M2)	L	←→	H

● V_{OH}, V_{OM}, V_{OL}

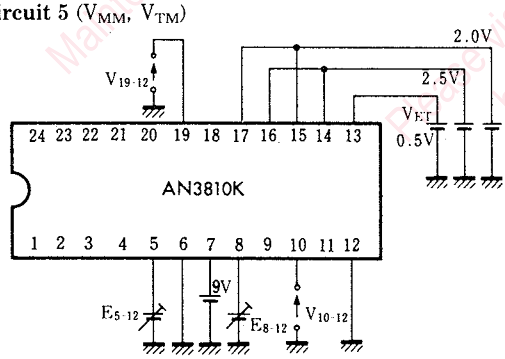
PG/FG 3 Value Output Voltage(1)			HES	HEM	MM
V_{OH}	(1)	S_8-on the 1 side	H→L	H	H
V_{OM}	(2)		L	L	H
V_{OL}	(3)		L	L	L

V_{19-12} where S_9 is on the 1, 2, or 3 side
HES, HEM H:3V, L:2V
MM H:5.2V L:3.2V

● V_{BFG}

		HES	HEM	MM
BFG Fetch Voltage V_{BFG}	S_8-on the 2 side	L	L	L→H

Test Circuit 5 (V_{MM}, V_{TM})



Measure E_2 when it is increased from 0V and V_{19-12} is changed from L to M. Test Circuit 5.

- MM threshold voltage (V_{MM}): Measure E_{8-12} when V_{19-12} changes from L to H by increasing E_{8-12} from 0V gradually.
- TM threshold voltage (V_{TM}): Measure E_{8-12} when V_{10-12} changes from H to L by increasing E_{5-12} from 0V gradually.

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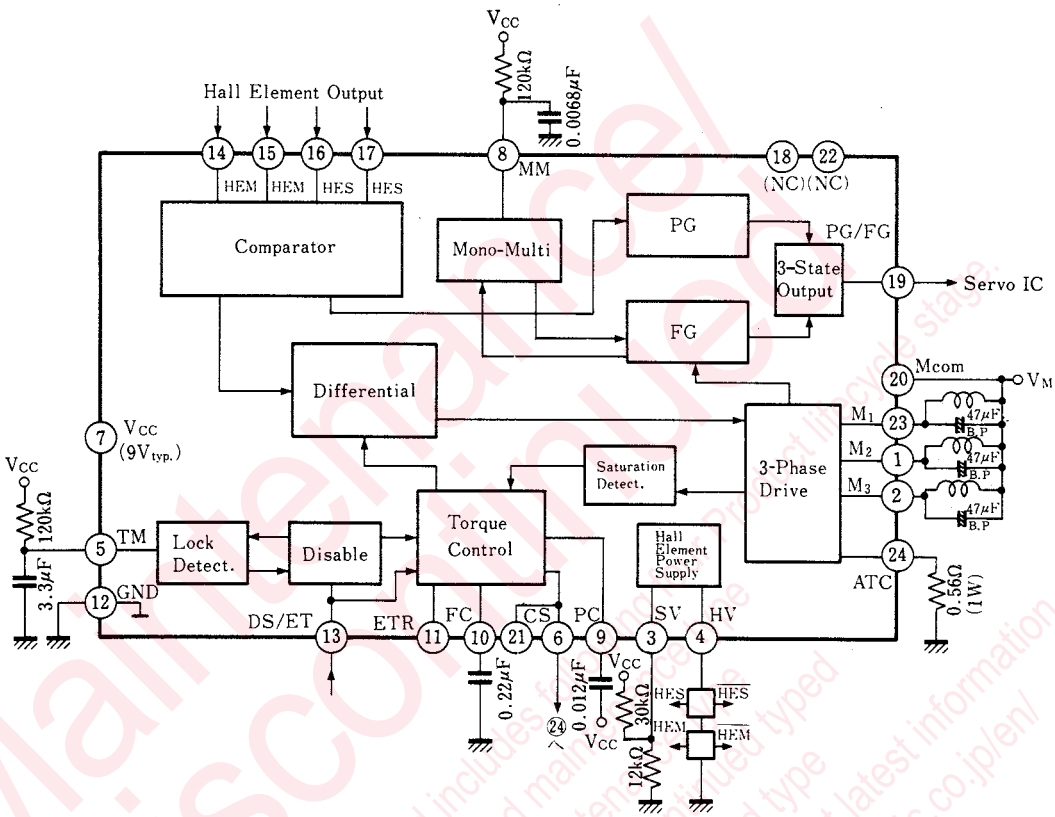
■ Application Circuit



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