

# DATA SHEET

Part No.	AN5891K
Package Code No.	SDIP024-P-0300B

Maintenance/Discontinued includes following product lifecycle stage.  
planned maintenance type  
maintenance type  
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# AN5891K

## TV and audio sound processor

### ■ Features

- Sound Processor using I<sup>2</sup>C bus
- This IC has Mute, AGC, super bass, tone, volume balance control, and 3-D surround.

### ■ Applications

- TV, Audio

### ■ Package

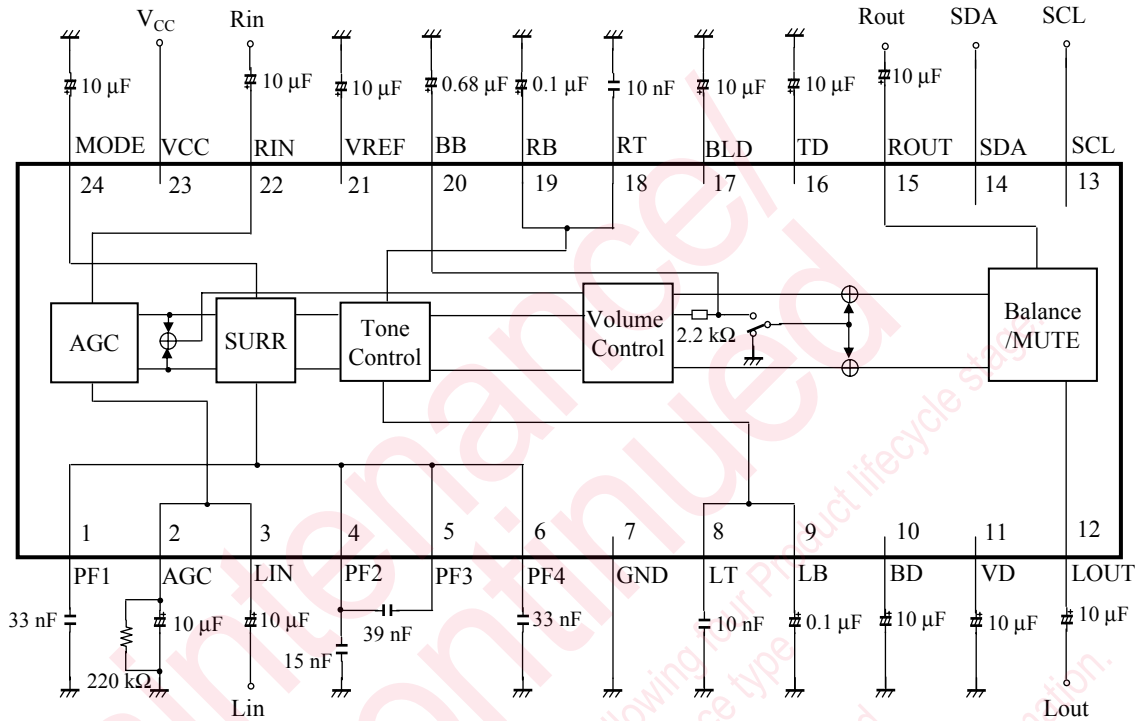
- 24 pin Plastic Shrink Dual Inline Package (SDIP Type)

### ■ Type

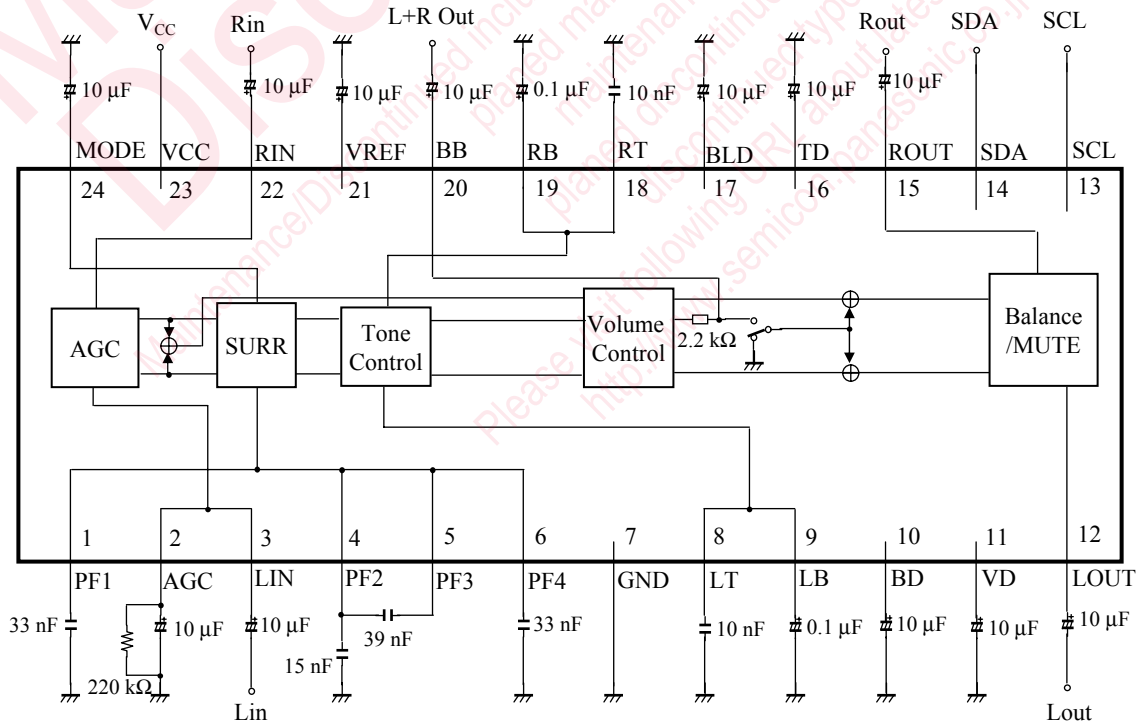
- Silicon monolithic bipolar IC

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Application Circuit Example

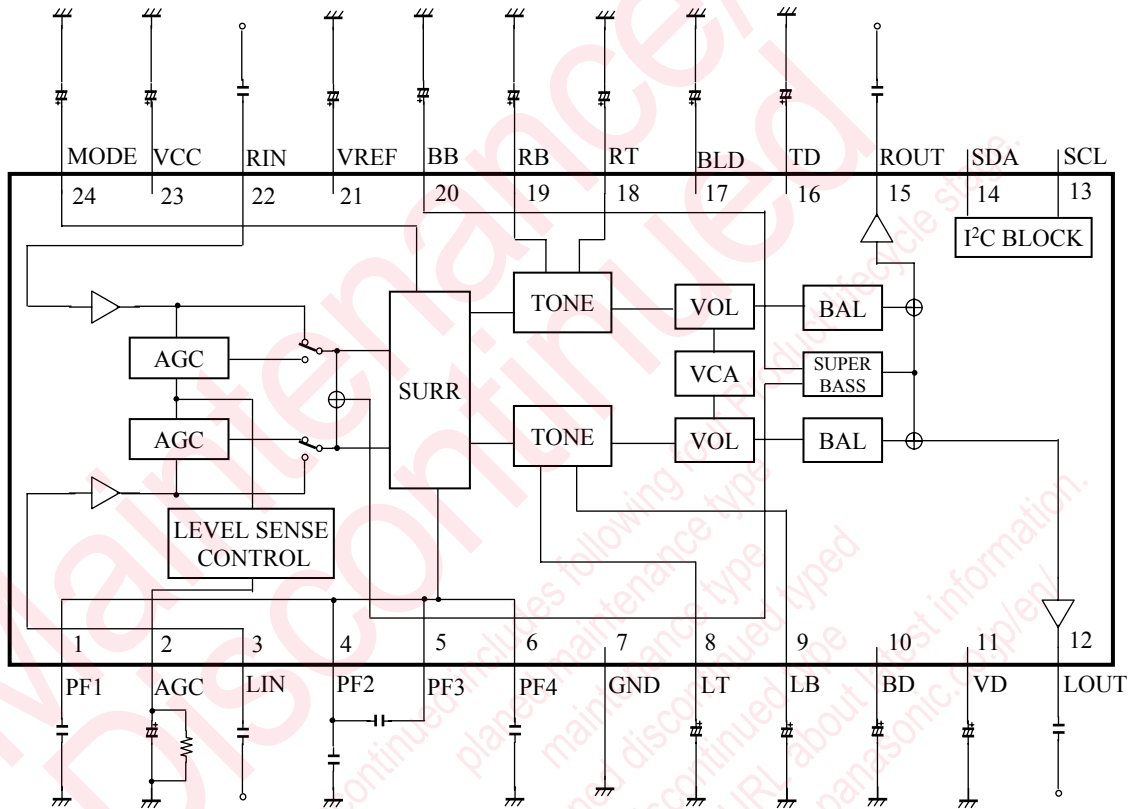


Application circuit to get L+R output instead of Super Bass Boost



Note) This application circuit is shown as an example but does not guarantee the design for mass production set.

■ Block Diagram



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

### ■ Pin Descriptions

Pin No.	Pin name	Description
1	PF1	Phase filter 1
2	AGC	AGC level sensor
3	LIN	L-ch. input
4	PF2	Phase filter 2
5	PF3	Phase filter 3
6	PF4	Phase filter 4
7	GND	Ground
8	LT	L-ch. treble Fc adjustment
9	LB	L-ch. bass Fc adjustment
10	BD	BASS DAC output
11	VD	Volume DAC output
12	LOUT	L-ch. output
13	SCL	SCL
14	SDA	SDA
15	ROUT	R-ch. output
16	TD	Treble DAC output
17	BLD	Balance DAC output
18	RT	R-ch. treble Fc adjustment
19	RB	R-ch. bass Fc adjustment
20	BB	Bass mixer gain adjustment
21	VREF	$1/2V_{CC}$
22	RIN	R-ch. input
23	VCC	Power supply pin ( $V_{CC}$ )
24	MODE	Mode control

### ■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which are not destructed, and are not the values to which operation is guaranteed.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage	$V_{CC}$	11.0	V	*1
2	Supply current	$I_{CC}$	50	mA	—
3	Power dissipation	$P_D$	550	mW	—
4	Operating ambient temperature	$T_{opr}$	-25 to +75	°C	*2
5	Storage temperature	$T_{stg}$	-55 to +150	°C	*2

Notes) \*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

\*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

### ■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range	$V_{CC}$	6.0 to 10.0	V	*

Note) \* : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

### ■ Electrical Characteristics at $V_{CC} = 9.0 \text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Notes
				Min	Typ	Max		
1	Quiescent Current	$I_{CC T}$	No input	—	45	60	mA	—
2	Volume (Max Level)	$V_{Vmax}$	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	-1	0	1	dB	*1
3	Volume (Mid Level)	$V_{Vmid}$	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	-14.5	-12.5	-10.5	dB	*1
4	Volume (Min Level)	$V_{Vmin}$	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	—	-100	-90	dB	*1
5	THD (1 kHz)	$THD_{max}$	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	—	0.1	0.3	%	*1
6	Max input level	$V_{Imax}$	THD = 1% $f = 1 \text{ kHz}$	2.0	2.2	—	V[rms]	*1
7	Output noise at volume min	$V_{Nmin}$	$V_{IN} = 0 \text{ V[rms]}$ $R_g = 4.7 \text{ k}\Omega$	—	3	10	$\mu\text{V}$	*2
8	Output noise at volume max	$V_{Nmax}$	$V_{IN} = 0 \text{ V[rms]}$ $R_g = 4.7 \text{ k}\Omega$	—	65	100	$\mu\text{V}$	*2
9	Mute Level	$V_{MUTE}$	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	—	-100	-90	dB	*1
10	Balance (Max Level)	$V_{Bmax}$	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	-1	0	1	dB	*1
11	Balance (Min Level)	$V_{Bmin}$	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	—	-82	-80	dB	*1
12	Bass (Max Level)	$VB_{Bmax}$	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	10	12.5	15	dB	—
13	Bass (Min Level)	$VB_{Bmin}$	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	-13.5	-11.0	-8.5	dB	—
14	Treble (Max Level)	$VT_{Bmax}$	$V_{IN} = 400 \text{ mV[rms]}$ $f = 20 \text{ kHz}$	10	12.5	15	dB	—
15	Treble (Min Level)	$VT_{Bmin}$	$V_{IN} = 400 \text{ mV[rms]}$ $f = 20 \text{ kHz}$	-13.5	-11.0	-8.5	dB	—
16	Super bass (Max Level)	$VX_{Bmax}$	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	3	5	7	dB	*1
17	Super bass (Min Level)	$VX_{Bmin}$	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	0	2	4	dB	*1

Notes) \*1 : DIN AUDIO filter used.

\*2 : A-weighted noise filter used.



■ Electrical Characteristics (continued) at  $V_{CC} = 9.0\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Notes
				Min	Typ	Max		
18	AGC gain 1	$V_{AGC1}$	$V_{IN} = 50\text{ mV[rms]}$ $f = 1\text{ kHz}$	77	110	150	mV[rms]	*1
19	AGC gain 2	$V_{AGC2}$	$V_{IN} = 1\text{ V[rms]}$ $f = 1\text{ kHz}$	230	345	470	mV[rms]	*1
20	Surround level 1	$V_{SU1}$	$V_{IN} = 50\text{ mV[rms]}$ $f = 50\text{ Hz}$	200	240	280	mV[rms]	*1
21	Surround level 2	$V_{SU2}$	$V_{IN} = 50\text{ mV[rms]}$ $f = 10\text{ kHz}$	130	170	210	mV[rms]	*1
22	Surround noise Level	$V_{SN}$	$V_{IN} = 0\text{ mV}$ $R_g = 4.7\text{ k}\Omega$	—	110	150	$\mu\text{V[rms]}$	*2
23	THD (Surround)	$THD_{SU}$	$V_{IN} = 400\text{ mV[rms]}$ $f = 1\text{ kHz}$	—	0.1	0.3	%	*1
24	Cross talk	CT	$V_{IN} = 1\text{ V[rms]}$ $f = 1\text{ kHz}$	—	-78	-66	dB	*2
25	Channel balance (Max)	$CB_{max}$	$V_{IN} = 1\text{ V[rms]}$ $f = 1\text{ kHz}$	-1	0	1	dB	*1
26	Channel balance (1/4)	$CB_{1/4}$	$V_{IN} = 1\text{ V[rms]}$ $f = 1\text{ kHz}$	-2	0	2	dB	*1

Notes) \*1 : DIN AUDIO filter used.

\*2 : A-weighted noise filter used.

■ Electrical Characteristics (continued) at  $V_{CC} = 9.0\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Notes
				Min	Typ	Max		
I <sup>2</sup> C Interface								
27	Suction current during ACK	$I_{ACK}$	Max. suction current value of Pin 14 at 0.4 V	3.0	10	—	mA	—
28	SCL, SDA signal input High level	$V_{IHI}$	—	3.0	—	5.0	V	—
29	SCL, SDA signal input Low level	$V_{ILO}$	—	0	—	1.5	V	—
30	Max frequency allowable to input	$f_{imax}$	—	—	—	100	kbit/s	—

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### ■ Electrical Characteristics (Reference values for design) at $V_{CC} = 9.0\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

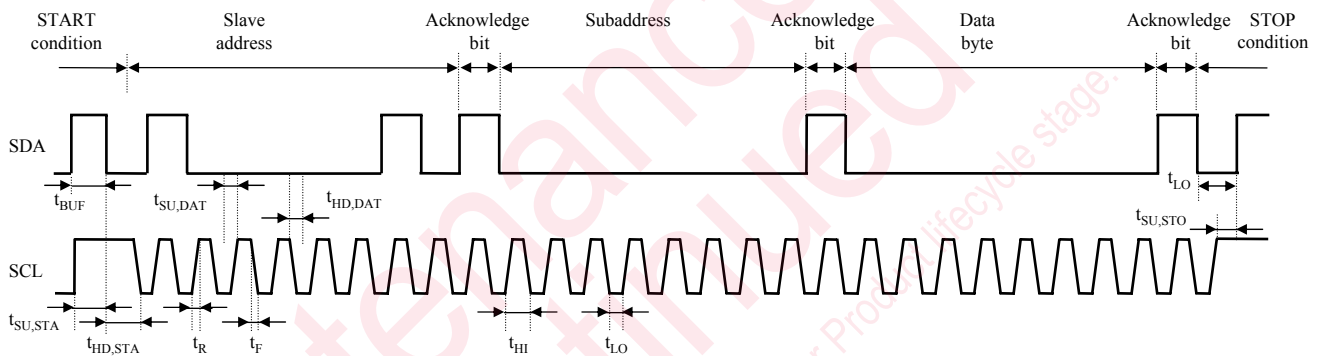
B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
<b>I<sup>2</sup>C interface</b>								
1	Bus free before start	$t_{BUF}$	—	4.0	—	—	$\mu\text{s}$	—
2	Set-up time of START condition	$t_{SU,STA}$	—	4.0	—	—	$\mu\text{s}$	—
3	Hold time of START condition	$t_{HD,STA}$	—	4.0	—	—	$\mu\text{s}$	—
4	Low period of SCL, SDA	$t_{LO}$	—	4.0	—	—	$\mu\text{s}$	—
5	High period of SCL	$t_{HI}$	—	4.0	—	—	$\mu\text{s}$	—
6	SCL, SDA rise time	$t_R$	—	—	—	1.0	$\mu\text{s}$	—
7	SCL, SDA fall time	$t_F$	—	—	—	0.35	$\mu\text{s}$	—
8	Data set-up time (Write)	$t_{SU,DAT}$	—	0.25	—	—	$\mu\text{s}$	—
9	Data hold time (Write)	$t_{HD,DAT}$	—	0	—	—	$\mu\text{s}$	—
10	Acknowledge set-up time	$t_{SU,ACK}$	—	—	—	3.5	$\mu\text{s}$	—
11	Acknowledge hold time	$t_{HD,ACK}$	—	0	—	—	$\mu\text{s}$	—
12	[STOP] condition set-up time	$t_{SU,STO}$	—	4.0	—	—	$\mu\text{s}$	—
<b>DAC</b>								
13	6 bit DAC DNLE	$L_6$	1LSB = [Data (max) – Data (00)]/63	0.1	1.0	1.9	LSB/ STEP	—

### ■ Electrical Characteristics (Reference values for design) (continued) at $V_{CC} = 9\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

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■ Electrical Characteristics (Reference values for design) (continued) at  $V_{CC} = 9.0\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
14	AGC gain 3 (Sub address 04H : 05H)	$V_{AGC3}$	$V_{IN} = 100\text{ mV[rms]}$ $f = 1\text{ kHz}$	—	150	—	mV[rms]	*1
15	AGC gain 4 (Sub address 04H : 03H)	$V_{AGC4}$	$V_{IN} = 140\text{ mV[rms]}$ $f = 1\text{ kHz}$	—	200	—	mV[rms]	*1
16	AGC gain 5 (Sub address 04H : 01H)	$V_{AGC5}$	$V_{IN} = 200\text{ mV[rms]}$ $f = 1\text{ kHz}$	—	250	—	mV[rms]	*1
17	AGC gain 6 (Sub address 04H : 07H)	$V_{AGC6}$	$V_{IN} = 280\text{ mV[rms]}$ $f = 1\text{ kHz}$	—	350	—	mV[rms]	*1
18	AGC gain 7 (Sub address 04H : 03H)	$V_{AGC7}$	$V_{IN} = 500\text{ mV[rms]}$ $f = 1\text{ kHz}$	180	290	430	mV[rms]	*1

Note) \*1 : DIN AUDIO filter used.

### ■ Electrical Characteristics Test Procedures

C No.	Parameter	Symbol	SW						Input conditions	Sub address				
			1	2	3	4	5	6		00H	01H	02H	03H	04H
1	Quiescent Current	$I_{CC T}$	—	—	—	—	ON	OFF	$V_{IN} = 0 \text{ mV}$	FC	80	77	00	00
2	Volume (Max Level)	$V_{Vmax}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	00
3	Volume (Mid Level)	$V_{Vmid}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	80	80	77	00	00
4	Volume (Min Level)	$V_{Vmin}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	00	80	77	00	00
5	THD (1 kHz)	$THD_{max}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	00
6	Max input level	$V_{Imax}$	b, a	a, b	b, a	a	ON	OFF	$THD = 1\%$ $f = 1 \text{ kHz}$	FC	80	77	00	00
7	Output noise at volume min	$V_{Nmin}$	c	c	b, a	b	ON	OFF	$V_{IN} = 0 \text{ mV}$ $R_g = 4.7 \text{ k}\Omega$	00	80	77	00	00
8	Output noise at volume max	$V_{Nmax}$	c	c	b, a	b	ON	OFF	$V_{IN} = 0 \text{ mV}$ $R_g = 4.7 \text{ k}\Omega$	FC	80	77	00	00
9	Mute Level	$V_{MUTE}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FE	80	77	00	00
10	Balance (Max Level)	$V_{Bmax}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FC	FC, 00	77	00	00
11	Balance (Min Level)	$V_{Bmin}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FC	FC, 00	77	00	00
12	Bass (Max Level)	$VB_{Bmax}$	b, a	a, b	b, a	c	ON	OFF	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	FC	80	7F	00	00
13	Bass (Min Level)	$VB_{Bmin}$	b, a	a, b	b, a	c	ON	OFF	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	FC	80	70	00	00
14	Treble (Max Level)	$VT_{Bmax}$	b, a	a, b	b, a	c	ON	OFF	$V_{IN} = 400 \text{ mV[rms]}$ $f = 20 \text{ kHz}$	FC	80	F7	00	00
15	Treble (Min Level)	$VT_{Bmin}$	b, a	a, b	b, a	c	ON	OFF	$V_{IN} = 400 \text{ mV[rms]}$ $f = 20 \text{ kHz}$	FC	80	07	00	00
16	Super bass (Max Level)	$VX_{Bmax}$	b, a	a, b	b, a	c	ON	OFF	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	FD	80	77	00	00
17	Super bass (Min Level)	$VX_{Bmin}$	b, a	a, b	b, a	c	ON	OFF	$V_{IN} = 400 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	FD	83	77	00	00

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Symbol	SW						Input conditions	Sub address				
			1	2	3	4	5	6		00H	01H	02H	03H	04H
18	AGC gain 1	$V_{AGC1}$	b, a	a, b	a, b	a	ON	OFF	$V_{IN} = 50 \text{ mV[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	03
19	AGC gain 2	$V_{AGC2}$	b, a	a, b	a, b	a	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	03
20	Surround level 1	$V_{SU1}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 50 \text{ mV[rms]}$ $f = 50 \text{ Hz}$	FC	80	77	80	00
21	Surround level 2	$V_{SU2}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 50 \text{ mV[rms]}$ $f = 10 \text{ kHz}$	FC	80	77	80	00
22	Surround noise Level	$V_{SN}$	c	c	b, a	b	ON	OFF	$V_{IN} = 0 \text{ mV[rms]}$ $R_g = 4.7 \text{ k}\Omega$	FC	80	77	80	00
23	THD (Surround)	$THD_{SU}$	b, a	a, b	a	a	ON	OFF	$V_{IN} = 400 \text{ mV[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	80	00
24	Cross talk	CT	b, a	a, b	a, b	b	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	00
25	Channel balance (Max)	$CB_{max}$	—	—	—	—	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	00
26	Channel balance (1/4)	$CB_{1/4}$	—	—	—	—	ON	OFF	$V_{IN} = 1 \text{ V[rms]}$ $f = 1 \text{ kHz}$	40	80	77	00	00

■ Electrical Characteristics (Reference values for design) Test Procedures

C No.	Parameter	Symbol	SW						Input conditions	Sub address				
			1	2	3	4	5	6		00H	01H	02H	03H	04H
14	AGC gain 3	$V_{AGC3}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 100 \text{ mV[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	05
15	AGC gain 4	$V_{AGC4}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 140 \text{ mV[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	03
16	AGC gain 5	$V_{AGC5}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 200 \text{ mV[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	01
17	AGC gain 6	$V_{AGC6}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 280 \text{ mV[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	07
18	AGC gain 7	$V_{AGC7}$	b, a	a, b	b, a	a	ON	OFF	$V_{IN} = 500 \text{ mV[rms]}$ $f = 1 \text{ kHz}$	FC	80	77	00	03



■ Technical Data

- I/O block circuit diagrams and pin function descriptions

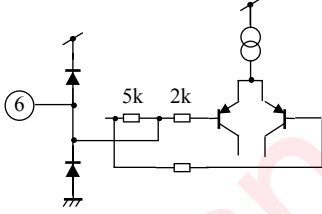
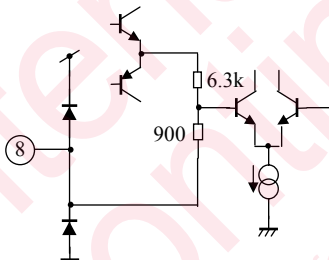
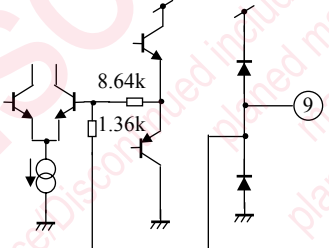
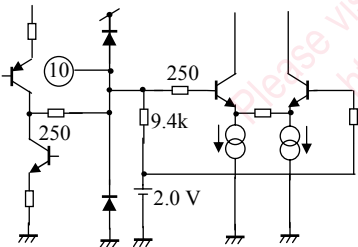
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
1	4.5 V		Phase filter 1
2	Depend on input level 0.5 V to 2.0 V		AGC level sensor
3	4.5 V		L-ch. input
4	4.5 V		Phase filter 2
5	4.5 V		Phase filter 3

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
6	4.5 V		Phase filter 4
7	0 V	—	GND
8	4.5 V		L-ch. Treble Fc adjustment
9	4.5 V		L-ch. Bass Fc adjustment
10	Depend on I <sup>2</sup> C data 1.6 V to 2.5 V		Bass DAC output

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

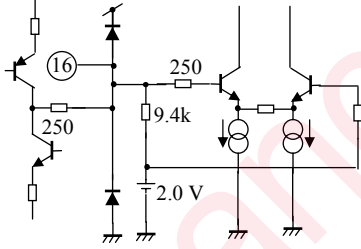
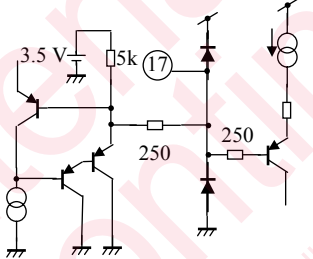
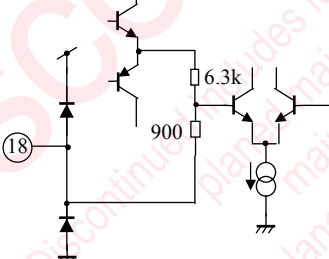
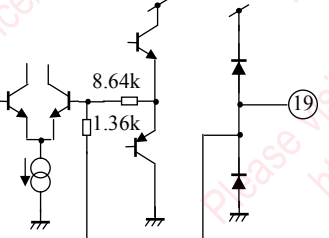
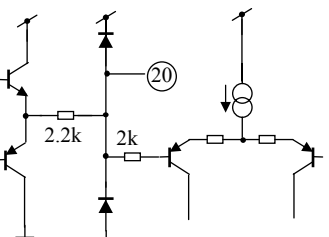
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
11	Depend on I <sup>2</sup> C data 2.0 V to 4.0 V		Volume DAC output
12	4.5 V		L-ch. output
13	—		I <sup>2</sup> C bus clock input
14	—		I <sup>2</sup> C bus data input
15	4.5 V		R-ch. output

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

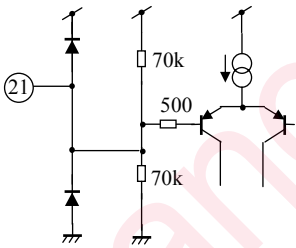
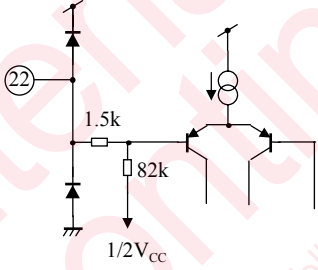
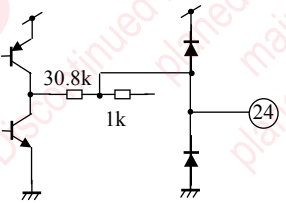
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
16	Depend on I <sup>2</sup> C data 1.6 V to 2.5 V		Treble DAC output
17	Depend on I <sup>2</sup> C data 2.5 V to 3.5 V		Balance DAC output
18	4.5 V		R-ch. Treble Fc adjustment
19	4.5 V		R-ch. Bass Fc adjustment
20	4.5 V		Bass mix gain adjustment

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
21	4.5 V		Reference voltage stabilizing
22	4.5 V		R-ch. input
23	9.0 V	—	V <sub>CC</sub>
24	Depend on I <sup>2</sup> C data 0.6 V to 2.6 V		Mode control

## ■ Technical Data (continued)

### • I<sup>2</sup>C-bus

#### 2. Transmission Message

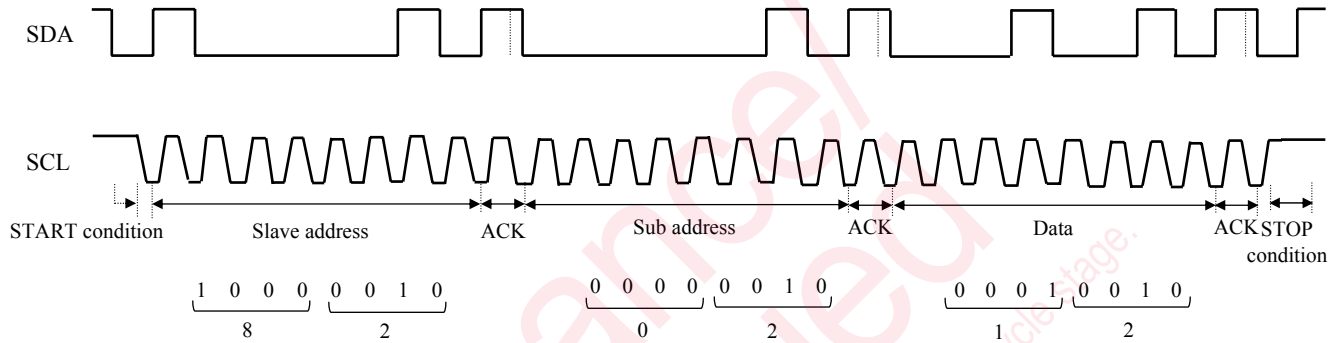


Fig.1 Example of transmission message

For transmission messages, both SCL and SDA are transferred in the form of synchronized serial transmission. SCL is a clock of a specific frequency, and SDA indicates address data for controlling the receiving side and is transferred in parallel, being synchronized with SCL.

Data is transferred in principle in 3 octets (bytes), and each one octet (one octet = 8 bits) includes one acknowledge bit.

Frame structure is described below.

- (a) START condition  
The receiver becomes possible to receive data when SDA changes from High to Low while SCL is High.
- (b) STOP condition  
The receiver halts receiving when SDA changes from Low to High while SCL is High.
- (c) Slave address  
This is an address which is determined for each device. If other device address is sent, receiving will be halted.
- (d) Sub address  
This is an address which is determined for each function.
- (e) Data  
This is control data.
- (f) Acknowledge bit  
This is a bit by which the master acknowledges that data was successfully received in each octet. Master sends the High signal and the receiver sends back the Low signal as shown in Figure 1 with dotted line, causing the master to acknowledge the reception by the receiver. If the Low signal is not returned, communication will be halted. Except START and STOP conditions, SDA does not change while SCL is High.

## ■ Technical Data (continued)

### • I<sup>2</sup>C-bus (continued)

#### 3. I<sup>2</sup>C Bus Addressing

(1) This contains 7 DAC controls and 4 SWs.

(2) オートインクリメント機能は以下のとおりです。

- Sub address 0xxxxxx : Auto-increment mode

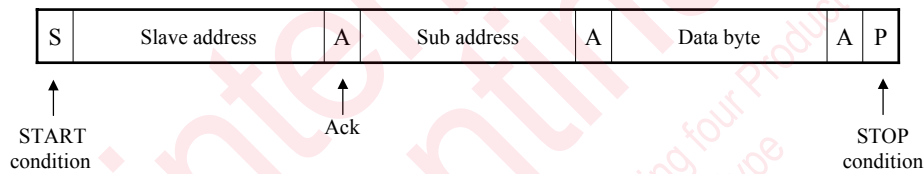
(When the data is sent in consecutive order, the Sub address will be changed in consecutive order, as data is input.)

- Sub address 1xxxxxx : Data update mode

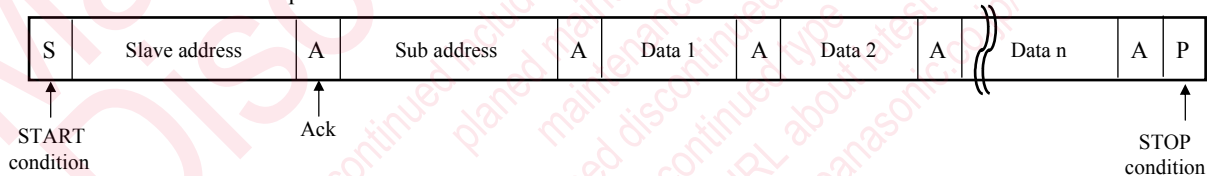
(When the data is sent consecutively, it is sent to the same Sub address.)

(3) I<sup>2</sup>C bus protocol

- Slave address : 10000010 (82H)
- Format (Usual)



- Auto increment mode/Data update mode



(4) Since the DAC initial status is not guaranteed, the standard data input is certainly necessary when power is turned ON.

### ■ Technical Data (continued)

- I<sup>2</sup>C-bus (continued)

#### 3. I<sup>2</sup>C Bus Addressing (continued)

##### (5) Sub address byte and data byte format

Sub address	Data byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00	Volume						Mute ON/OFF	Super Bass ON/OFF
01	Balance						BASS Mix Effect	
02	L/R Treble				L/R Bass			
03	MODE	×	×	Surround Effect				
04	Not defined					AGC ADJ		AGC ON/OFF

#### 1) MODE

"00" = Bypass  
 "01" = Simulated Stereo  
 "10" = Stereo Surround  
 "11" = Mono surround

#### 2) Volume

DATA = "000000" : min  
 DATA = "111111" : max

#### 3) Balance

DATA = "000000" : Lout : min, Rout : max  
 DATA = "100000" : CENTER  
 DATA = "111111" : Lout : max, Rout : min

#### 4) L/R Treble, Bass

DATA = "0000" : min  
 DATA = "0111" : CENTER  
 DATA = "1111" : max

#### 5) Mute ON/OFF

DATA = "0" : OFF  
 DATA = "1" : ON

#### 6) Bass Mix ON/OFF

DATA = "0" : OFF  
 DATA = "1" : ON

#### 7) Bass Mix Effect

DATA = "11" : min  
 DATA = "00" : max

#### 8) AGC ON/OFF

DATA = "0" : OFF  
 DATA = "1" : ON

#### 9) AGC ADJ (0 dB Adjustment) \*

DATA = "00" : 200 mV[rms]  
 DATA = "01" : 140 mV[rms]  
 DATA = "10" : 100 mV[rms]  
 DATA = "11" : 280 mV[rms]

#### 10) Surround Effect

DATA = "1111" : min  
 DATA = "0000" : max

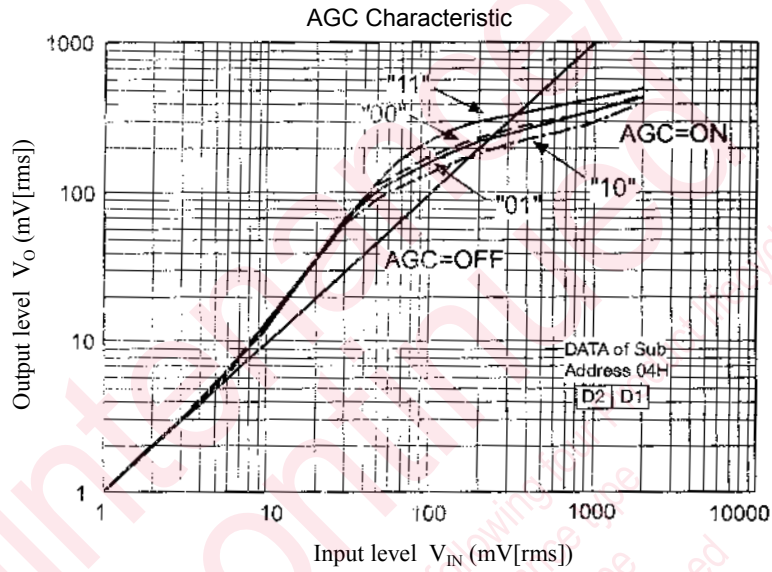
Note) \* : 0 dB Adjustment level of AGC is reference value, and not guaranteed by shipping inspection.



### ■ Technical Data (continued)

- Adjust method of AGC control

AGCがONの場合、入出力ゲインは小信号レベルにおいては0 dB、標準信号レベルでは上昇し、大信号レベルでは減少します。また、AGCの入出力特性は下記のとおりICによって制御できます。



## ■ Usage Notes

### • Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [Television].  
Consult our sales staff in advance for information on the following applications:
  - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
    - (1) Space appliance (such as artificial satellite, and rocket)
    - (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
    - (3) Medical equipment for life support
    - (4) Submarine transponder
    - (5) Control equipment for power plant
    - (6) Disaster prevention and security device
    - (7) Weapon
    - (8) Others : Applications of which reliability equivalent to (1) to (7) is required
2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin- $V_{CC}$  short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .  
And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.  
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
7. When using the LSI for new models, verify the safety including the long-term reliability for each product.
8. When the application system is designed by using this LSI, be sure to confirm notes in this book.  
Be sure to read the notes to descriptions and the usage notes in the book.

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- (2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.
- (3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).  
Consult our sales staff in advance for information on the following applications:
  - Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
- (4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
- (5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
  - Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
- (6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
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