# 1.0A, 100V, 0.6 Ohm, P-Channel Power MOSFET

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17501.

## Ordering Information

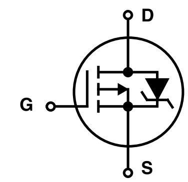
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| IRFD9120 | HEXDIP | IRFD9120 |

NOTE: When ordering, use the entire part number.

## Features

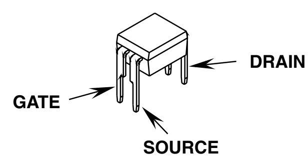
- 1.0A, 100V
- $r_{DS(ON)} = 0.6\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

## Symbol




## Packaging

HEXDIP



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | IRFD9120 | UNITS |
|---|---|---|---|
| Drain to Source Breakdown Voltage (Note 1) | $V_{DS}$ | -100 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | -100 | V |
| Continuous Drain Current | $I_D$ | -1.0 | A |
| Pulsed Drain Current (Note 3) | $I_{DM}$ | -8.0 | A |
| Gate to Source Voltage | $V_{GS}$ | ±20 | V |
| Maximum Power Dissipation (Figure 1) | $P_D$ | 1.0 | W |
| Linear Derating Factor (Figure 1) | | 0.008 | W/$^o$C |
| Single Pulse Avalanche Energy Rating (Note 4) | $E_{AS}$ | 370 | mJ |
| Operating and Storage Temperature | $T_J, T_{STG}$ | -55 to 150 | $^o$C |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^o$C |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | $^o$C |

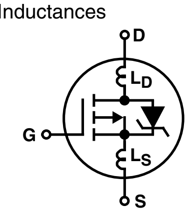
*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $125^oC$.

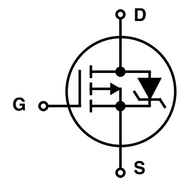
## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = -250μA, $V_{GS}$ = 0V, (Figure 9) | -100 | - | - | V |
| Gate to Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D$ = -250μA | -2 | - | -4 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = Rated $BV_{DSS}$, $V_{GS}$ = 0V | - | - | -25 | μA |
| | | $V_{DS}$ = 0.8 x Rated $BV_{DSS}$, $V_{GS}$ = 0V, $T_C = 125^oC$ | - | - | -250 | μA |
| On-State Drain Current (Note 2) | $I_{D(ON)}$ | $V_{DS} > I_{D(ON)} \times r_{DS(ON)\,MAX}$, $V_{GS}$ = -10V | -1.0 | - | - | A |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20V | - | - | ±500 | nA |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$ | $I_D$ = -0.8A, $V_{GS}$ = -10V, (Figures 7, 8) | - | 0.5 | 0.6 | Ω |
| Forward Transconductance (Note 2) | $g_{fs}$ | $V_{DS}$ < 50V, $I_D$ = -0.8A (Figure 11) | 0.8 | 1.2 | - | S |
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{DD}$ = 0.5 x Rated $BV_{DSS}$, $I_D$ = -1.0A, $R_G$ = 9.1Ω, $V_{GS}$ = -10V, (Figures 16, 17) $R_L$ = 50Ω for $V_{DD}$ = -50V MOSFET Switching Times are Essentially Independent of Operating Temperature | - | 25 | 50 | ns |
| Rise Time | $t_r$ | | - | 50 | 100 | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 50 | 100 | ns |
| Fall Time | $t_f$ | | - | 50 | 100 | ns |
| Total Gate Charge (Gate to Source + Gate to Drain) | $Q_{g(TOT)}$ | $V_{GS}$ = -10V, $I_D$ = -1.0A, $V_{DS}$ = 0.8 x Rated $BV_{DSS}$ (Figures 13, 18, 19) Gate Charge is Essentially Independent of Operating Temperature | - | 16 | 20 | nC |
| Gate to Source Charge | $Q_{gs}$ | | - | 9 | - | nC |
| Gate to Drain "Miller" Charge | $Q_{gd}$ | | - | 7 | - | nC |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = -25V, $V_{GS}$ = 0V, f = 1MHz, (Figure 10) | - | 300 | - | pF |
| Output Capacitance | $C_{OSS}$ | | - | 200 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | - | 50 | - | pF |
| Internal Drain Inductance | $L_D$ | Measured From the Drain Lead, 2.0mm (0.08in) From Header to Center of Die; Modified MOSFET Symbol Showing the Internal Devices Inductances | - | 4.0 | - | nH |
| Internal Source Inductance | $L_S$ | Measured From the Source Lead, 2.0mm (0.08in) From Header to Source Bonding Pad | - | 6.0 | - | nH |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | Typical Socket Mount | - | - | 120 | $^o$C/W |



## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Continuous Source to Drain Current | $I_{SD}$ | Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode   | - | - | -1.0 | A |
| Pulse Source to Drain Current (Note 3) | $I_{SDM}$ | | - | - | -8.0 | A |
| Source to Drain Diode Voltage (Note 2) | $V_{SD}$ | $T_C = 25^oC$, $I_{SD} = -1.0A$, $V_{GS} = 0V$, (Figure 12) | - | - | -1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J = 150^oC$, $I_{SD} = -4.0A$, $dI_{SD}/dt = 100A/\mu s$ | - | 150 | - | ns |
| Reverse Recovery Charge | $Q_{RR}$ | $T_J = 150^oC$, $I_{SD} = -4.0A$, $dI_{SD}/dt = 100A/\mu s$ | - | 0.9 | - | μC |

NOTES:

2. Pulse test: pulse width ≤ 80μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.
4. $V_{DD} = 25V$, starting $T_J = 25^oC$, L = 555mH, $R_G = 25\Omega$, Peak $I_{AS}$= 1.0A (Figures 14, 15).

## *Typical Performance Curves* Unless Otherwise Specified

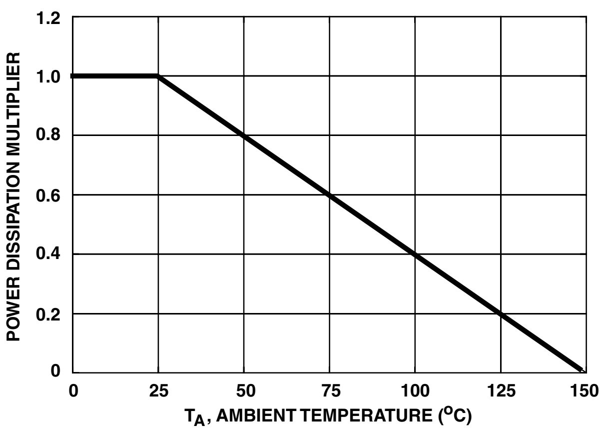



FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

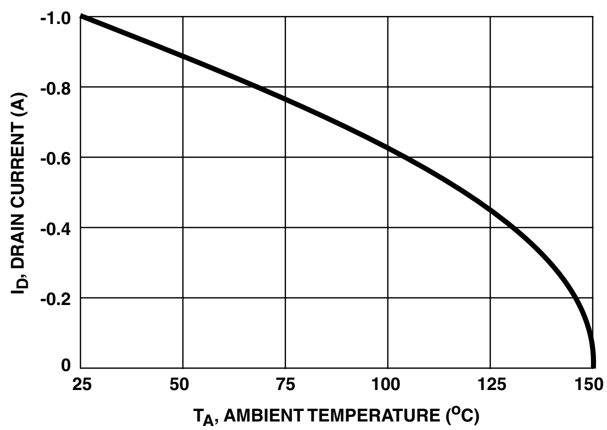



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

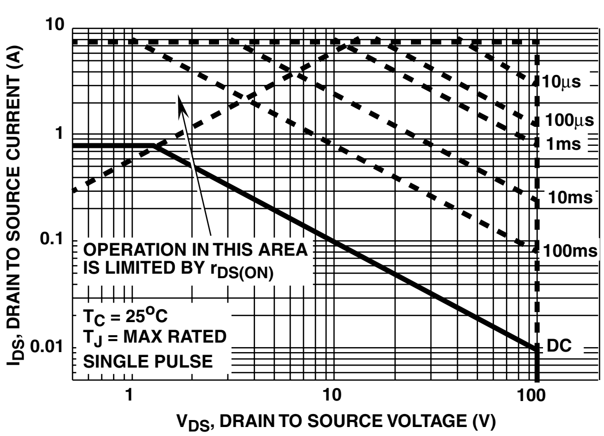



FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

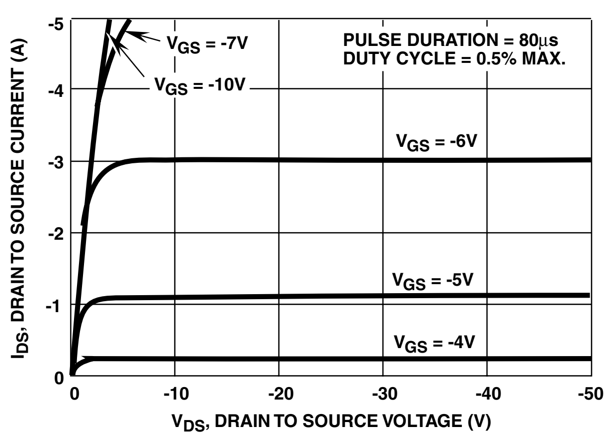



FIGURE 4. OUTPUT CHARACTERISTICS

## Typical Performance Curves Unless Otherwise Specified (Continued)

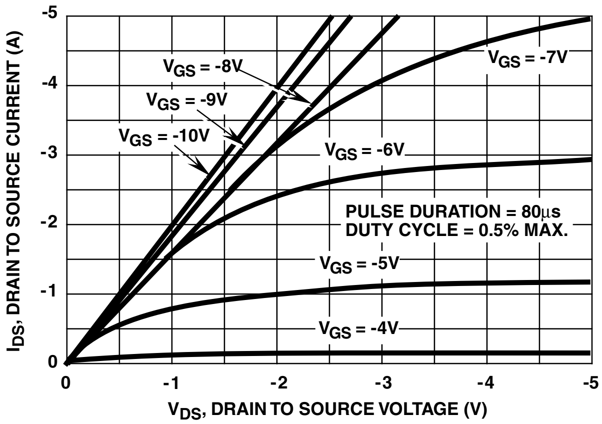



FIGURE 5. SATURATION CHARACTERISTICS

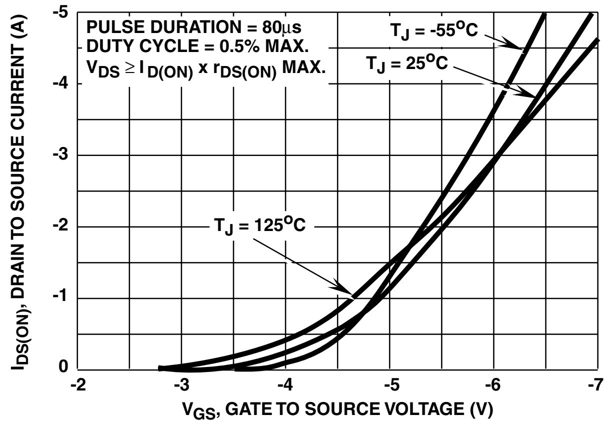
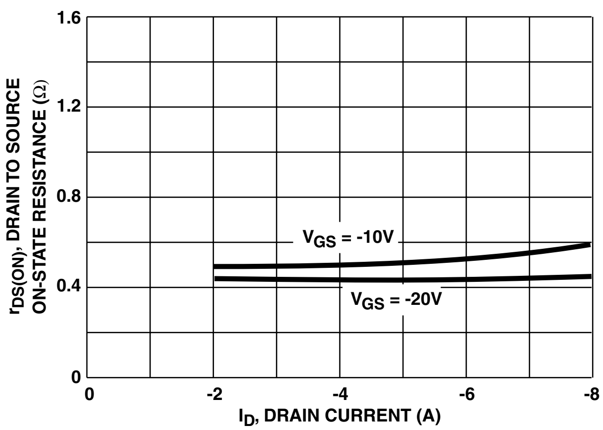



FIGURE 6. TRANSFER CHARACTERISTICS




NOTE: Heating effect of 2µs pulse is minimal.

FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

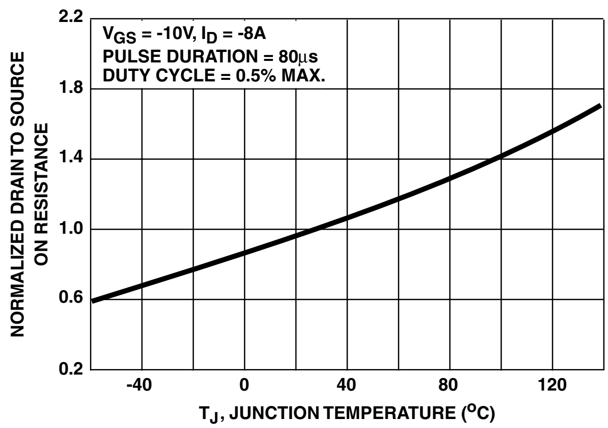



FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

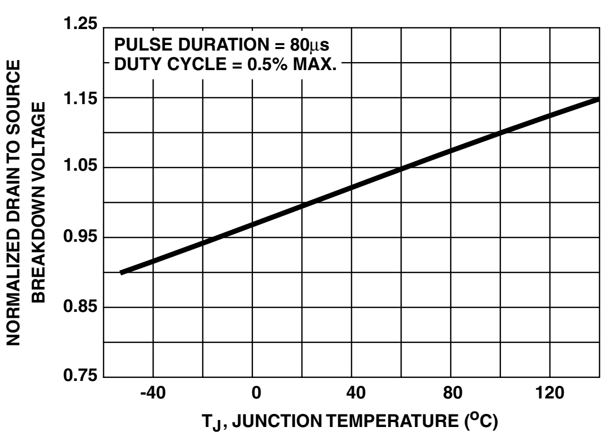



FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

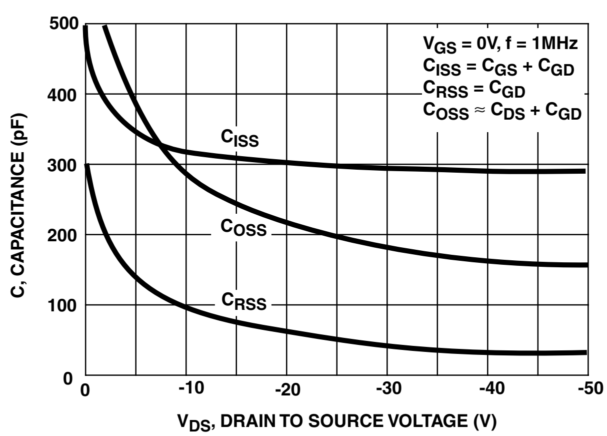



FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

## *Typical Performance Curves* Unless Otherwise Specified **(Continued)**

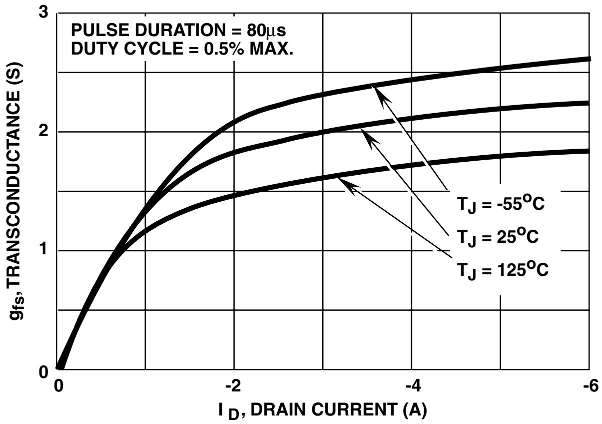



FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

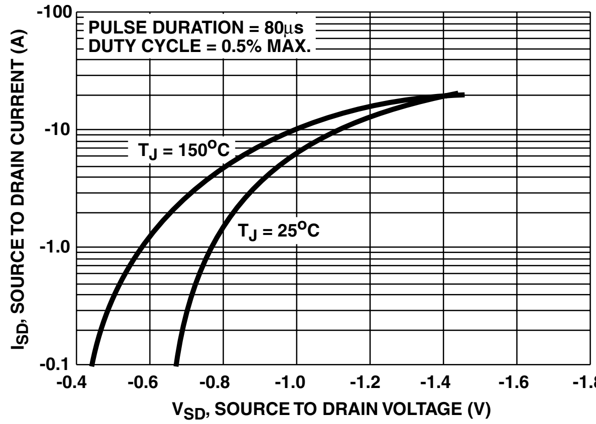



FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

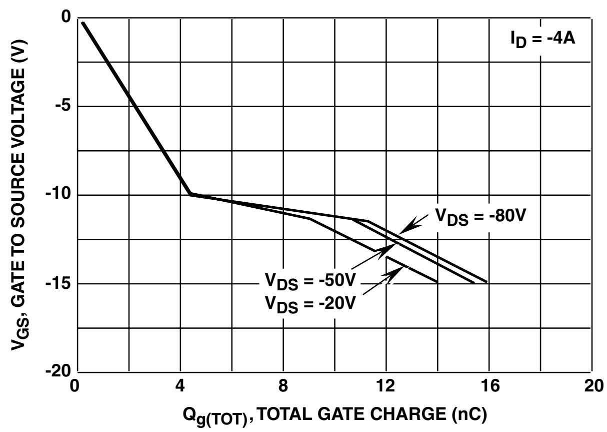



FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

## *Test Circuits and Waveforms*

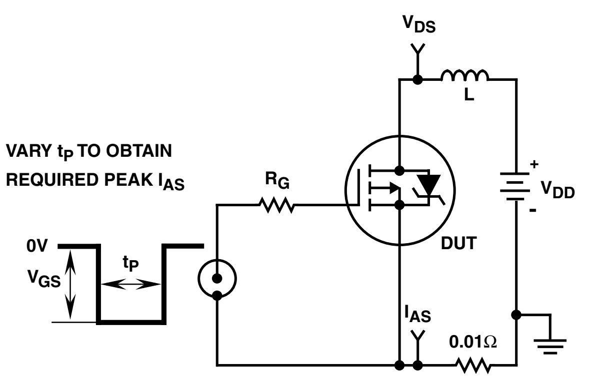



FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

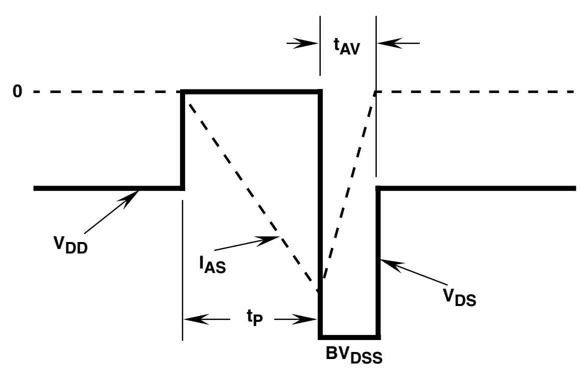



FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

## Test Circuits and Waveforms (Continued)

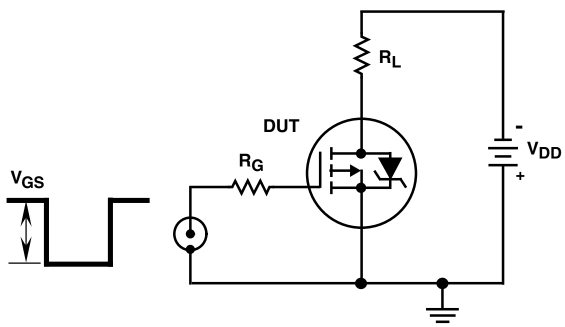



FIGURE 16. SWITCHING TIME TEST CIRCUIT

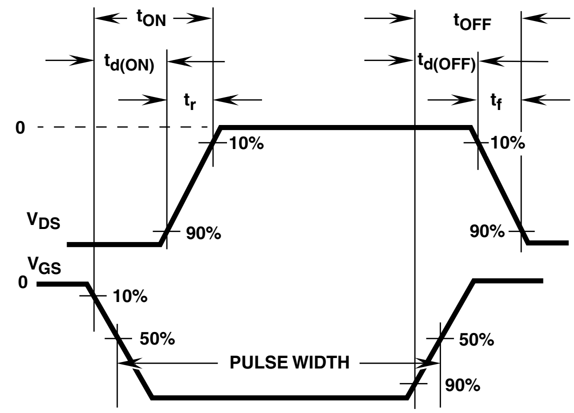



FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

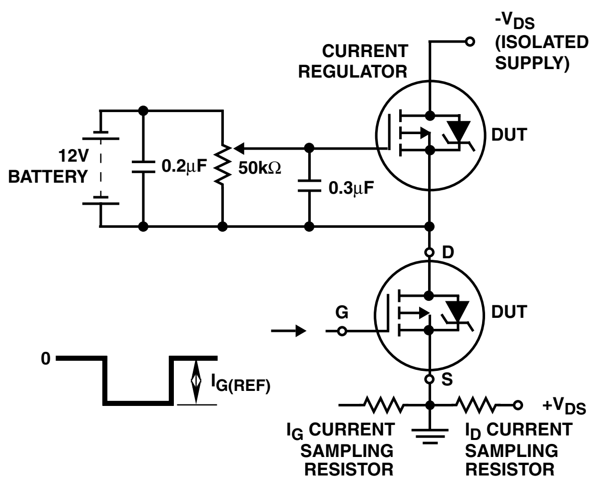



FIGURE 18. GATE CHARGE TEST CIRCUIT

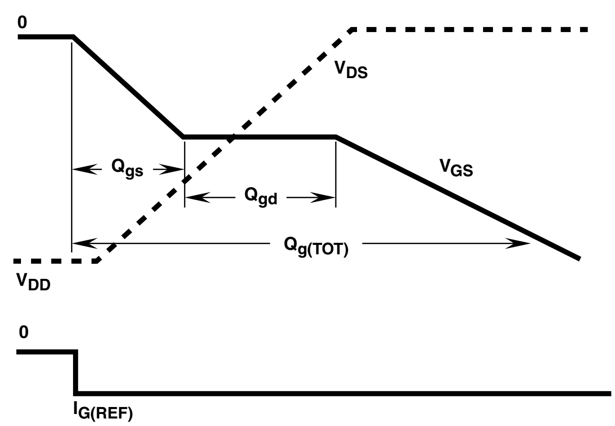



FIGURE 19. GATE CHARGE WAVEFORMS

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| DenseTrench™ | HiSeC™ | QS™ | TinyLogic™ |
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| $E^2$CMOS™ | MicroFET™ | SILENT SWITCHER ® | VCX™ |
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