

IRFPS30N60K

SMPS MOSFET

HEXFET® Power MOSFET

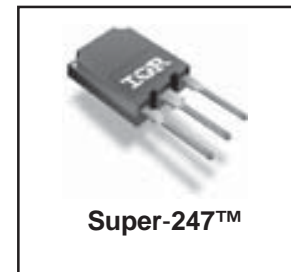
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

V_{DSS}	$R_{DS(on)}$ typ.	I_D
600V	160mΩ	30A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	30	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	19	
I_{DM}	Pulsed Drain Current ①	120	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	450	W
	Linear Derating Factor	3.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	10	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	520	mJ
I_{AR}	Avalanche Current①	—	30	A
E_{AR}	Repetitive Avalanche Energy①	—	45	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.28	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

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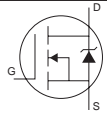
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.66	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	160	190	mΩ	$V_{GS} = 10V, I_D = 18A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	16	—	—	S	$V_{DS} = 50V, I_D = 18A$
Q_g	Total Gate Charge	—	—	220	nC	$I_D = 30A$
Q_{gs}	Gate-to-Source Charge	—	—	64		$V_{DS} = 480V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	110		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	29	—	ns	$V_{DD} = 300V$
t_r	Rise Time	—	120	—		$I_D = 30A$
$t_{d(off)}$	Turn-Off Delay Time	—	56	—		$R_G = 3.9\ \Omega$
t_f	Fall Time	—	50	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	5870	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	530	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	54	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	6920	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	140	—		$V_{GS} = 0V, V_{DS} = 480V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	270	—		$V_{GS} = 0V, V_{DS} = 0V\ \text{to}\ 480V$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	120		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	640	960	ns	$T_J = 25^\circ\text{C}, I_F = 30A$
Q_{rr}	Reverse Recovery Charge	—	11	16	μC	$di/dt = 100A/\mu s$ ④
I_{RRM}	Reverse Recovery Current	—	31	—	A	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.1\text{mH}$, $R_G = 25\ \Omega$, $I_{AS} = 30A$
- ③ $I_{SD} \leq 30A$, $di/dt \leq 420A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss\ eff.}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

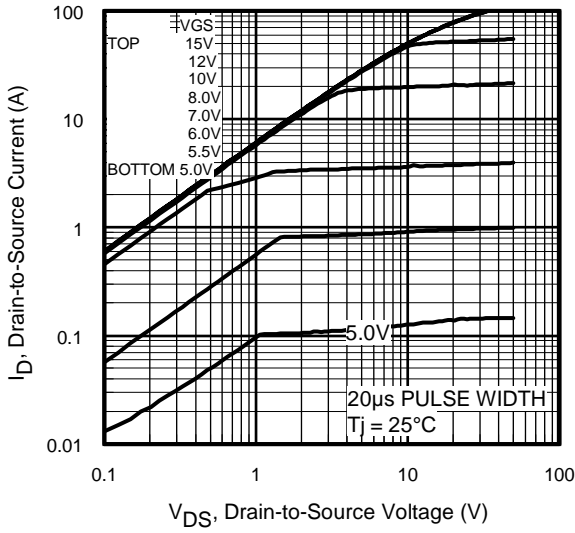


Fig 1. Typical Output Characteristics

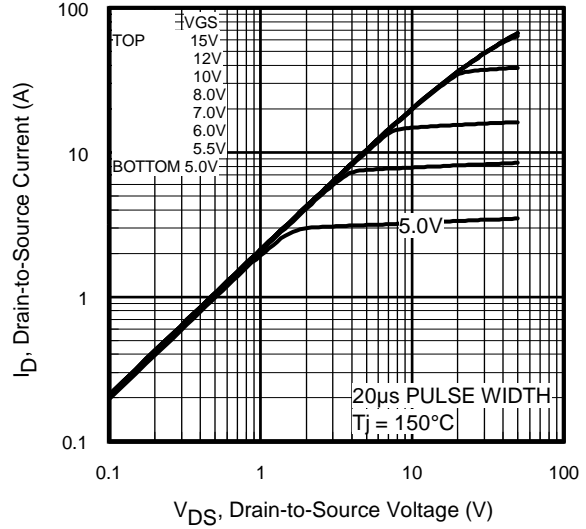


Fig 2. Typical Output Characteristics

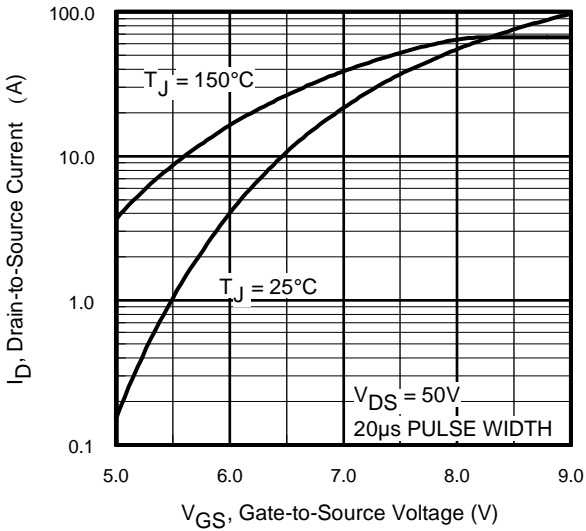


Fig 3. Typical Transfer Characteristics

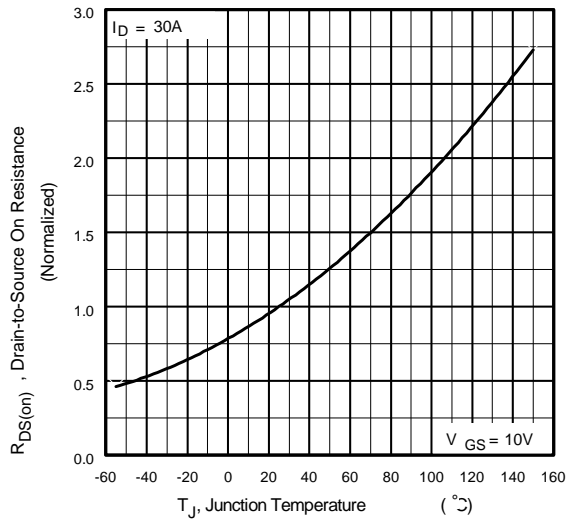


Fig 4. Normalized On-Resistance Vs. Temperature

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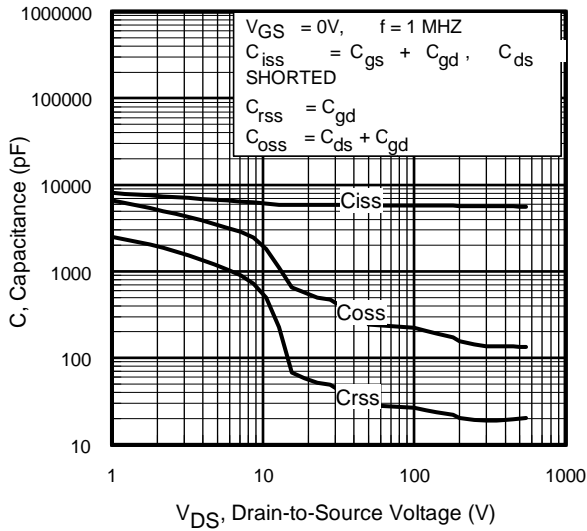


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

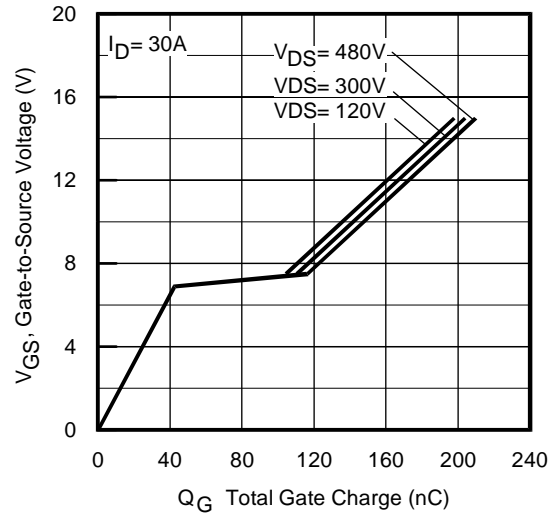


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

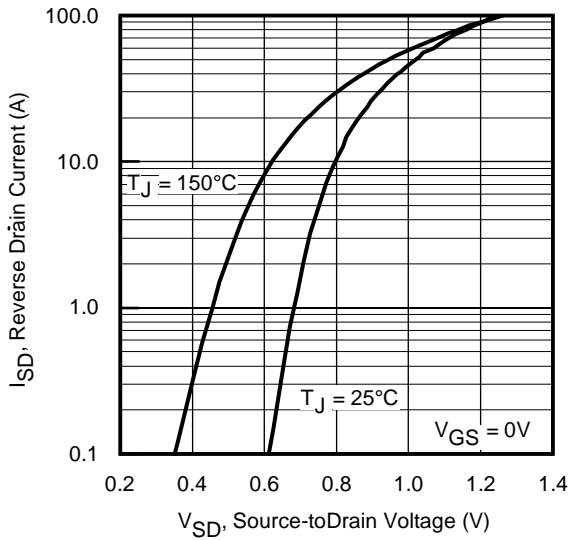


Fig 7. Typical Source-Drain Diode Forward Voltage

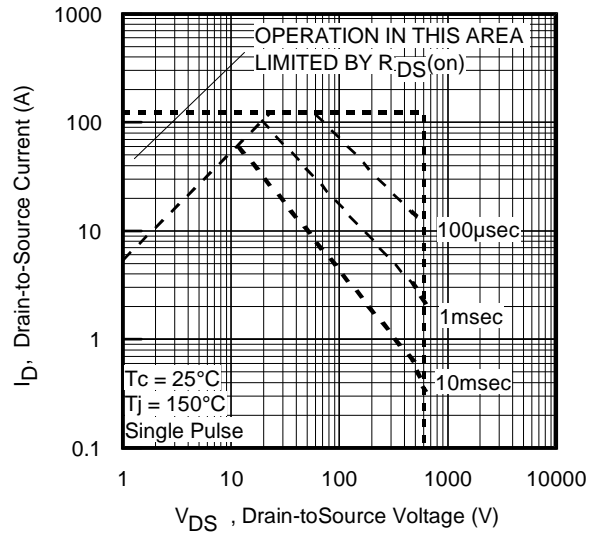


Fig 8. Maximum Safe Operating Area

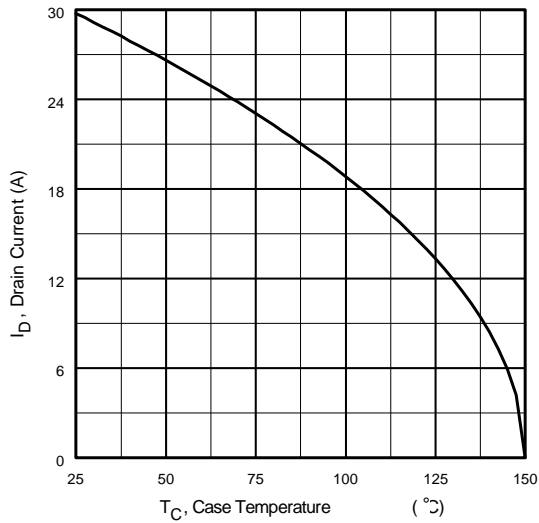


Fig 9. Maximum Drain Current Vs. Case Temperature

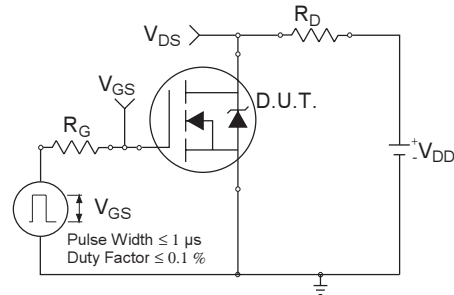


Fig 10a. Switching Time Test Circuit

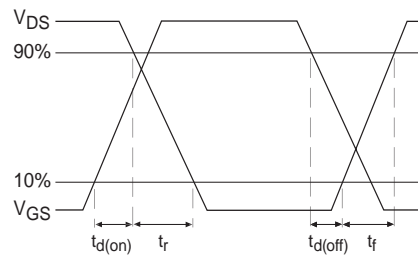


Fig 10b. Switching Time Waveforms

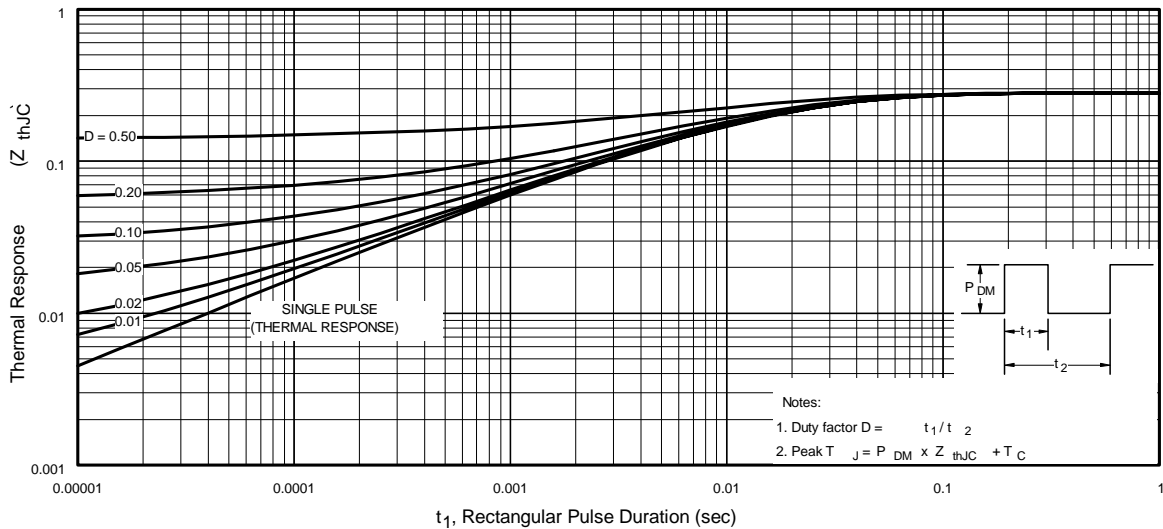


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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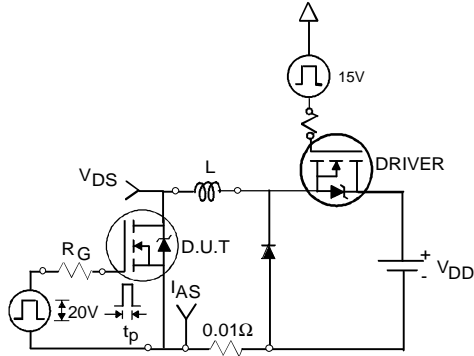


Fig 12a. Unclamped Inductive Test Circuit

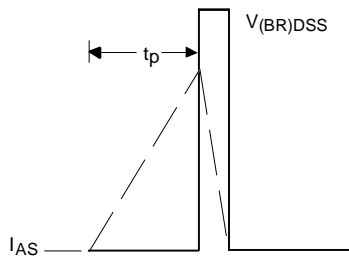


Fig 12b. Unclamped Inductive Waveforms

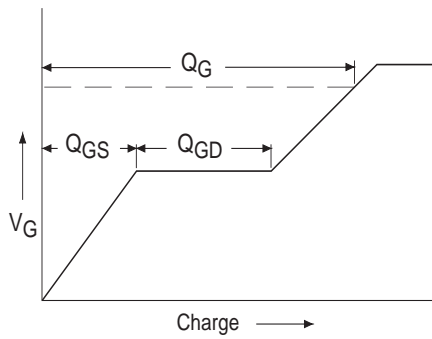


Fig 13a. Basic Gate Charge Waveform

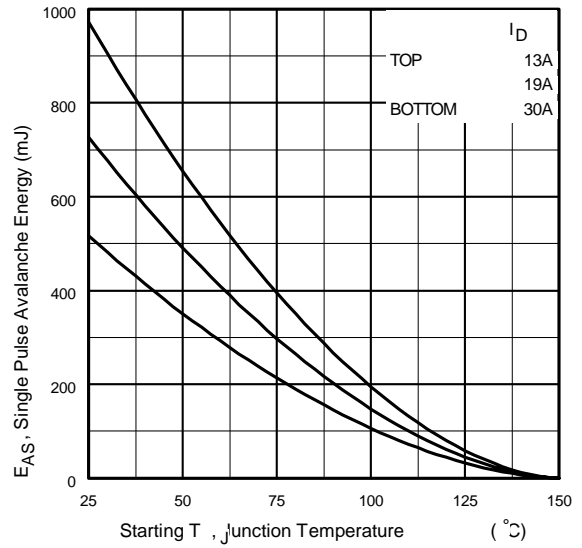


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

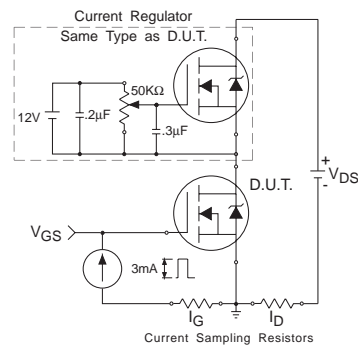
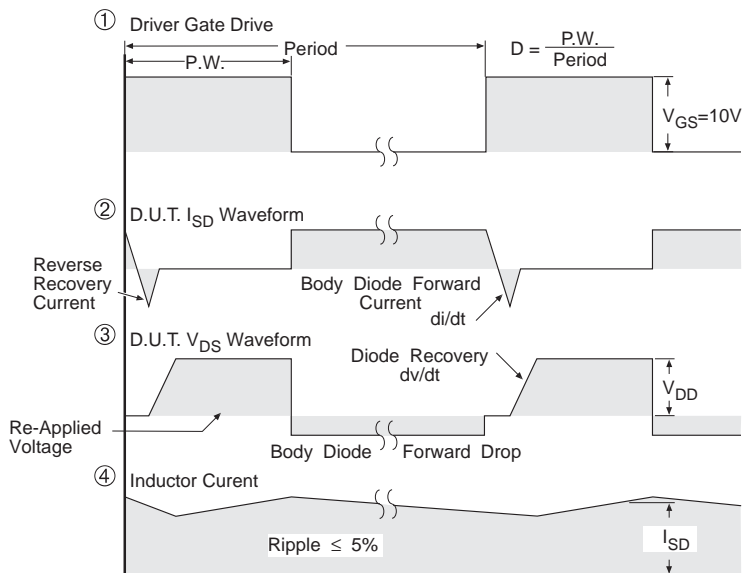
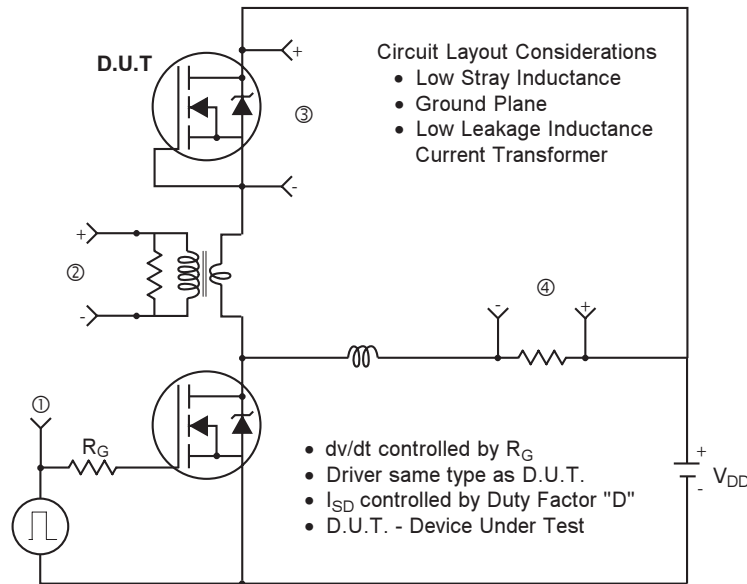


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



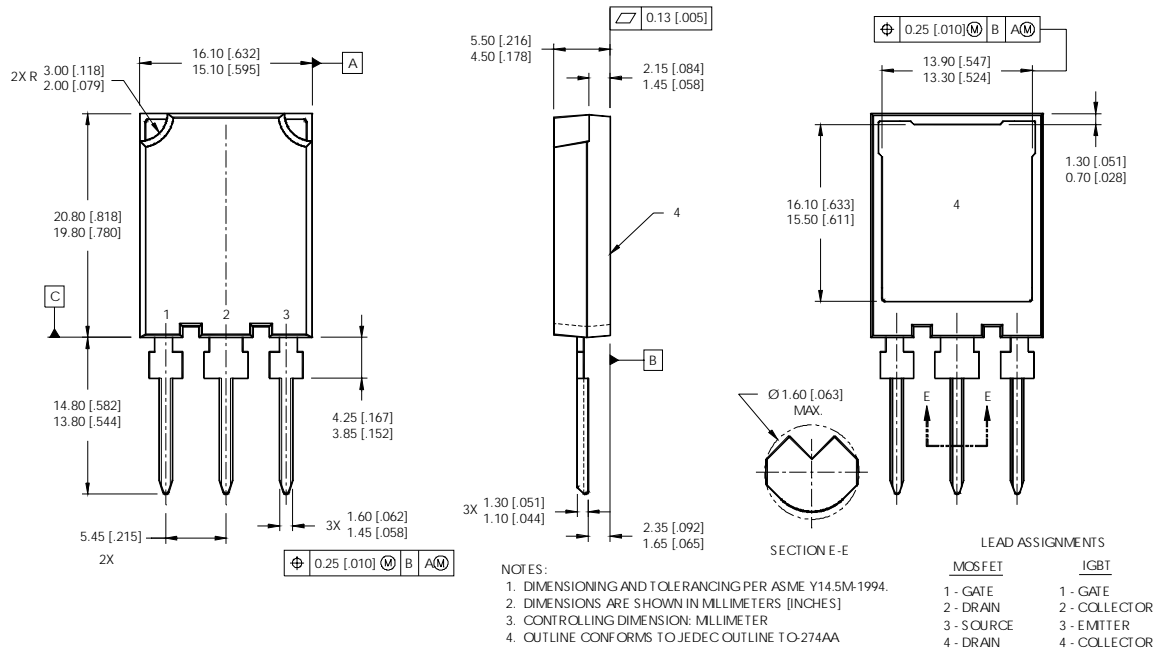
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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Super-247™ Package Outline



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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