STD6N52K3
STF6N52K3

N-channel 525 V, 1 Ω, 5 A, DPAK, TO-220FP SuperMESH3™ Power MOSFET

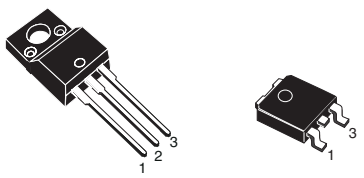
Preliminary Data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STD6N52K3	525 V	< 1.2 Ω	5 A	70 W
STF6N52K3	525 V	< 1.2 Ω	5 A(1)	25 W

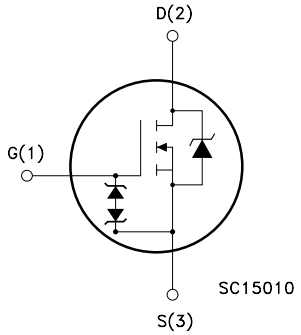
1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected



TO-220FP DPAK

Figure 1. Internal schematic diagram



Application

- Switching applications

Description

The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with a new optimization of the vertical structure. In addition to reducing on-resistance significantly versus previous generation, special attention has been taken to ensure a very good dv/dt capability and higher margin in breakdown voltage for the most demanding application.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD6N52K3	6N52K3	DPAK	Tape and reel
STF6N52K3	6N52K3	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	525		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	5	5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	3.15	3.15(1)	A
I_{DM} (2)	Drain current (pulsed)	20	20 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	W
	Derating factor	0.56	0.2	W/°C
dv/dt (3)	Peak diode recovery voltage slope	9		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)	--	2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 6.3 A, di/dt = TBD, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	DPAK	TO-220FP	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.79	5	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max	50	--	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	--	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	TBD	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	525			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C				1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 30 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.5 A		1.0	1.2	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 2.5 A		TBD		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		TBD TBD TBD		pF pF pF
$C_{OSS\ eq}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 240 V		TBD		pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain		TBD		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 240 V, I_D = 5 A, V_{GS} = 10 V (see *Figure 3*)		TBD TBD TBD		nC nC nC

1. $C_{oss\ eq}$. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_DS increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 150 V, I_D = 3.15 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2*)		TBD TBD TBD TBD		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				6.3 25	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 7*)		TBD TBD TBD		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 7*)		TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
BV_{GSO} (1)	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

3 Test circuits

Figure 2. Switching times test circuit for resistive load

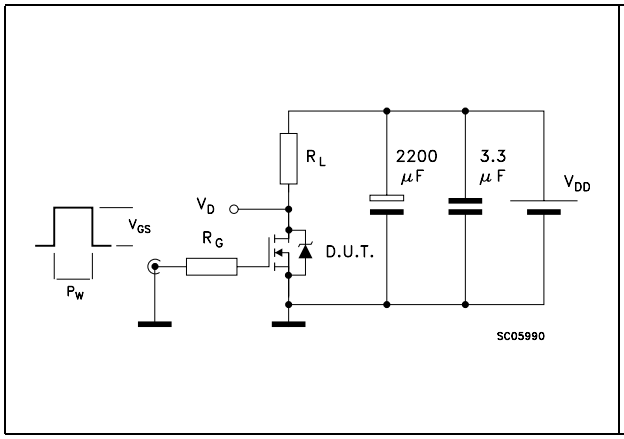


Figure 3. Gate charge test circuit

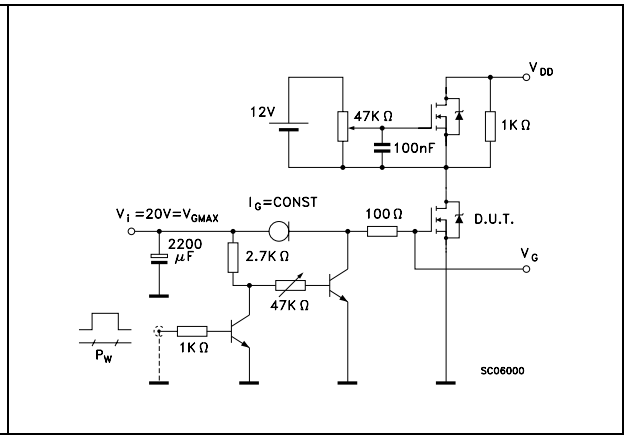


Figure 4. Test circuit for inductive load switching and diode recovery times

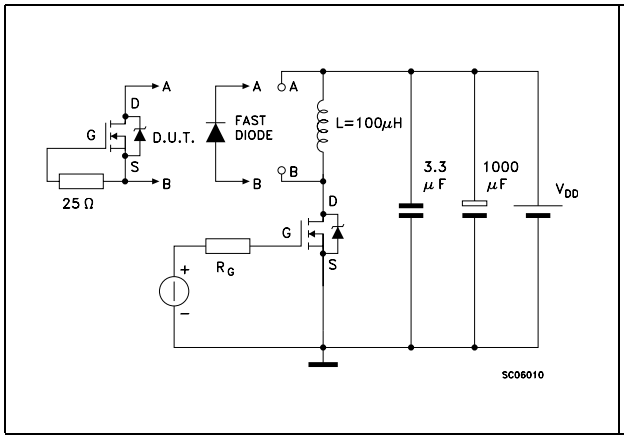


Figure 5. Unclamped Inductive load test circuit

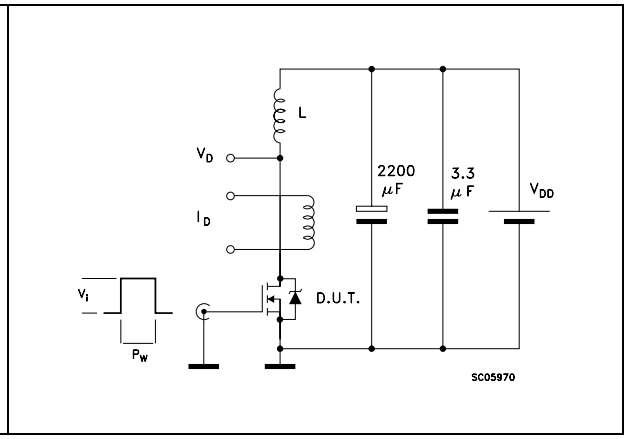


Figure 6. Unclamped inductive waveform

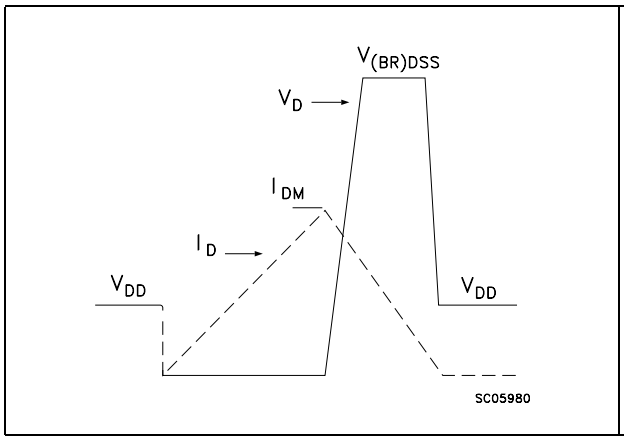
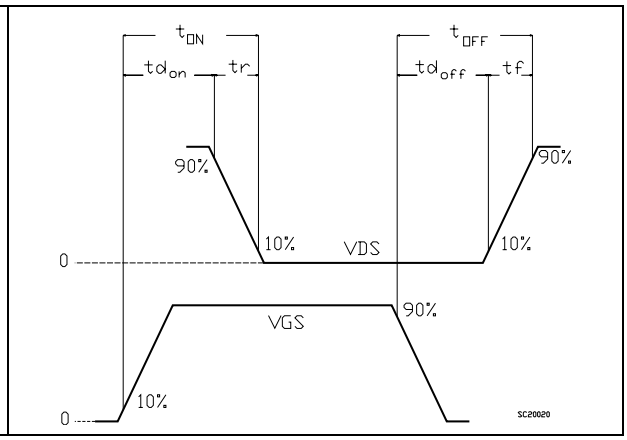


Figure 7. Switching time waveform

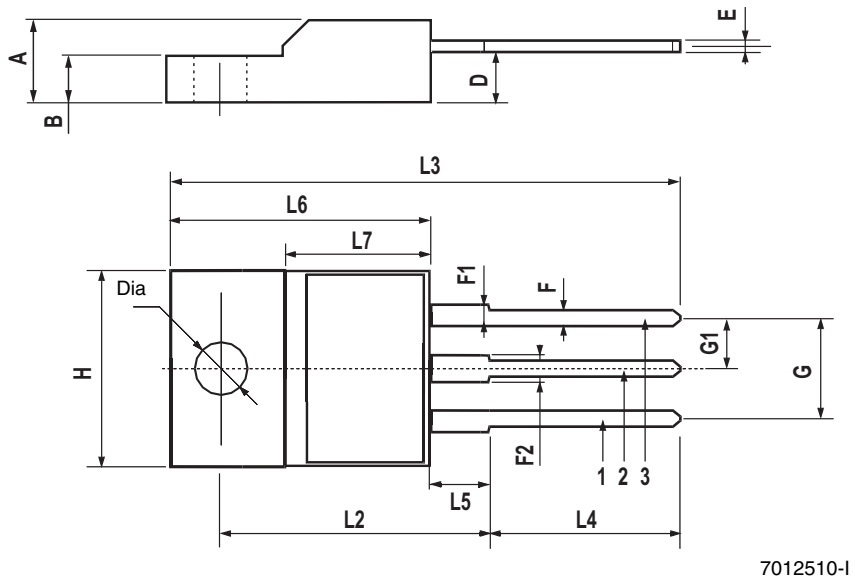


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

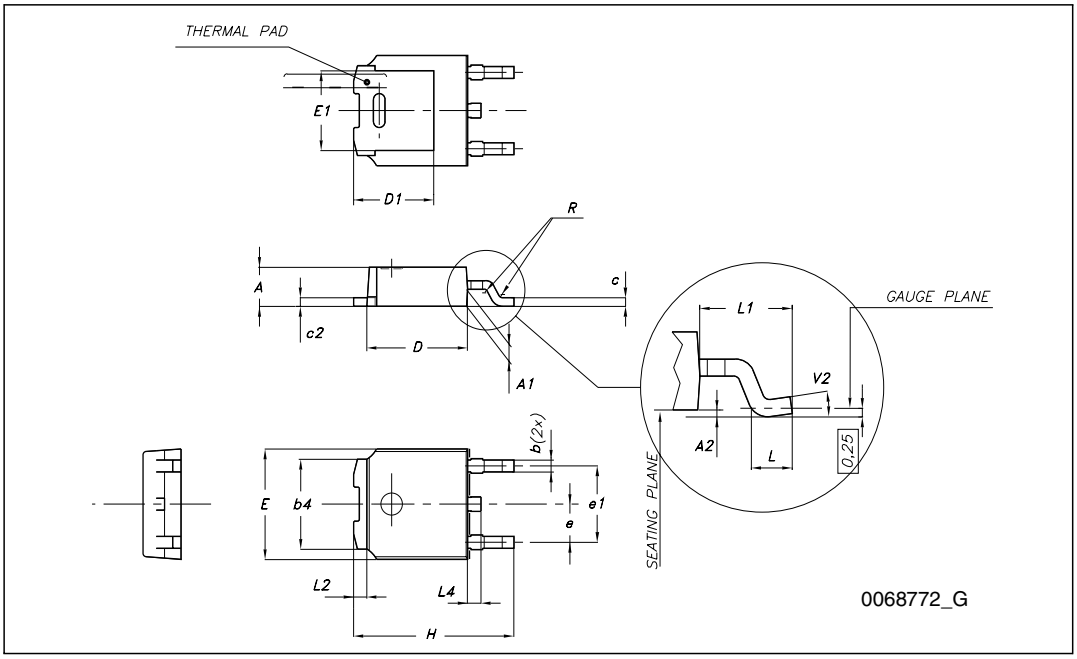
TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



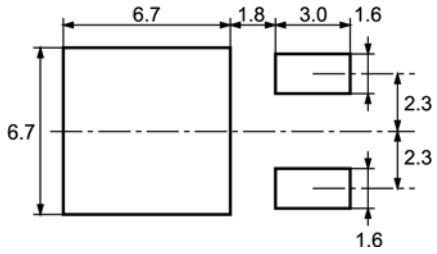
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



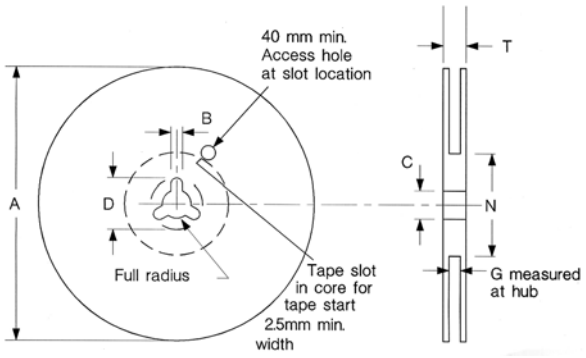
5 Package mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



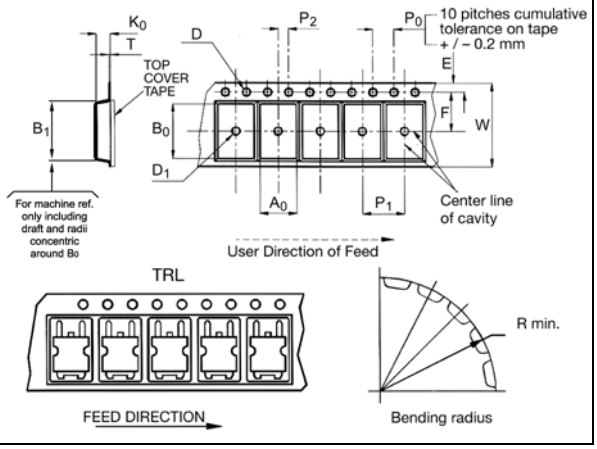
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
03-Sep-2008	1	Initial release