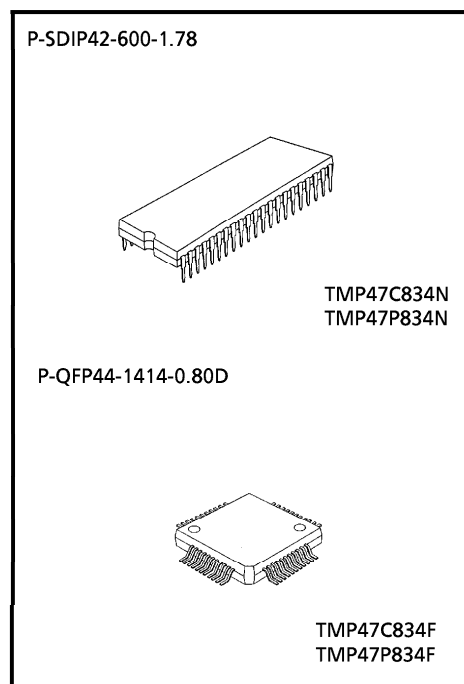## CMOS 4-Bit Microcontroller

TMP47C834N
TMP47C834F

The TMP47C834 are based on the TLCS-470 CMOS series. The TMP47C834 have on-screen display circuit to display characters and marks which indicate channel or time on TV screen, AD converter (comparator) input, and DA converter output such as TV.

Part No.	ROM	RAM	Package	OTP
TMP47C834N	8192 × 8-bit	512 × 4-bit	P-SDIP42-600-1.78	TMP47P834N
TMP47C834F			P-QFP44-1414-0.80D	TMP47P834F

Features

◆4-bit single chip microcomputer

◆Instruction execution time: 1.9 μs (at 4.2 MHz)

◆92 basic instructions

◆Table look-up instructions

◆Subroutine nesting: 15 levels max

◆6 interrupt sources (External: 2, Internal: 4)
   All sources have independent latches each,
   and multiple interrupt control is available

◆I/O port (30 pins)
   ● Input   2 ports   5 pins
   ● I/O   7ports   25 pins

◆Interval Timer

◆Two 12-bit Timer / Counters
   Timer, event counter, and pulse width measurement mode

◆Watchdog timer

◆Serial Interface with 8-bit buffer
   ● Simultaneous transmission and reception capability
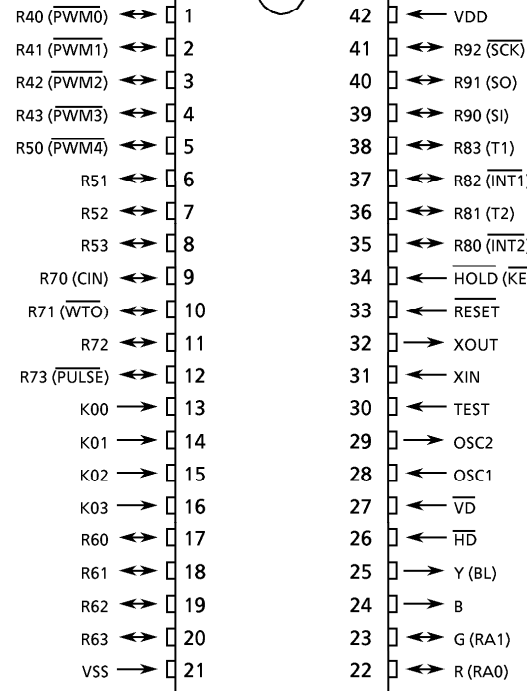   ● External / internal clock, leading / trailing edge shift, 4/8-bit

P-SDIP42-600-1.78

TMP47C834N
TMP47P834N

P-QFP44-1414-0.80D

TMP47C834F
TMP47P834F

000707EBA1

◆On-screen display circuit
- Character patterns: 62 characters
- Characters displayed: 16 columns × 2 lines
- Composition: 8 × 8 dots (smoothing function)
- Size of character: 2 kinds (line by line)
- Color of character: 7 kinds (character by character)
- Variable display position: horizontal 64 / vertical 64 steps
- Double scan mode switching function

◆DA converter (Pulse width modulation) outputs
- 14-bit resolution 1 channel
- 6-bit resolution 4 channels

◆3-bit AD converter (Comparator) input
  Auto frequency control signal (S-shaped curve) detection

◆Pulse output (clock for PLL IC)

◆Horizontal synchronous signal is detected by timer/counter

◆Remote control signal preprocessing capability

◆High current outputs
  LED direct drive capability (typ. 20 mA × 4 bits)

◆HOLD function: Battery / Capacitor back-up

◆Real Time Emulator: BM47C834B

Pin Assignment (Top View)

(1) P-SDIP42-600-1.78

Left	Pin	Pin	Right
R40 (PWM0) ↔	1	42	← VDD
R41 (PWM1) ↔	2	41	↔ R92 (SCK)
R42 (PWM2) ↔	3	40	↔ R91 (SO)
R43 (PWM3) ↔	4	39	↔ R90 (SI)
R50 (PWM4) ↔	5	38	↔ R83 (T1)
R51 ↔	6	37	↔ R82 (INT1)
R52 ↔	7	36	↔ R81 (T2)
R53 ↔	8	35	↔ R80 (INT2)
R70 (CIN) ↔	9	34	← HOLD (KE0)
R71 (WTO) ↔	10	33	← RESET
R72 ↔	11	32	→ XOUT
R73 (PULSE) ↔	12	31	← XIN
K00 →	13	30	← TEST
K01 →	14	29	→ OSC2
K02 →	15	28	← OSC1
K03 →	16	27	← VD
R60 ↔	17	26	← HD
R61 ↔	18	25	→ Y (BL)
R62 ↔	19	24	→ B
R63 ↔	20	23	↔ G (RA1)
VSS →	21	22	↔ R (RA0)

(2) P-QFP44-1414-0.80D

Top pins (33–23): R82 (INT1), R81 (T2), R80 (INT2), HOLD (KE0), RESET, XOUT, XIN, TEST, OSC2, OSC1, VD

Left	Pin	Pin	Right
R83(T1) ↔	34	22	← HD
R90(SI) ↔	35	21	→ Y/BL
R91(SO) ↔	36	20	→ B
R92(SCK) ↔	37	19	↔ G(RA1)
N.C.	38	18	↔ R(RA0)
VDD →	39	17	N.C.
R40(PWM0) ↔	40	16	← VSS
R41(PWM1) ↔	41	15	↔ R63
R42(PWM2) ↔	42	14	↔ R62
R43(PWM3) ↔	43	13	↔ R61
R50(PWM4) ↔	44	12	↔ R60

Bottom pins (1–11): R51, R52, R53, R70 (CIN), R71 (WTO), R72, R73 (PULSE), K00, K01, K02, K03

Block Diagram

Pin Function

Pin Name	Input / Output	Functions		
K03 to K00	input	4-bit input port		
R43 (PWM3) to R41 (PWM1)	I/O (output)	4-bit I/O port with latch. When used as input port or DA converter outputs pins, the latch must be set to "1".		6-bit DA converter (PWM) output
R40 (PWM0)				14-bit DA converter (PWM) output
R53 to R51	I/O			
R50 (PWM4)	I/O (output)			6-bit DA converter (PWM) output
R63 to R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".		
R73 (PULSE)	I/O (output)	4-bit I/O port with latch. When used as input port, watchdog timer output pin, or AD converter input pin, the latch must be set to "1".	PULSE output	
R72	I/O			
R71 (WTO)	I/O (output)		Watchdog timer output	
R70 (CIN)	I/O (input)		3-bit AD converter input	
R83 (T1)	I/O (input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".	Timer / counter 1 external input	
R82 (INT1)			External interrupt 1 input	
R81 (T2)			Timer / counter 2 external input	
R80 (INT2)			External interrupt 2 input	
R92 (SCK)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O	
R91 (SO)	I/O (output)		Serial data output	
R90 (SI)	I/O (input)		Serial data input	
G (RA1)	Output (I/O)	RGB output	2-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R (RA0)				
B	Output			
Y (BL)	Output (output)	Focus signal output	Background blanking control signal output	
HD, VD	Input	Horizontal synchronous signal input, Vertical synchronous signal input		
OSC1, OSC2	input, output	Resonator connecting pin of on-screen display circuit		
XIN, XOUT	input, output	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.		
RESET	input	Reset signal input		
HOLD (KE0)	input (input)	HOLD request/release signal input	Sense input	
TEST	input	Test pin for out-going test. Be opened or fixed to low level.		
VDD	Power supply	+ 5 V		
VSS		0 V (GND)		

Operational Description

Concerning the TMP47C834 the configuration and functions of hardware are described.
As the description has been provided with priority on those parts differing from the TMP47C834, the technical data sheets for the TMP47C834 shall all so be referred to.

1. System Configuration

◆ Internal CPU Function
They are the same as those of the TMP47C860 except system clock controller.

◆ Peripheral Hardware Function
① Input / Output Ports
② Interval Timer
③ Timer / Counters (TC1, TC2)
④ Watchdot Timer
⑤ Remote Control pulse detector
⑥ On-screen display (OSD) control circuit
⑦ AD converter (comparator) input
⑧ DA converter (Pulse Width Modulation) output
⑨ Pulse output circuit

The description has been provide with priority on functions (①, ⑥, ⑦, ⑧ and ⑨) added to and changed from TMP47C860.

2. Internal CPU Function

2.1 Operation clock control

On the TMP47C834 only single clock mode is available. As single clock mode is automatically selected at the initilization, there is no necessary to set system clock control command register (OP16).
After reset, TMP47C834 is placed in the single-clock mode.
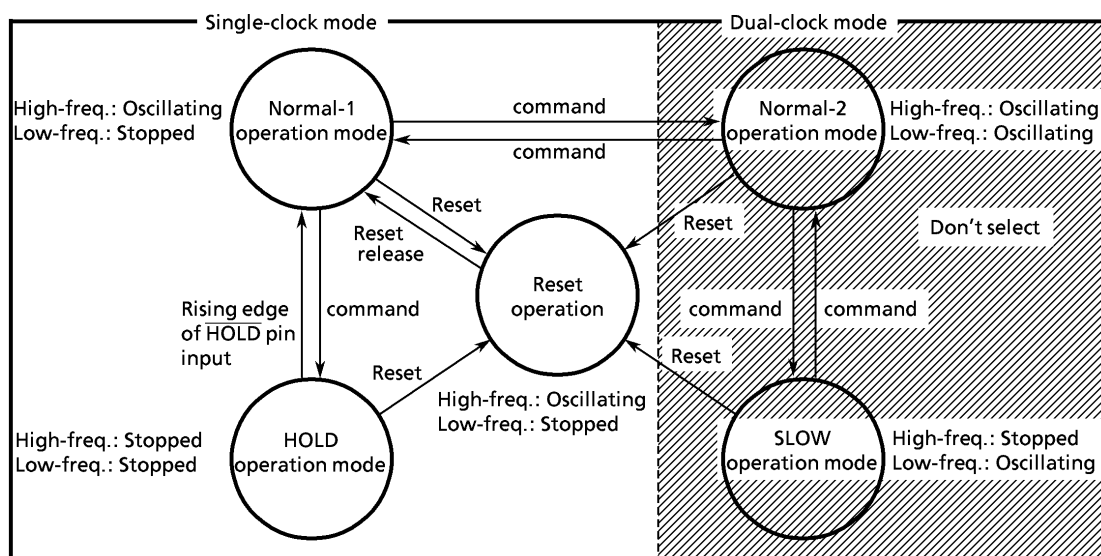Only the normal 1 operating mode can be active.

Figure 2-1. Operation mode transition diagram

3. Peripheral Hardware Function

3.1 I/O ports

The TMP47C834 have 9 I/O ports (30 pins) each as follows.

① K0   ; 4-bit input
② R4 , R5 ; 4-bit input / output (shared with pulse width modulation output)
③ R6   ; 4-bit input / output
④ R7   ; 4-bit input / output (shared with comparator input and watchdog timer output)
⑤ R8   ; 4-bit input / output (shared with external interrupt input and timer / counter input)
⑥ R9   ; 3-bit input / output (shared with serial port)
⑦ RA   ; 2-bit input / output (shared with on-screen display output)
⑧ KE   ; 1-bit sense input (shared with hold request / release signal input)

The description has been provide with priority on functions (② and ④) added to and changed from TMP47C860, and it describes port of ⑦, which item of on-screen display circuit.

(1) Port R4 (R43 to R40)

This is a 4-bit I/O port with latch. It is a port common to DA converter(PWM) output port. R4 port output buffers are Tri-state, and each bit of them can be controled independently by the program. Controling the Tri-state is performed by the command register accessed as port address OP00. When some bit of the OP00 is 0, the corresponding bit of the output buffers becomes high impedance state. The output latch should be set to "1" when the port is used as $\overline{PWM}$ output port,the $\overline{PWM}$ output should be to "H" level(PWM data is all "0")when the port is used as R 4 port. The output buffers should be set to high impedance state,when the port is used as input port. And the R4 output latch be set to "1", $\overline{PWM}$ output be set to "High" level, and the output buffer be set to High-Inpedance state during reset.

R4 (Port Address: OP04/IP04)

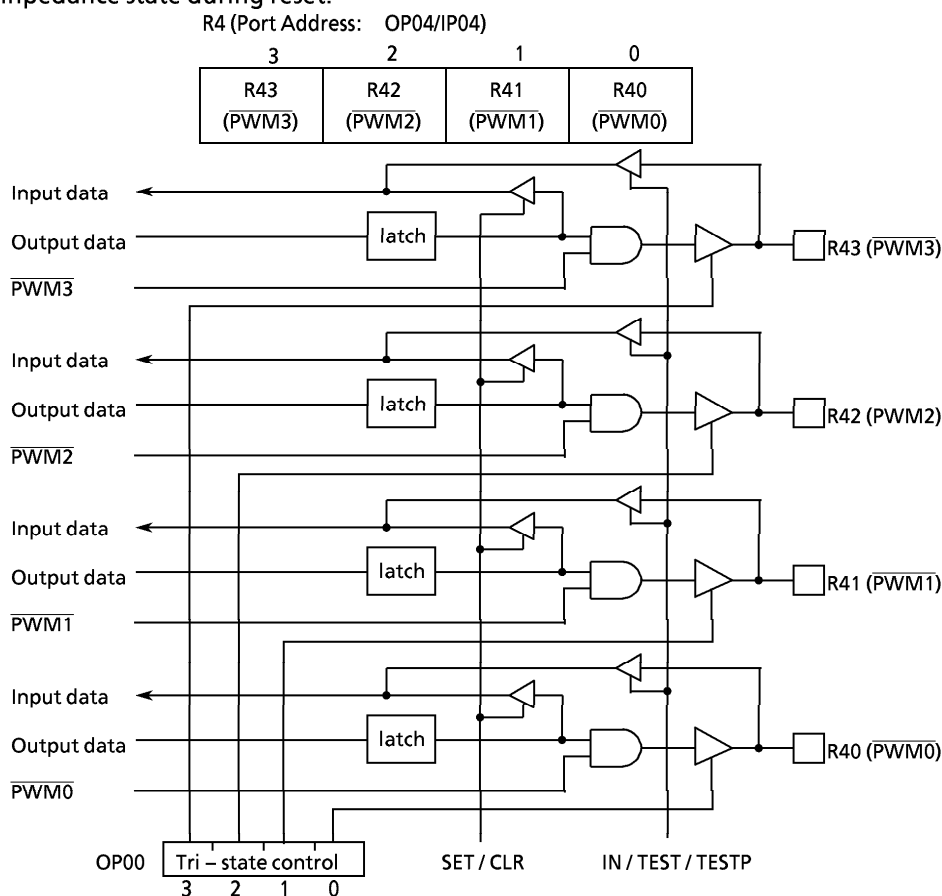Figure 3-1.　Port R4 ($\overline{PWM}$)

(2) Port R5 (R53 to R50)

The 4-bit I/O port with latch. The only R50 pin share DA converter (PWM) output. The port output buffers are tri-state, and each bit of them can be controled independently by the program. Controling the tri-state is performed by the command register accessed as port address OP13.

Example: LD   A,#1111$_B$;   OP13 ← 1111$_B$
          OUT   A,%OP13
          OUT   #05H,%OP05   ;   R5 port ← 5$_H$

R5 Port (Port Address: OP05 / IP05)

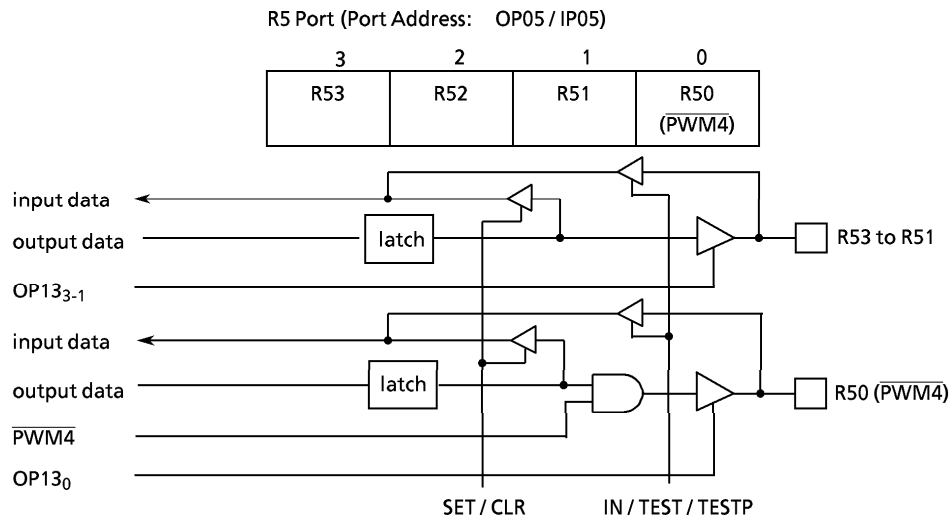| 3	2	1	0
R53	R52	R51	R50 (PWM4)

Figure 3-2. Port R5

(3) Port R7 (R73 to R70)

The 4-bit I/O port with latch. When used as an input port, the latch should be set to "1". The latch is initialized to "1" during reset. R72 pins is I/O port usually.

Pin R70 (CIN) is shared with the digital input usual and the AD converter (comparator) input for Auto Frequency Control signal detection. CIN input is comparator input and setting of 3-bit DIA convert for reference voltage are performed by the command register. R71 ($\overline{\text{WTO}}$), R73 ($\overline{\text{PULSE}}$) pins are shared with the watchdog timer output and pulse output. R70, R71, R73 pins latch is initialized to "1" during reset, and they are able to use I/O port usually.
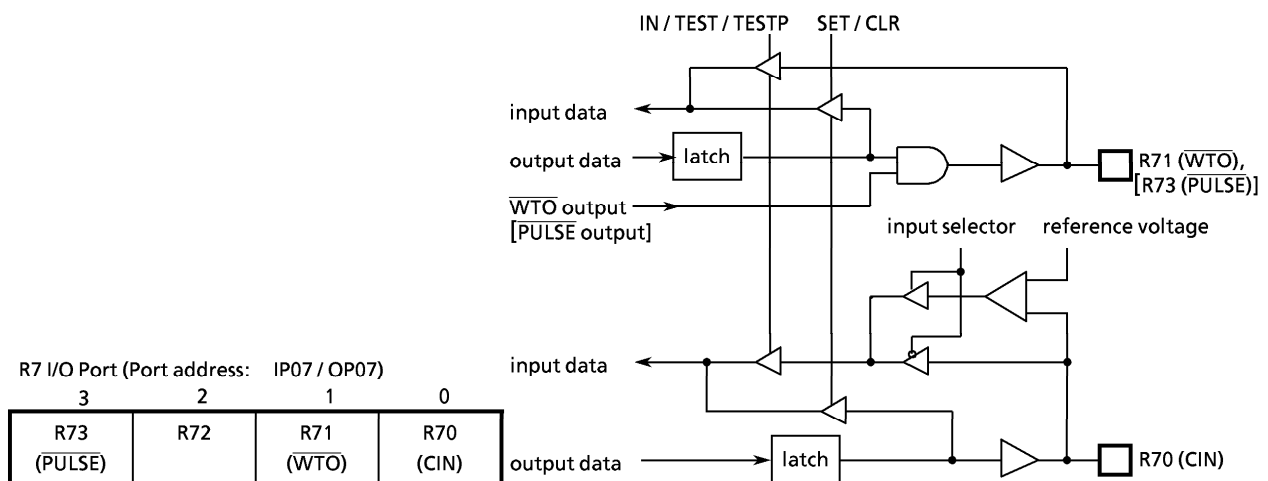

R7 I/O Port (Port address: IP07 / OP07)

3	2	1	0
R73 (PULSE)	R72	R71 ($\overline{\text{WTO}}$)	R70 (CIN)

Figure 3-3. Port R7

Table 3-1. Port address assignments and available I/O instructions

Port Address (**)	Input (IP**)	Output (OP**)	IN %p, A / IN %p, @HL	OUT A, %p / OUT @HL, %p	OUT #k, %p	OUTB@HL	SET %p, b / CLR %p, b	TEST %p, b / TESTP %p, b	SET @L / CLR @L / TEST @L
00H	K0 input port	Tri-state(R4 port)control	○	○	○	—	—	○	—
01	——	——	—	—	—	—	—	—	—
02	——	——	—	—	—	—	—	—	—
03	——	——	—	—	—	—	—	—	—
04	R4 input port	R4 output port	○	○	○	—	○	○	○
05	R5 input port	R5 output port	○	○	○	—	○	○	○
06	R6 input port	R6 output port	○	○	○	—	○	○	○
07	R7 input port	R7 output port	○	○	○	—	○	○	○
08	R8 input port	R8 output port	○	○	○	—	○	○	—
09	R9 input port	R9 output port	○	○	○	—	○	○	—
0A	RA input port	RA output port	○	○	○	—	○	○	—
0B	——	——	—	—	—	—	—	—	—
0C		OSD command selector	—	○	○	—	—	—	—
0D	Remote control count value register	Remote control offset value register	○	○	○	—	—	—	—
0E	status input (Note 2)	Remote control single preprocess circuit control	○	○	○	—	—	○	—
0F	Serial receive buffer	Serial transmit buffer	○	○	○	—	—	—	—
10H	undefined	Hold operation mode	—	○	—	—	—	—	—
11	undefined	——	—	—	—	—	—	—	—
12	undefined	AD converter input control	—	○	—	—	—	—	—
13	undefined	Tri-state (R5 port) control	—	○	—	—	—	—	—
14	undefined	——	—	—	—	—	—	—	—
15	undefined	Watchdog timer control	—	○	—	—	—	—	—
16	undefined	——	—	—	—	—	—	—	—
17	undefined	PWM buffer selector	—	○	—	—	—	—	—
18	undefined	PWM data transfer buffer	—	○	—	—	—	—	—
19	undefined	Interval timer interrupt control	—	○	—	—	—	—	—
1A	undefined	OSD control	—	○	—	—	—	—	—
1B	undefined	——	—	—	—	—	—	—	—
1C	undefined	Timer/counter 1 control	—	○	—	—	—	—	—
1D	undefined	Timer/counter 2 control	—	○	—	—	—	—	—
1E	undefined	SIO control 1	—	○	—	—	—	—	—
1F	undefined	SIO control 2	—	○	—	—	—	—	—

Note 1: "——" means the reserved state. Unavailable for the user programs.
Note 2: the status input of serial interface, clock generator, and HOLD (KE0) pin.

3.2   On-screen display (OSD) circuit

An on-screen display (OSD) circuit used to display characters and symbols in built into the TV screen.
A maximum of 32 characters, as 16 columns × 2 lines, out of 62 character patterns can be displayed at a time.

3.2.1   OSD circuit function

①	Number of characters	62 kinds
②	Number of characters displayed	32 characters (16 columns × 2 lines)
③	Composition of a character	8 × 8 dots (with smoothing function)
④	Size of character	2 kinds (selectable line by line)
⑤	Color of character	7 kinds (selectable character by character)
⑥	Display position variable	horizontal 64 steps, vertical 64 steps
⑦	Double Scan mode switching function	

3.2.2 OSD circuit configuration

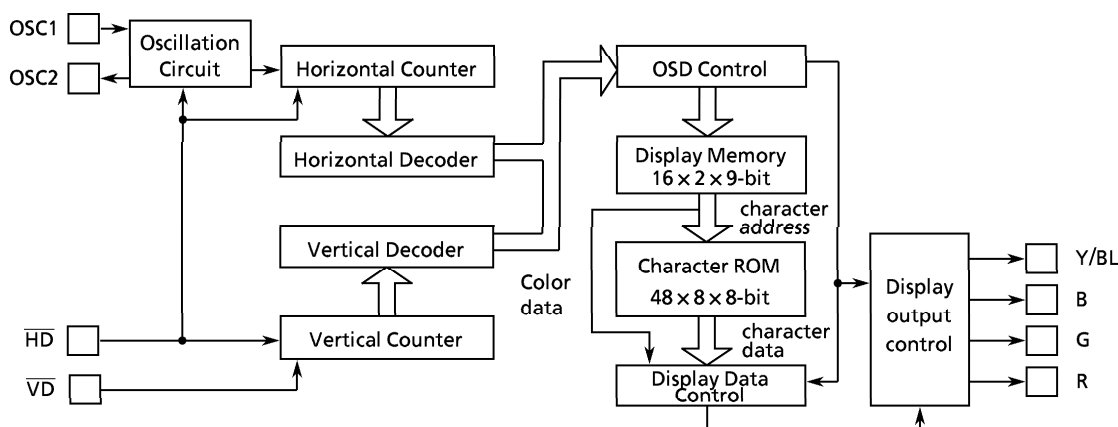
Figure 3-4.   OSD circuit

3.2.3 OSD circuit control

The OSD circuit is controlled by the command selector (OP0C) and control register (OP1A). Table 3-2 shows the relationship between OP0C and OP1A. OP1A is multiplexed with the six output control registers which control the display start position, color of character and character size of character, and the two transfer control registers which transter character data to the display memory.

The output control registers consist of 8 bits and all bits can be written by accessing OP1A two times. However, the second access is not required unless the second data are changed. The addressed "0 to 5" are assigned to the six output control registers. OP1A can be accessed by writing the address of the control register where data are to be changed to OP0C. The transfer control registers can be accessed by writing "6" or "7" to OP0C. The transfer control registers have a 12-bit configuration and can access OP1A three times succession. The first access sets which column is displayed within one line 16 columns. The second and third accesses written 6 bit of character data.

The display memory has a 16-columns × 9-bit × 2 lines configuration with a one-to-one correspondence to the number of columns displayed on the screen. The display data consist of 6 character data bits and 3 color data bits for a total of 9 bits. When "6" is written to OP0C, line 1 is stored to the display memory, when "7" is written to OP0C, line 2 is stored. That is after accessing OP0C, the character data specified the second and third times are written to the display memory area specified in the first OP1A access together with the color data loaded to control register DCR50. Thus color can be specified for each character. After setting of all control registers is completed, the character data read from the character ROM(00 to $2F_H$)are output to the R, G and B pins together with the color data by setting OP0C to "F".

Note: The writing a data from display memeory is prior than the reading. Therefore, if a data is written to the display memory until the display line is displaying, the display is incorrect.

A data must be written to display memeory when the display is off or when one and two display line are not displayed.

Table 3-2. OSD control commands and control registers

OSD command selector (OP0C)	OSD control register to be accessed through OP1A					
0	Control for the horizontal start position of the first display line					
		3	2	1	0	
	DCR00	–	–	HS15	HS14	(1st access)
	DCR01	HS13	HS12	HS11	HS10	(2st access)
1	Control for the vertical start position of the first display line					
		3	2	1	0	
	DCR10	–	–	VS15	VS14	(1st access)
	DCR11	VS13	VS12	VS11	VS10	(2st access)
2	Control for the horizontal start position of the second display line.					
		3	2	1	0	
	DCR20	–	–	HS25	HS24	(1st access)
	DCR21	HS23	HS22	HS21	HS20	(2st access)
3	Control for the vertical start position of the second display line.					
		3	2	1	0	
	DCR30	–	–	VS25	VS24	(1st access)
	DCR31	VS23	VS22	VS21	VS20	(2st access)
4	Control for the character sizes,smoothing switch and OSD output polarities					
		3	2	1	0	
	DCR40	CS21	CS20	CS11	CS10	(1st access)
	DCR41	ESMZ	BLIV	YIV	RGBIV	(2st access)
5	Control for the color register and OSD output buffers'tri-state'					
		3	2	1	0	
	DCR50	–	RDT	GDT	BDT	(1st access)
	DCR51	EBF3	EBF2	EBF1	EBF0	(2st access)
6	display memory write mode for the first display line(address 00 to 0F)					
		3	2	1	0	
		DMA3	DMA2	DMA1	DMA0	(1st access)
		–	–	CRA5	CRA4	(2st access)
		CRA3	CRA2	CRA1	CRA0	(3st access)
7	display memory write mode for the second display line(address 10 to 1F)					
		3	2	1	0	
		DMA3	DMA2	DMA1	DMA0	(1st access)
		–	–	CRA5	CRA4	(2st access)
		CRA3	CRA2	CRA1	CRA0	(3st access)
E	display OFF					
F	display ON					

3.2.4 Configuration of display character

(1) Composition of character and smoothing function
Each character is compsited by 8×8 dots. Each dot corresponds to a bit in the character ROM. Figure 3-5. (a) shows an example Composition of a character.
Smoothing function is the function to make characters look smooth. In the time the smoothing function is enabled, additional dots are displayed in the middle of the place where two dots contact each other only at a corner. Controlling of the smoothing function is performed by ESMZ in the OSD control register DCR41. Figure 3-5. (b) shows an example of the smoothing function.

(a) without smoothing   (b) with smoothing
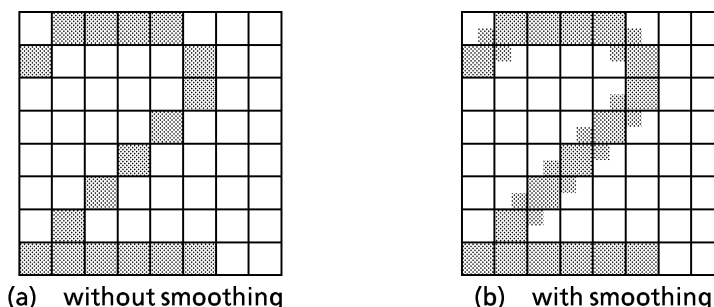
Figure 3-5. Composition of character and smoothing function

(2) Character size and color to display
Size of the characters displayed on screen is selectable line by line from 2 sizes. The size of the first and second display line is disignated by CS11 to CS10 and CS21 to CS20 in the OSD control register DCR40,respectively.
Table 3-3 shows the setting values and character sizes of DCR40.
Table 3-4 shows the display character sizes.
One out of seven colors can be selected for each character to be displayed and are determined by RDT,GDT,and BDT of DCR50. The color data are written to the display memory automatically at the same time as character data are written

Table 3-3. Designation of character size

Character size (DCR40)	second display line		first display line	
	CS21	CS20	CS11	CS10
small character	1	0	1	0
large character	0	1	0	1
display OFF	0	0	0	0

Table 3-4. Character size.

	small character	large character
dot size	$2T_{HD} \times 2T_{OSC}$	$4T_{HD} \times 4T_{OSC}$
character size	$16T_{HD} \times 16T_{OSC}$	$32T_{HD} \times 32T_{OSC}$

Note: T_{HD}:the period of horizontal synchrorous signal
T_{OSC}:the period of OSD clock oscillation

Table 3-5. Select of color to display

colors displayed on screen	color data(DCR50)		
	RDT	GDT	BDT
Blank	0	0	0
Blue	0	0	1
Green	0	1	0
Sian	0	1	1
Red	1	0	0
Mazenda	1	0	1
Yellow	1	1	0
White	1	1	1

Note: Color to display: RGB pin uses Red, Green, Blue such as.

3.2.5 Display start position

Display start position of each display line on screen can be shifted by software.
The vertical and horizontal display starting position for the first line is determined by HS10 to 15 and VS10 to 15 of DCR00 to 11.
The vertical and horizontal display starting position for the second line is determined by HS20 to25 and VS20 to 25 of DCR20 to 31. Each has a resolution of 64 steps.
The control register and display line on screen are shown in Table 3-6.
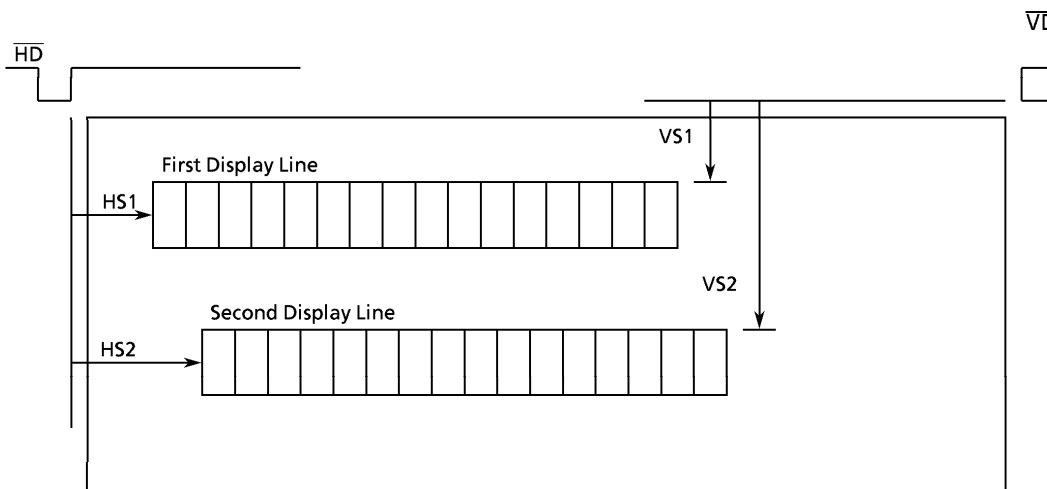
Figure 3-6. TV screen image

Table 3-6. Display start position

Symbol	Contents
HS10 to HS15	horizontal start position of the first display line $HS1 = ((32 \times HS15 + 16 \times HS14 + 8 \times HS13 + 4 \times HS12 + 2 \times HS11 + HS10) \times 4 + X) T_{OSC}$
VS10 to VS15	vertical start position of the first display line $VS1 = (32 \times VS15 + 16 \times VS14 + 8 \times VS13 + 4 \times VS12 + 2 \times VS11 + VS10) \times 4 T_{HD}$
HS20 to HS25	horizontal start position of the second display line $HS2 = ((32 \times HS25 + 16 \times HS24 + 8 \times HS23 + 4 \times HS22 + 2 \times HS21 + HS20) \times 4 + X) T_{OSC}$
VS20 to VS25	vertical start position of the second display line $VS2 = (32 \times VS25 + 16 \times VS24 + 8 \times VS23 + 4 \times VS22 + 2 \times VS21 + VS20) \times 4 T_{HD}$

Note: X; X is 17 when small character.
X is 34 when large character.

* The vertical display positions of lines 1 and 2 can be specified independently but,to prevent overlapping of the two lines on the display, the value for the vertical display position of line 2 must satisfy 〔 $VS2 > VS1 + CS11 \times 16T_{HD} + CS10 \times 32T_{HD}$ 〕.

3.2.4 Y/BL signal

The Y signal (the logical or output of the R, G and B signals) makes the display clearer by deleting the background only where characters are displayed. The BL signal deletes the entire background for one character (8 × 8 dots) and is output for all data except that at address $2F_H$ in the character ROM.

The Y/BL pin is used for both Y signal and BL signal output. Which of the two signals is to be output is determined by the upper 2 bits of OP0A. The dotted lines in Figure 3-7 show the Y/BL signal output being scanned.
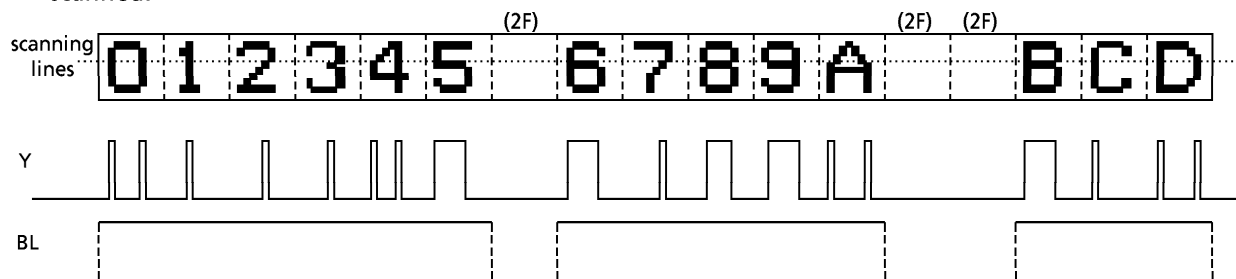
Figure 3-7. Example of Y and BL signal output

3.2.5 Control of OSD outputs buffer

The OSD outputs for Y,BL and RGB use tri-state output buffers for which the respective polarities can be inverted. Polarity is controlled by DRC41 and tri-state is controlled by DRC51.
Bit 3 of DRC41 is used for controlling the smoothing function.

Table 3-7. Control of OSD output

register	bit	symbol	output name	data "0"	data "1"
DRC41	3	ESMZ	‾‾	smoozing OFF	smoozing ON
	2	BLIV	BL	active High	active Low
	1	YIV	Y	active High	active Low
	0	RGBIV	RGB	active High	active Low
DRC51	3	EBF3	Y / BL	output buffer OFF	output buffer ON
	2	EBF2	B	output buffer OFF	output buffer ON
	1	EBF1	G	output buffer OFF	output buffer ON
	0	EBF0	R	output buffer OFF	output buffer ON

3.2.6 RA Port function

R signal output and G signal output ports are also used as I/O ports. When not used for color signals,use is possible as normal I/O ports. RA port and Y/BL selection is performed by OP0A.
Also,the upper 2 bits of IP0A are used to input the OSD display status.

Port address: OP0A

OP0A3	OP0A2	OP0A1	OP0A0

→ RA0 output

→ RA1 output

control of OSD output and RA port

OP0A3	OP0A2	output pin No.			
		22	23	24	25
0	0	R	G	B	Y
0	1	R	G	B	B L
1	0	RA0	G	B	Y
1	1	RA0	RA1	B	B L

Port address: IP0A

V02	V01	IP0A1	IP0A0

→ RA0 input

→ RA1 input

0: first display line display ON
1: first display line display OFF

0: second display line display ON
1: second display line display OFF

Figure 3-8. Port RA

3.2.7 Character ROM

The TMP47C834 can display 62 different 8 × 8 dot characters (character ROM addresses 00$_H$ - 3D$_H$). Address 2F$_H$ in the character ROM displays a blank, as with the TMP47C434/634, so set all ROM data to "0".

The first 48 characters of the TMP47C834 character ROM are the same as those of the TMP47C434A/634A; therefore, TMP47C434A/634A programs can be used without change.

Address
```
00_H ┌──────────────┐
  ⋮  │              │
 2D  │              │
 2E  ├──────────────┤
     │  Background  │
 2F  ├──────────────┤
     │  Blank data  │
     └──────────────┘
```
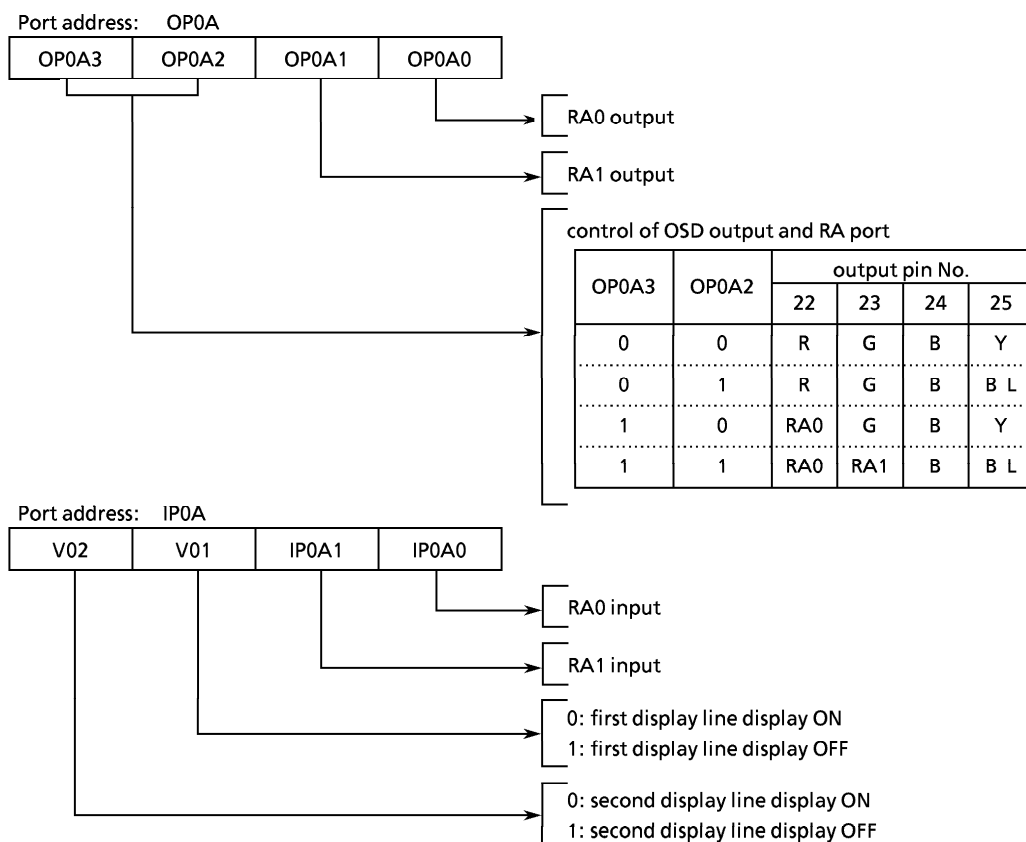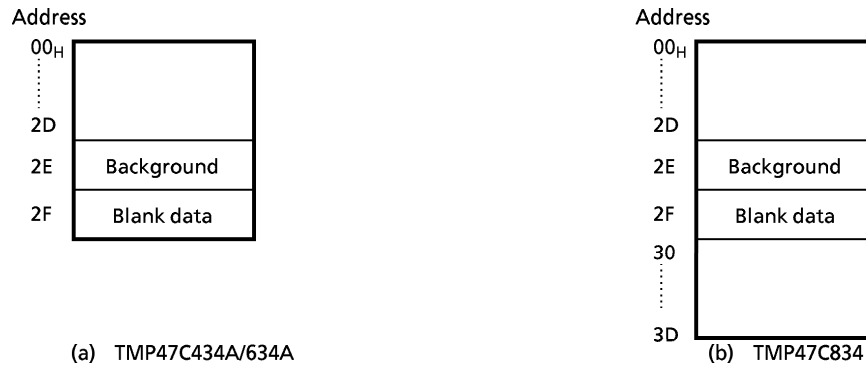(a) TMP47C434A/634A

Address
```
00_H ┌──────────────┐
  ⋮  │              │
 2D  │              │
 2E  ├──────────────┤
     │  Background  │
 2F  ├──────────────┤
     │  Blank data  │
 30  ├──────────────┤
  ⋮  │              │
 3D  └──────────────┘
```
(b) TMP47C834

Figure 3-9. Character ROM configuration

Note: *Addresses 3EH and 3FH the character ROM are used in out going test.*
Data can be not specified by users.

3.2.8 Double scan mode switching function

The TMP47C834 has an Double scan mode switching function for selecting the interlace mode or the double scan (non-interlace) mode.

When the double scan mode is used, the number of scan lines on the screen is double that of the interlace mode; therefore, the $\overline{HD}$ signal is single-stage divided so that the vertical display start position and character size will be the same as with the interlace mode.

In the double scan mode, the horizontal scan line cycle is one-half that of the interlace mode; therefore, it is necessary to increase the OSD oscillation frequency.

(a) Interlace mode
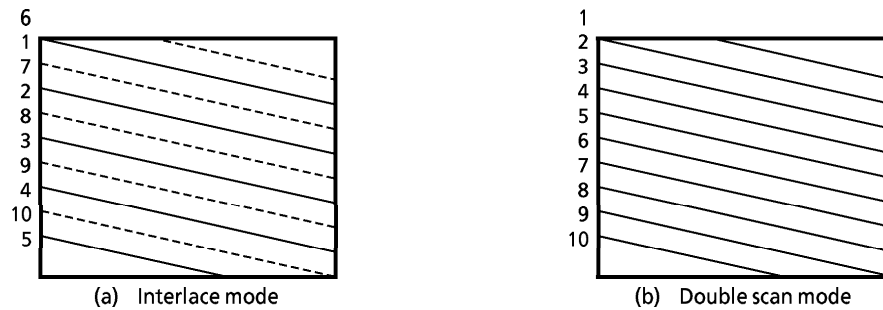
(b) Double scan mode

Figure 3-10. Double scan mode

3.2.9 Double scan mode control

Double scan mode switching is controlled by WHD of the command register OP0B. Setting WHD to "0" selects the double scan mode and setting WHD to "1" selects the interlace mode. The initial setting selects the interlace mode.

Double Scan Mode Control
(Port address: OP0B   Initial value: 11*1)

WHD	Double Scan mode
0:	Double scan mode
1:	Interlace mode
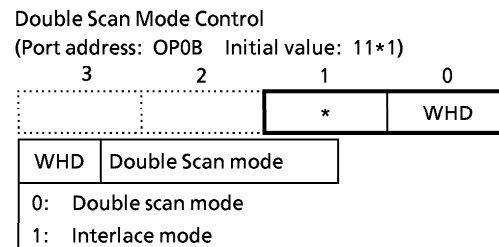
Figure 3-11. Double scan mode command register

3.3   3-bit AD converter (Comparator) input

Comparator input consists of a comparator and a 3-bit DA comvertor. AFC input voltage can be detected in 8 steps by sensing bit 0 of IP07 while cahnging the reference voltage (DA convertor output voltage) with the command register (OP12).

R70 pin is also used for comparator input. Bit 3 is used to set R70 pin for ordinary digital input.

The comparator is disabled and bit 3 is set to "0" during reset. The latch should be set to "1" when R70 pin is used for comparator input and digital input.

3.3.1 Circuit configuration

The comparator input circuit shown in figure 3-12.
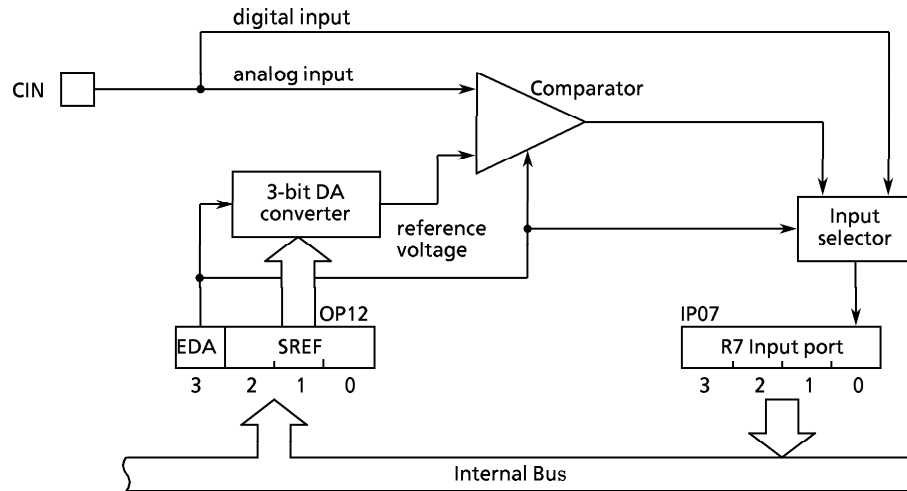
Figure 3-12.   Comparator input circuit

3.3.2 Control of comparator input

The reference voltage of the comparator is set using the lower 3 bits of the command register. Table 3-8 shows the reference voltage when $V_{DD} = 5$ V.

Comparator input control command registor (Port address: OP12)
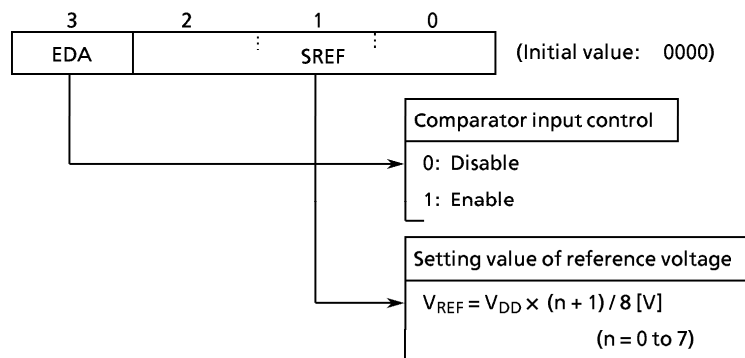
Figure 3-13.   Control command registor

Table 3-8.   Reference voltage

OP12			Reference voltage [V]
2	1	0	
0	0	0	0.62
0	0	1	1.25
0	1	0	1.87
0	1	1	2.50
1	0	0	3.12
1	0	1	3.75
1	1	0	4.37
1	1	1	5.00

3.4 DA converter (PWM) output

The TMP47C434A/634A have five channels built-in DA converter (Pulse width Modulation) outputs. $\overline{PWM}$ output can easily be obtained by connecting an external low pass filter.

$\overline{PWM}$ outputs data are multiplex to the R4 port and R50 pin. When the R4 ($\overline{PWM}$) port and R50 pin are used for $\overline{PWM}$ output, the corresponding bits of R4, R50 output latch should be set to "1". The R4, R5 output latch is initialized to "1" during reset.

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). PWM data written to the data transfer buffer can be sent to the PWM data latch by writing "C_H" to the buffer selector, and $\overline{PWM}$ output $\overline{PWM}$ output. PWM data transferred to the PWM data latch remain intact until overwritten. Resetting and holding clear the buffer selector, data transfer buffer and PWM data latch to "0" ($\overline{PWM}$ output is "H" level).

3.4.1 Configuration of pulse width modulation circuit

Configuration of pulse width modulation circuit shown in Figure 3-15.

3.4.2 Output waveform of PWM circuit

(1) $\overline{PWM0}$ output

$\overline{PWM0}$ is a PWM output controlled by 14 bits data. The basic period of the $\overline{PWM0}$ is $T_M = 2^{15}/fc$.

The higher 8 bits of 14 bits data are used to control the pulse width of the pulse output with the period of $T_S = T_M/64$, which is the sub - period of the $\overline{PWM0}$. When the 8 bits data are decimal n ($0 \leq n \leq 255$), this pulse width becomes $n \times t_0$, where $t_0 = 2/fc$.

The lower 6 bits of 14 bits data are used to control the generation of an additional t_0 wide pulse in each T_S period. When the 6 bits data are decimal m ($0 \leq m \leq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a T_M period. The relationship between the 6 bits data and the position of T_S period where the additional pulse is generated is shown in Table 3-9. (The additional pulse is not generated on $T_{S(0)}$).

(2) $\overline{PWM1}$ to $\overline{PWM4}$ output

Each of $\overline{PWM1}$ to $\overline{PWM4}$ is a PWM output controlled by 6 bits data. The period of them is $T_M = 2^7/fc$. When the 6 bits data are decimal k ($0 < k < 63$), the pulse width becomes $k \times t_0$. The waveform is also illustrated in Figure 3-14.
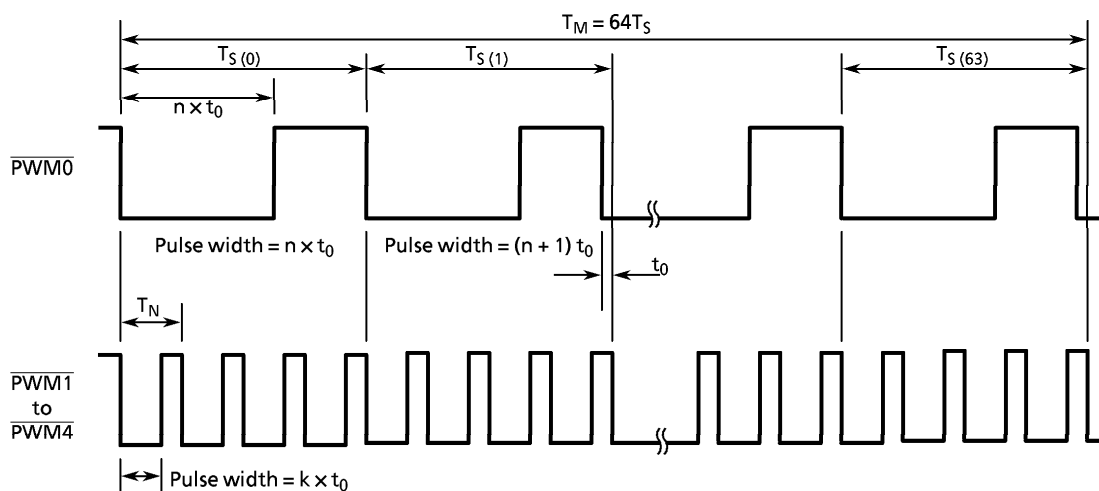

Figure 3-14. $\overline{PWM}$ output waveform (It is shown to the additional pulse $T_{S(1)}$ and $T_{S(63)}$ of the $\overline{PWM0}$)
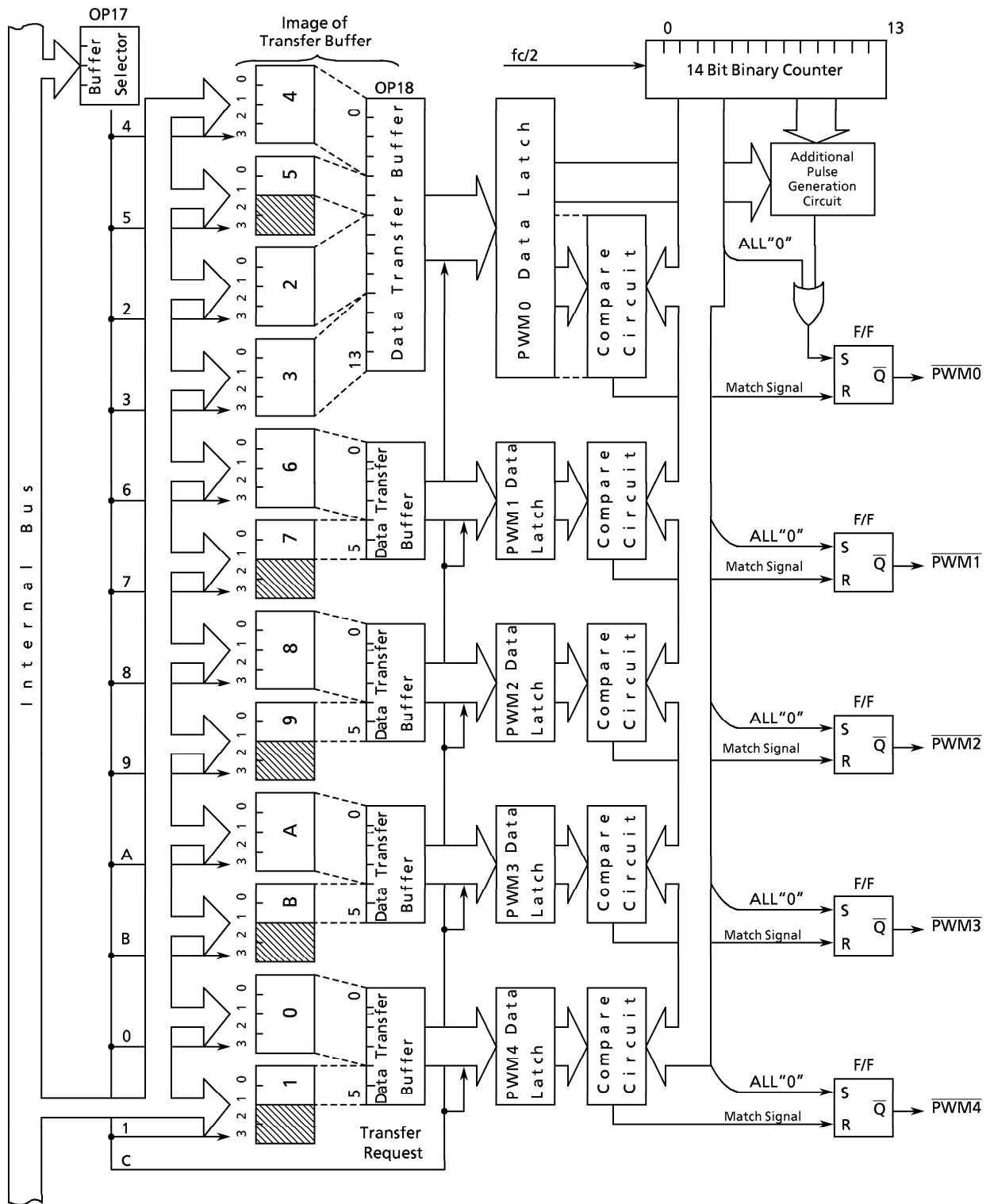
Figure 3-15. Pulse width modulation circuit

Table 3-9. Correspondence between 6 bits data and the additional pulse generated T_S periods

Bit position of 6 vits data	Relative position of T_S where the output pulse is generated (No. i of $T_{S(i)}$ is listed)
bit0	32
bit1	16, 48
bit2	8, 24, 40, 56
bit3	4, 12, 20, 28, 36, 44, 52, 60
bit4	2, 6, 10, 14, 18, 22, 26, 30, ·····, 58, 62
bit5	1, 3, 5, 7, 9, 11, 13, 15, 17, ·····, 59, 61, 63

Note: When the corresponding bit is "1", it is output.

3.4.3 Control of PWM circuit (Data transfer)

$\overline{PWM}$ output is controlled by writing output data to a data transfer buffer (OP18). For writing, the output data are divided using the buffer selector (OP17). Buffer numbers are assigned to the data transfer buffers for these divided data, after which the data are written as shown in Table 3-10.

    ① The number of the transfer buffer to which the data are to be written is written to the buffer selector (OP17).

    ② The corresponding PWM data are written to the selected buffer (OP18).

    ③ Operations ① and ② are repeated, continuously writing data to the transfer buffer.

    ④ When all of the output data have been written. "C_H" is written to the buffer selector.

While the output data are being writen to the transfer buffer, the previously written data are being output. For $\overline{PWM0}$ output, switching to $\overline{PWM}$ output occurs at a maximum of $2^{15}/fc$ [s] (at 4 MHz, 8192fs) after "C_H" is written to the buffer selector. For $\overline{PWM1}$ through $\overline{PWM4}$ output data switching, this requires $2^9/fc$ [s] (at 4 MHz, 128 μs).

Table 3-10. The bit and Buffer number of data transfer Buffer

Buffer Number (OP17)	Correspondence to bit (OP18)		Mode	PWM Output
0	Bit of PWM4 transfer buffer	3 to 0	Write	Preceding data
1	Bit of PWM4 transfer buffer	5 to 4	Write	Preceding data
2	Bit of PWM0 transfer buffer	9 to 6	Write	Preceding data
3	Bit of PWM0 transfer buffer	13 to 10	Write	Preceding data
4	Bit of PWM0 transfer buffer	3 to 0	Write	Preceding data
5	Bit of PWM0 transfer buffer	5 to 4	Write	Preceding data
6	Bit of PWM1 transfer buffer	3 to 0	Write	Preceding data
7	Bit of PWM1 transfer buffer	5 to 4	Write	Preceding data
8	Bit of PWM2 transfer buffer	3 to 0	Write	Preceding data
9	Bit of PWM2 transfer buffer	5 to 4	Write	Preceding data
A	Bit of PWM3 transfer buffer	3 to 0	Write	Preceding data
B	Bit of PWM3 transfer buffer	5 to 4	Write	Preceding data
C	None		Transfer	Present data

3.5 Pulse output circuit

Pulse output circuit generates the pulse clock by dividing the clock frequency to R73 port. The pulse output is used for the basic clock for the PLL IC or peripheral ICs. The pulse output frequency can be set by accessing command register (OP0B). Command register is initialized to "11**" during reset. When R73 port is used as the pulse output, set R73 output latch to "1".
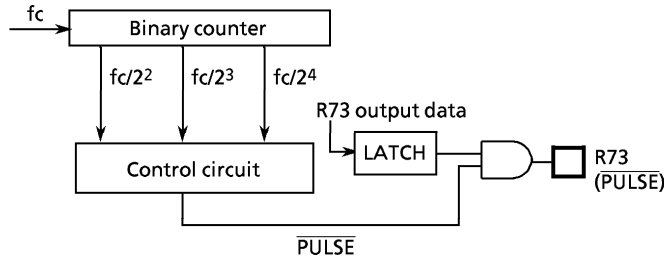
Figure 3-16. Pulse output circuit

Pulse Output Control Command Register
(Port address: OP0B)

SPF	Select pulse frequency
	at fc = 4 MHz
00:	Output pulse of $fc/2^4$ [Hz] ... 250 kHz
01:	Output pulse of $fc/2^3$ [Hz] ... 500 kHz
10:	Output pulse of $fc/2^2$ [Hz] .... 1 MHz
11:	Disable the pulse output
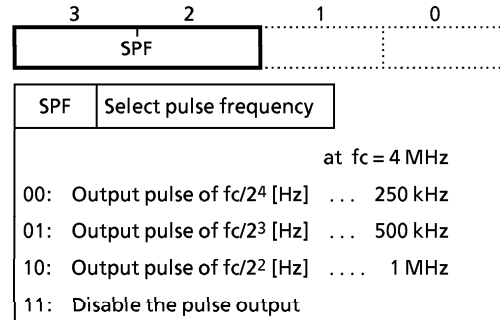
Figure 3-17. Pulse output command register

Notice of ROM code release for masked products

When releasing ROM code for mask products, please take notice as follows,

(1) The area of program and program / fixed data
- Fill the data "FF_H" at all addresses of unused area.

(2) The area of character data
- Load the character data at the address 2000_H to $21EF_H$.
- Fill the data "FF_H" at all addresses of unused characters.

Address

0000_H

Program

Program /
Fixed data

$1FFF_H$
2000_H

Character data

$21EF_H$

TMP47C834
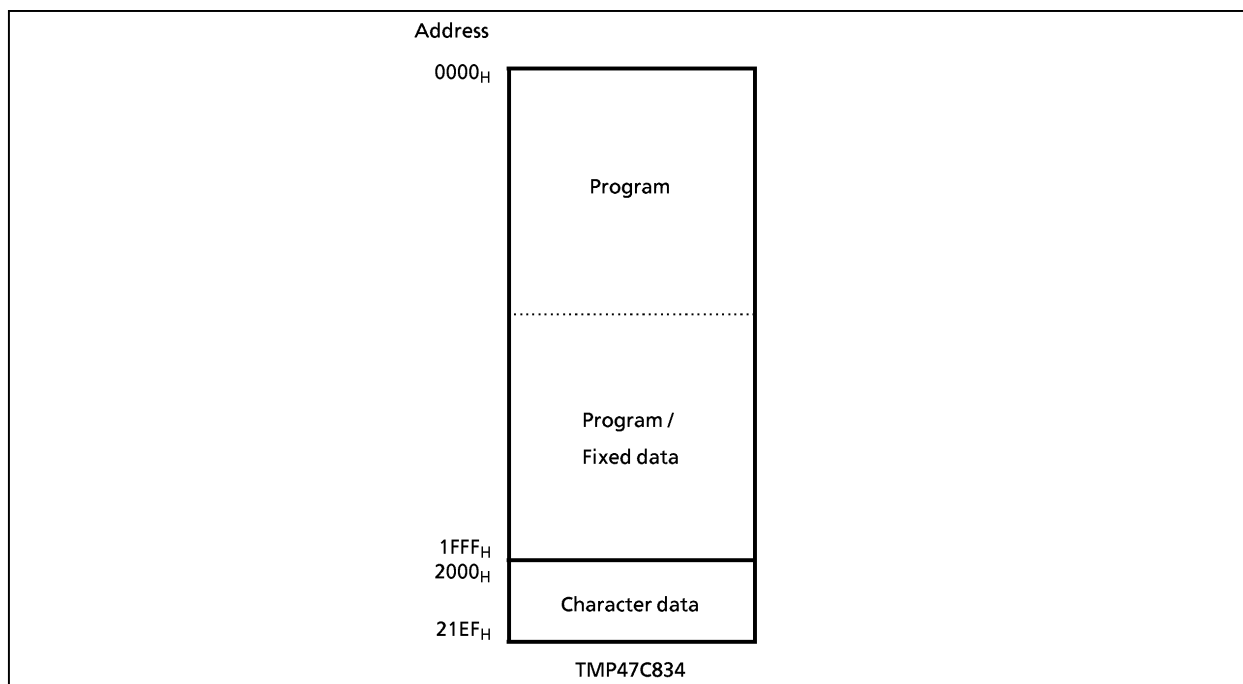
Port Condition by RESET Operation

The transition of Port condition by RESET operation is shown as below.
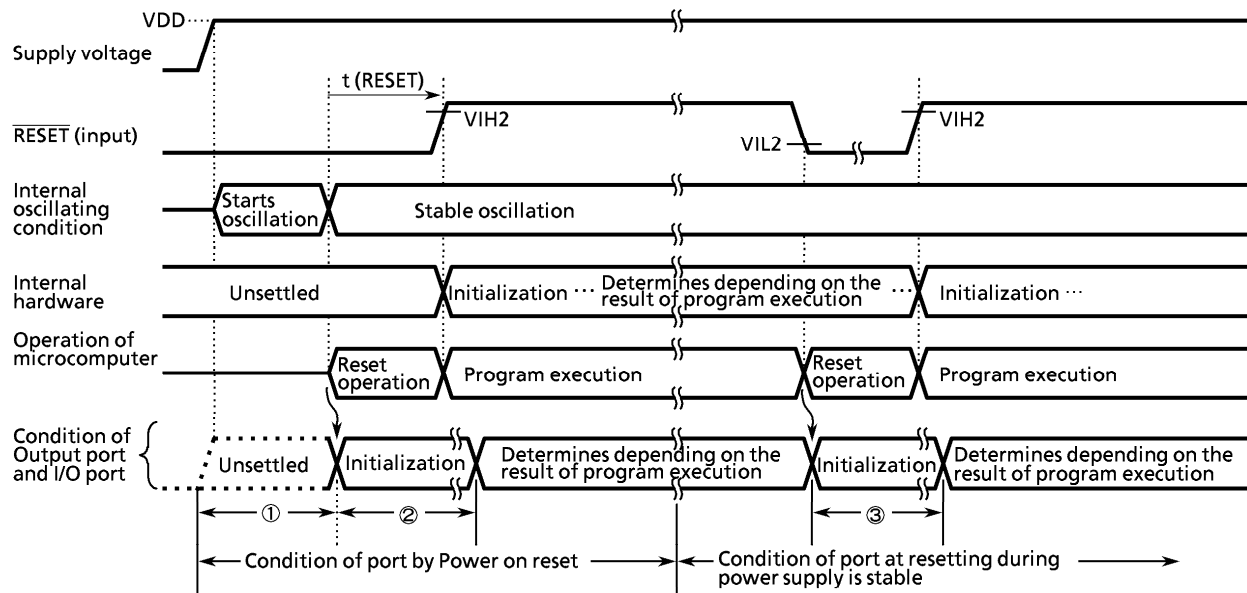
Figure 3-18. Port condition by Reset operation

Note 1: $t (RESET) > 24/fc$

Note 2: *VIL2:* *Stands for low level input voltage of* $\overline{RESET}$ *pin.*

VIH2: *Stands for high level input voltage of* $\overline{RESET}$ *pin.*

Note 3: *The condition of each port is unstable until the reset operation is started (① in the above Figure). Thus, when using port as an output pin, in the term of ①, to prevent the malfunction of external application circuit, insert the circuit outside of microcomputer between the output pin of Port and input pin of external application circuit.*

Note 4: *The term starting from reset operation to the program which accesses port is executed (②, ③ in the above Figure), the condition of port becomes on the status of initialization by Reset operation. The initial condition of port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ② and ③, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and/or pull-down resistor.*

Input / Output Circuitry

(1) Control Pins
Input / output circuitries of the TMP47C834 control pins are shown below.

Control Pin	I/O	Circuitry	Remarks
XIN XOUT	Input Output		Resonator connecting pins $R = 1\,k\Omega$ (typ.) $R_f = 1.5\,M\Omega$ (typ.) $R_O = 2\,k\Omega$ (typ.)
$\overline{\text{RESET}}$	Input		Hysteresis input Contained pull-up resistor $R_{IN} = 220\,k\Omega$ (typ.) $R = 1\,k\Omega$ (typ.)
$\overline{\text{HOLD}}$ (KE0)	Input (Input)		Hysteresis input (Sense input) $R = 1\,k\Omega$ (typ.)
TEST	Input		Contained pull-down resistor $R_{IN} = 70\,k\Omega$ (typ.) $R = 1\,k\Omega$ (typ.)
OSC1 OSC2	Input Output		Oscillation terminals for OSD $R = 1\,k\Omega$ (typ.) $R_f = 1.5\,M\Omega$ (typ.) $R_0 = 2\,k\Omega$ (typ.)
$\overline{\text{HD}}$ $\overline{\text{VD}}$	Input		Synchronous signal input Hysteresis input $R = 1\,k\Omega$ (typ.)

(2)   I/O Ports
The input / output circuitries of the TMP47C834 I/O ports are shown below, any one of the circuitries (PB, PC, PF, PU) can be chosen by a code as a mask option.

Port	I/O	Input / Output Circuitry and Code		Remarks
K0	Input	**PB** — VDD, R_{IN}, R	**PC, PF, PU** — R, R_{IN}	Pull-up or pull-down resistor $R_{IN} = 70\ k\Omega$ (typ.) $R = 1\ k\Omega$ (typ.)
R4 R50	I/O	**PB, PC** — VDD, DISABLE, R	**PF, PU** — R	Tri-state or Sink open drain Initial "Hi-Z" $R = 1\ k\Omega$ (typ.)
R51 R52 R53	I/O	VDD, DISABLE, R		Tri-state Initial "Hi-Z" $R = 1\ k\Omega$ (typ.)
R6 R8 R9	I/O	**R6** — R	**R8, R9** — R	Sink open drain Initial "Hi-Z" Hysteresis input (R8, R9) $R = 1\ k\Omega$ (typ.)
R7	I/O	**R70** Initial "Hi-Z" — R, $+$, V_{REF}	**R71~R73** Initial "High" — VDD, R	Sink open drain and push-pull Comparator input (R70 pin) $R = 1\ k\Omega$ (typ.)
R (RA0) G (RA1)	I/O	**PB, PC, PF** — VDD, DISABLE, OSD status, R, b, a	**PU** — OSD status, R, b, a	Tri-state Initial "Hi-Z" $R = 1\ k\Omega$ (typ.) R, G: Side a B, Y: Side b
B Y (BL)	Output			

Electrical Characteristics

| Absolute Maximum Ratings | (V_{SS} = 0 V) |

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7 port	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	R6 port	30	mA
	I_{OUT2}	R7, R8, R9 port	3.2	
Output Current (Total)	$\Sigma\ I_{OUT1}$	R6 port	60	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

| Recommended Opeating Conditions | (V_{SS} = 0 V, Topr = – 30 to 70°C) |

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz
	f_{OSD}			–	6.0	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage V_{IH3}, V_{IL3}: In the SLOW or HOLD mode.

DC Characteristics $(V_{SS} = 0\ V,\ Topr = -30\ to\ 70°C)$

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	K0 port, TEST, $\overline{RESET}$, $\overline{HOLD}$	$V_{DD} = 5.5\ V$, $V_{IN} = 5.5\ V / 0\ V$	—	—	± 2	μA
	I_{IN2}	R port (open drain)					
Input Resistance	R_{IN1}	K0 port with pull-up / pull-down		30	70	150	$k\Omega$
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output leakage Current	I_{LO}	Tri-state R6, R8, R9 port (open drain)	$V_{DD} = 5.5\ V, V_{OUT} = 5.5\ V$	—	—	± 2	μA
Output High Voltage	V_{OH2}	R port (tri-state), OSD output	$V_{DD} = 4.5\ V,\ I_{OH} = -0.7\ mA$	4.1	—	—	V
Output Low Voltage	V_{OL1}	R7, R8, R9 port	$V_{DD} = 4.5\ V,\ I_{OL} = 1.6\ mA$	—	—	0.4	V
	V_{OL2}	R port (tri-state), OSD output	$V_{DD} = 4.5\ V,\ I_{OL} = 0.7\ mA$				
Output Low Current	I_{OL}	R6 port	$V_{DD} = 4.5\ V,\ V_{OL} = 1.0\ V$	—	20	—	mA
Supply Current (in the Normal mode)	I_{DD}		$V_{DD} = 5.5\ V,\ fc = 4\ MHz$	—	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		$V_{DD} = 5.5\ V$	—	0.5	10	μA

Note 1: Typ. values show those at $Topr = 25°C, V_{DD} = 5\ V$.

Note 2: Input Current I_{IN1}: The current through resistor is not included, when the pull-up / pull-down resistor is contained.

Note 3: Supply Current: $V_{IN} = 5.3\ V / 0.2\ V$

The K0 port is open when the pull-up / pull-down resistor is contained.

The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

AD Converter Characteristics

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Analog Input Voltage	V_{AIN}	CIN		V_{SS}	–	V_{DD}	V
AD Conversion Error	–			–	–	$\pm \frac{1}{4}$	LSB

AC Characteristics	(V$_{SS}$ = 0 V, V$_{DD}$ = 4.5 to 6.0 V, Topr = − 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Instruction Cycle Time	tcy		1.9	–	20	μs
High level Clock Pulse Width	t$_{WCH}$	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t$_{WCL}$					
Shift data Hold Time	t$_{SDH}$		0.5 tcy – 0.3	–	–	μs

Note: Shift data Hold Time
External circuit for $\overline{SCK}$ pin and SO pin.

Serial port (Completion of transmission)
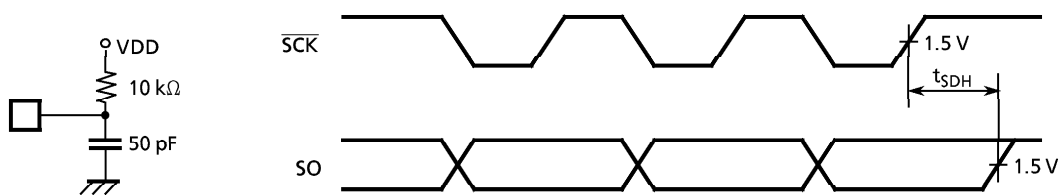
Recommended Oscillating Conditions	(V$_{SS}$ = 0 V, V$_{DD}$ = 4.5 to 6.0 V, Topr = − 30 to 70°C)

(1) 4 MHz
Ceramic Resonator
   CSA4.00MG   (MURATA)   C$_{XIN}$ = C$_{XOUT}$ = 30 pF
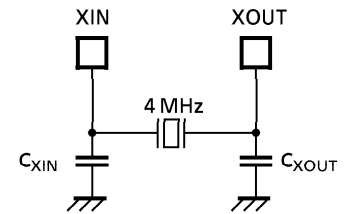   KBR-4.00MS   (KYOCERA)   C$_{XIN}$ = C$_{XOUT}$ = 30 pF
Crystal Oscillator
   204B-6F 4.0000   (TOYOCOM)   C$_{XIN}$ = C$_{XOUT}$ = 20 pF

(2) 400 kHz
Ceramic Resonator
   CSB400B   (MURATA)   C$_{XIN}$ = C$_{XOUT}$ = 220 pF,
                                    R$_{XOUT}$ = 6.8 kΩ
   KBR-400B   (KYOCERA)   C$_{XIN}$ = C$_{XOUT}$ = 100 pF,
                                    R$_{XOUT}$ = 10 kΩ
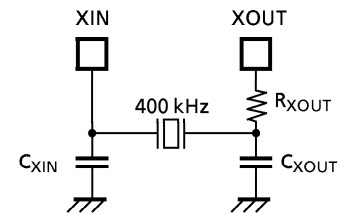
(3) 32.768 kHz   (VSS = 0 V,   VDD = 2.7 to 6.0V,
                                       Topr = − 30 to 70°C)
                      CXTIN, CXTOUT ; 10 to 33pF
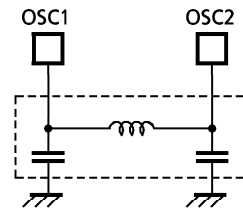
(4) 6 MHz (for OSD)
LC Resonator
   TBEKSES-30361FBY   (TOKO)

Note: An electrical shield by metal shield plate on the surface of the IC
package should be recommendable in order to prevent the device from
the high electric fieldstress applied from CRT (Cathode Ray Tube) for
continuous reliable operation.

Typical Characteristics

R – Ta   K0 port

R (kΩ)
$V_{DD} = 5.5$ V
100
50
0
−40   0   40   80   Ta (°C)

R – Ta $\overline{RESET}$ pin

R (kΩ)
$V_{DD} = 5.5$ V
400
300
200
100
0
−40   0   40   80   Ta (°C)

$I_{OH} – V_{OH}$ TRI-STATE port

I_{OH} (mA)
$V_{DD} = 4.5$ V
Ta = 25°C
−20
−15
−10
−5
0
2   4   6 V_{OH} (V)

$I_{OL} – V_{OL}$ P6 port

I_{OL} (mA)
$V_{DD} = 4.5$ V
Ta = 25°C
40
30
20
10
0
0.4   0.8   1.2 (V) V_{OL}

$I_{OL} – V_{OL}$ TRI-STATE port

I_{OL} (mA)
$V_{DD} = 4.5$ V
Ta = 25°C
8
6
4
2
0
0.4   0.8   1.2 (V) V_{OL}

$I_{DD} – V_{DD}$

I_{DD} (mA)
Ta = 25°C
4
3
2
1
0
fc = 4 MHz
fc = 1 MHz
3   5   7 (V) V_{DD}

$I_{DD} – fc$

I_{DD} (mA)
$V_{DD} = 5.5$ V
Ta = 25°C
4
3
2
1
0
0.1   0.4   1   4   10 (MHz)   fc

Operating area

fc (MHz)
Ta = −30 to 70°C
(Normal mode)
8
6
4
2
0
2   4   6 (V) V_{DD}

(: OTP / OSD operation)