BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1318AV

23 W AF POWER AMPLIFIER

DESCRIPTION

The μPC1318AV is an audio power amplifier in a 14-lead vertical dual in-line package, specifically designed for car stereo applications.

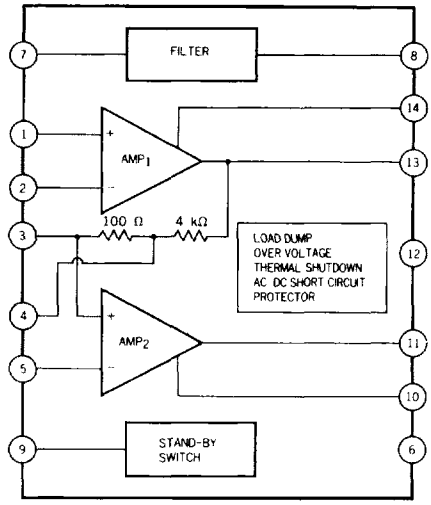
Typically it provides output power of 23 W at 14.4 V or 20 W at 13.2 V to a 4 Ω load.

This IC can be used without output capacitors, because its two output terminals have the same potential and it includes original short circuit protection function which protects internal output power transistors and a speaker at the same time when one output terminal is shorted to ground or V_{CC}.

FEATURES

- Internal stand-by switch circuit; CMOS drive possible.
- Can be used as OCL connection.
- Very low output offset voltage : V_{offset} = 150 mV (MAX.)
- High output power : P_O = 23 W (TYP.) @ R_L = 4 Ω, V_{CC} = 14.4 V, THD = 10 %
  P_O = 20 W (TYP.) @ R_L = 4 Ω, V_{CC} = 13.2 V, THD = 10 %
- Very low distortion : THD = 0.06 % (TYP.)
- Following protection circuits are included.
  (1) Load dump voltage surge protection circuit.
  (2) Thermal shut down protection circuit.
  (3) Output terminal short circuit protection circuit. (V_{CC} to OUT, OUT to GND, OUT to OUT)
  (4) Loudspeaker protection circuit.

BLOCK DIAGRAM



CONNECTION DIAGRAM

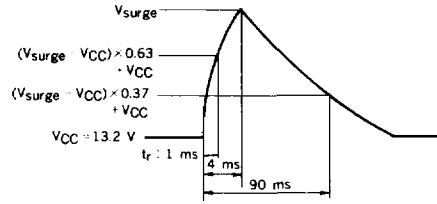
PIN NO.	CONNECTION	PIN NO.	CONNECTION
1	Input $_1$	8	V_{CC}
2	NFB $_1$	9	Stand-by switch
3	GND (Input)	10	Bootstrap $_2$
4	Output $_1$ Devided	11	Output $_2$
5	NFB $_2$	12	GND (Output)
6	GND	13	Output $_1$
7	Filter	14	Bootstrap $_1$

5

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage (Note)	$V_{CC\ surge}$	60*	V
Supply Voltage (Operational)	V_{CC}	18	V
Circuit Current (Peak)	$I_{CC\ peak}$	4.5	A
Power Dissipation	P_D	20	W
Operating Temperature	T_{opt}	−30 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*



Surge Pulse Waveform

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C)

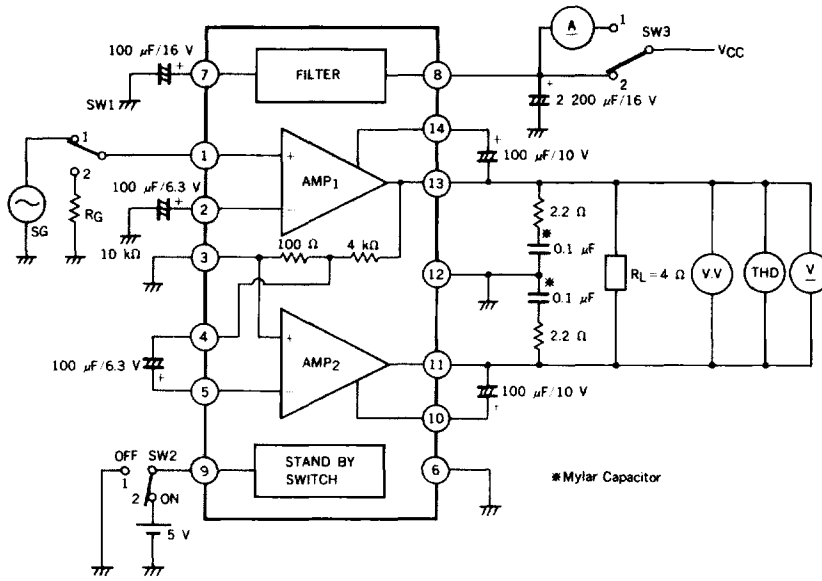
Supply Voltage Range	9 to 16	V
Load Impedance	3.2 to 16	Ω
Pin 9 Voltage (Operating)	3.5 to V_{CC}	V
Pin 9 Voltage (Stand-by)	0 to 1.5	V
Voltage Gain	34 MIN.	dB

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 13.2 V, R_L = 4 Ω, f = 1 kHz, Using 4 °C/W heatsink)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Quiescent Current	I_{CC}		120	150	mA	V_i = 0
Output Offset Voltage	V_{offset}		0	±150	mV	V_i = 0
Output Power	P_O		23		W	V_{CC} = 14.4 V, THD = 10 %**
		16	20		W	V_{CC} = 13.2 V, THD = 10 %**
Voltage Gain	A_v	38	40	42	dB	P_O = 1 W
Total Harmonic Distortion	THD		0.06	0.3	%	P_O = 1 W
Output Noise Level	V_n		0.24	0.8	mV	R_G = 10 kΩ, BW = 20 Hz to 20 kHz
Supply Voltage Rejection Ratio	SVR	40	52		dB	R_G = 0, f_{rip} = 100 Hz, V_{rip} = 1.0 V
Input Resistance	R_i	45	60		kΩ	
Roll-off Frequency	f_H		160		kHz	A_v = −3 dB from 1 kHz Ref High
	f_L		10		Hz	A_v = −3 dB from 1 kHz Ref Low
Stand-by Current	$I_{CC(SB)}$		0.4	0.6	mA	$0 \leq V_g \leq 1.5$ V

(**Using a Voltmeter: HP-400FL)

TEST CIRCUIT

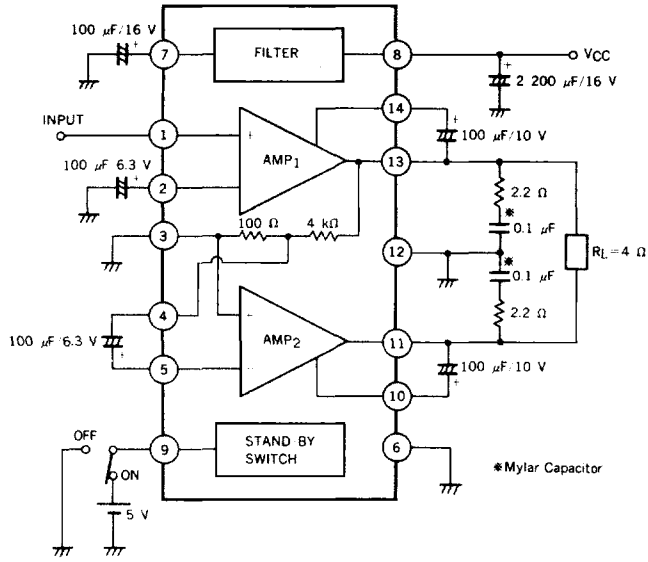


SWITCH POSITION

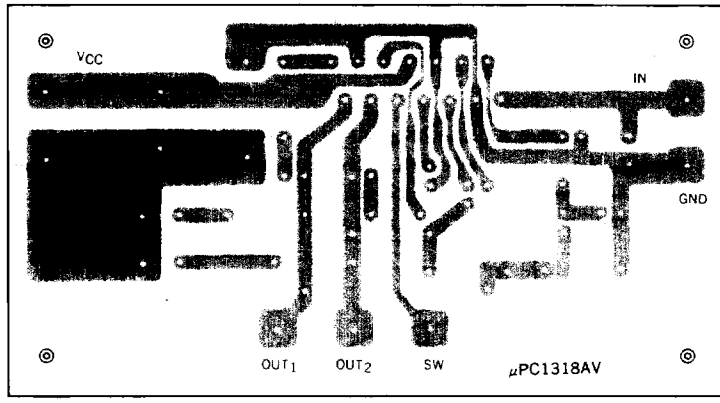
CHARACTERISTIC	SYMBOL	SW 1	SW 2	SW 3
Quiescent Current	I_{CC}	2	2	1
Output Offset Voltage	V_{offset}	2	2	2
Voltage Gain	A_V	1	2	2
Output Power	P_O	1	2	2
Total Harmonic Distortion	THD	1	2	2
Output Noise Level	V_n	2	2	2
Stand-by Current	$I_{CC(SB)}$	1	1	1

5

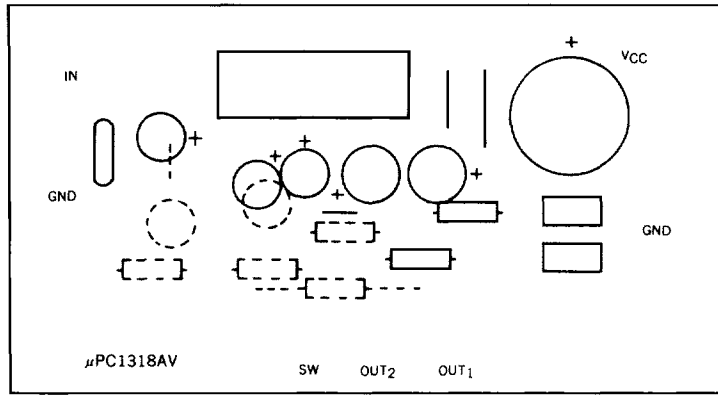
TYPICAL APPLICATION



EXAMPLE FOR PRINTED CIRCUIT BOARD (Copper foil side)



COMPONENT LAYOUT



INSTRUCTION FOR USE

(1) How to attach the heatsink.

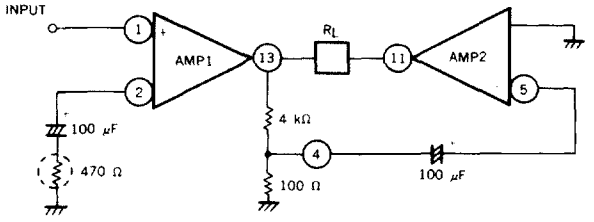
- Surely use the silicon grease.
- Please keep the fastening torque for the screw in the range of 5 to 8 kg-cm.
- Flatness of attached area of heatsink should be kept within 0.1 mm.

(2) When this IC is unstable due to the high impedance of signal source, connect a capacitor (about 1 000 pF) between Pin 1 and Pin 3.

(3) How to decrease voltage gain A_v.

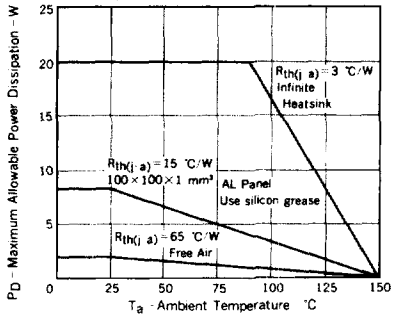
This IC is designed to use A_v of 40 dB but A_v can be set down to 34 dB by modifying the application circuit. The modified point are shown by dotted areas which include additional component. Other external components are as same as in the case of typical application (page 5).

(4) Polarity inversion of the power supply cause μPC1318AV to break down immediately.

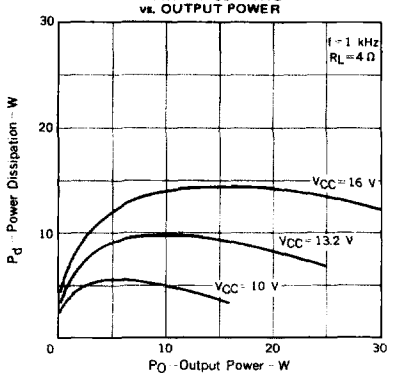


TYPICAL CHARACTERISTICS (T_a = 25 °C)

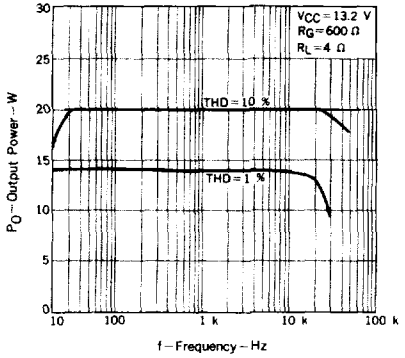
MAXIMUM ALLOWABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE



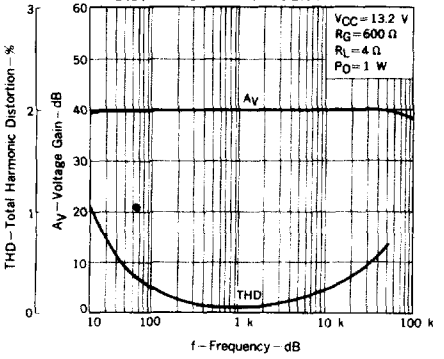
POWER DISSIPATION vs. OUTPUT POWER



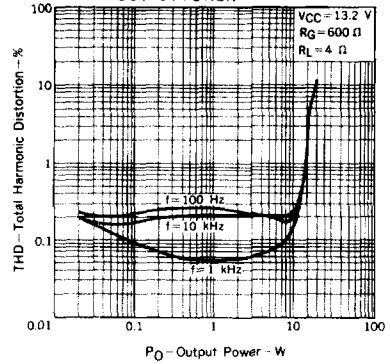
OUTPUT POWER vs. FREQUENCY



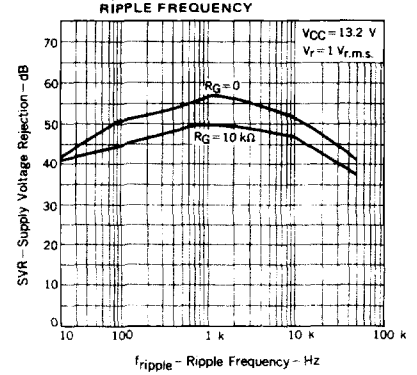
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



SUPPLY VOLTAGE REJECTION vs. RIPPLE FREQUENCY



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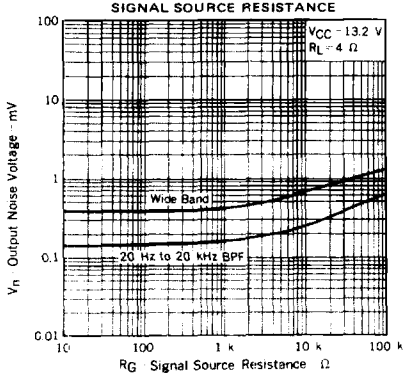
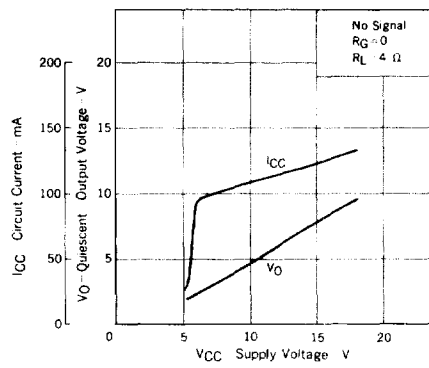
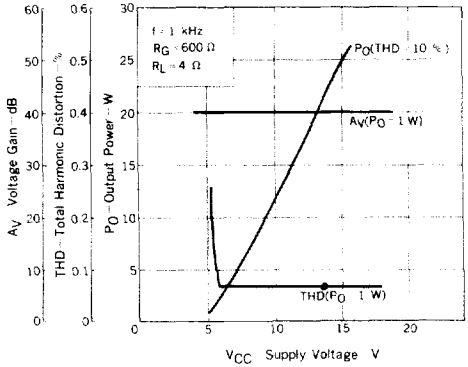
OUTPUT NOISE VOLTAGE vs.
SIGNAL SOURCE RESISTANCE



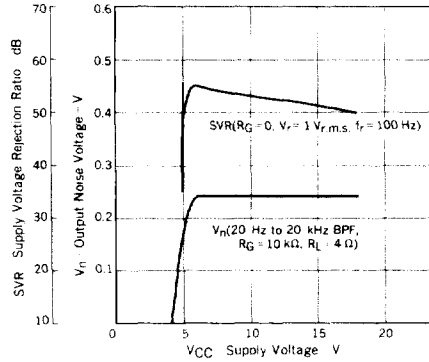
SUPPLY VOLTAGE CHARACTERISTICS



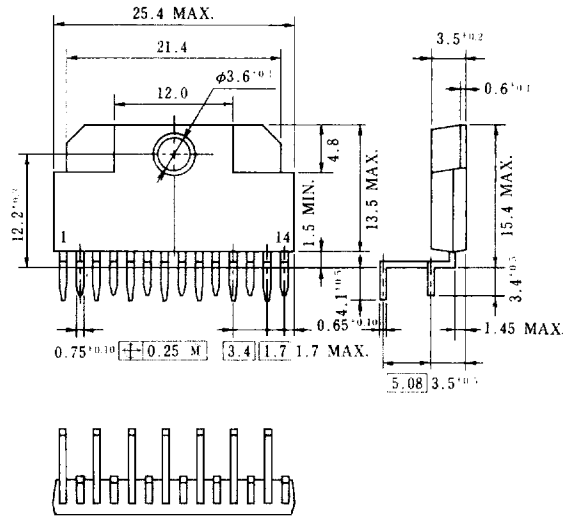
SUPPLY VOLTAGE CHARACTERISTICS



SUPPLY VOLTAGE CHARACTERISTICS



14 PIN PLASTIC POWER V-DIP (L) (Unit : mm)



The μPC1318AV is an audio power amplifier specifically designed for car audio applications.

This IC contains a stand-by switch circuit so the entire circuit can be turned on and off with external control signal from microprocessors and so on.

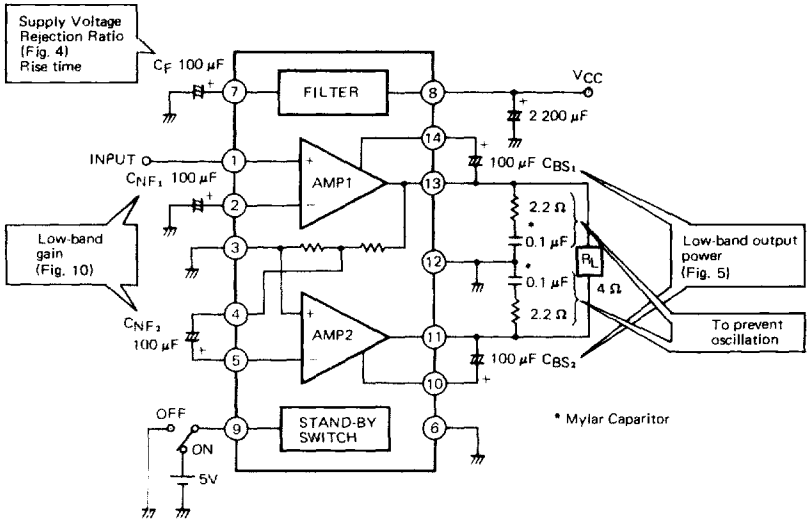
It also contains various protection circuit against external stresses.

This data sheet describes the μPC1318AV circuit operation, influences of external parts changing on the characteristics, and notes for use.

1. APPLICATION CIRCUIT

Fig. 1 shows the recommended application circuit for the μPC1318AV.

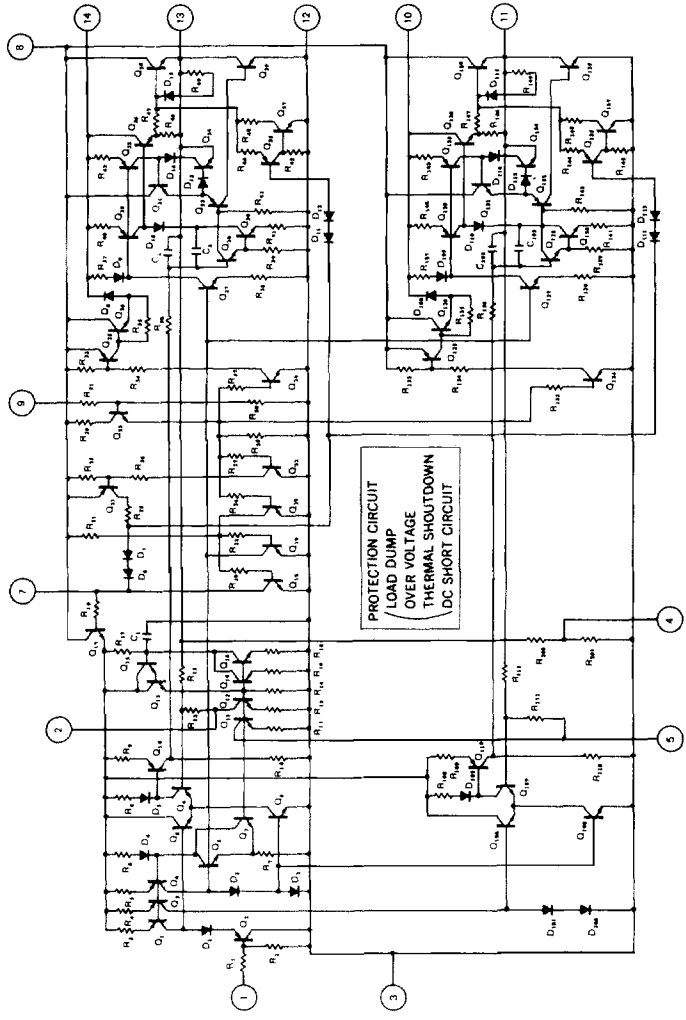
Fig. 1 μPC1318AV Recommended Application Circuit



2. EQUIVALENT CIRCUIT

Fig. 2 shows the μPC1318AV equivarent circuit.

Fig. 2 μPC1318AV Equivarent Circuit



3. CIRCUIT OPERATION

The description below uses the equivarent circuit in Fig. 2.

3.1 Circuit Operation Summary

The input signal passes through the level-shift circuit, is amplified in the differential amplifier stage while being single-ended, and is sent to the driver stage. It is then further amplified in the pre-driver stage and get out through the SEPP circuit (AMP1). In AMP2, the signal (a pat of the output signal from AMP1) is input to the inverted input terminal (NF terminal) in the differential amplifier stage and get out by the SEPP circuit in the same way as AMP1.

3.2 Input Stage

The input stage consists of Q_1 through Q_{10}, R_1 through R_{10}, and D_1 through D_5. Q_1, Q_3, Q_4, D_4, R_3 through R_6, D_3, and D_8 compose constant-current circuits that supply bias current to D_1 through D_3, Q_2, Q_6 and Q_9. R_8, D_5, R_9, and Q_{10} compose a current-mirror circuit that shifts the level of the signal amplified in the differential amplifier stage while single-ending the signal and sends it to the pre-driver stage.

This IC contains bias resistor R_2 in the signal input section to allow direct connection to the input coupling capacitor.

3.3 Output DC Voltage Set-up Circuit

In the case of a power amplifier operating with a single power supply such as the μPC1318AV, output DC voltage (V_{ODC}) is required to be set at a half of the supply voltage to obtain sufficient output power.

The output DC voltage set-up circuit of the μPC1318AV cosists of Q_{12} (Q_{11}), Q_{14}, Q_{16}, R_{13} (R_{11}), R_{14}, R_{15} (R_{115}), R_{16} through R_{19}, R_{21}, D_6 and D_7.

The V_{ODC} can be obtained by the following expression:

$$V_{ODC} = V_{NF} + I_{R15} \times R_{15} \quad \cdots (1)$$

(V_N: Base voltage of Q_9, I_{R15}: Current through R_{15})

Q_{12}, Q_{14}, Q_{16}, R_{13}, R_{14}, R_{16} and R_{18} compose a current-mirror circuit and following relations are satisfied:

$$R_{13} = R_{16} = R_{18} \quad \cdots (2)$$

$$I_{R13} = I_{R16} = I_{R18} = I_{R15} \quad \cdots (3)$$

Therefore, expression (1) can be rewritten as shown below:

$$V_{ODC} = 2\,V_{BE}' + (V_{CC} - 6\,V_{BE}' - V_{R19} - V_{R23} - V_{CE(sat)Q21}) \times R_{15}/(R' + 2R_{17}) \quad \cdots (4)$$

In the above expression, following relations are satisfied:

$$V_{BE}' = V_{BEQ12} = V_{BEQ14} = V_{BEQ16} = V_{BEQ13} = V_{BEQ15} = V_{BEQ17} = V_{D6} = V_{D7} = V_{BEQ8} = V_{BEQ9} \quad \cdots (5)$$

(V_{BEQ12}: Voltage between emitter and base of Q_{12},
V_{D6}: Forward voltage of diode D_6)

$$R' = R_{13} = R_{16} = R_{18} \quad \cdots (6)$$

The μPC1318AV is designed as follows:

$$R_{15}/(R' + 2\,R_{17}) = 0.61 \quad \cdots (7)$$

$$V_{R19} + V_{R27} = 0.36\ [V] \quad \cdots (8)$$

$$V_{CE(sat)Q21} = 0.1\ [V] \quad \cdots (9)$$

$$V_{BE}' = 0.7\ [V] \quad \cdots (10)$$

For example, if V_{CC} = 13.2 [V], V_{ODC} can be the following value:

$$V_{ODC} = 6.61 \text{ [V]} \quad \ldots\ldots (11)$$

That is to say, the V_{ODC} is set at almost a half of the supply voltage.
The above explanation is for AMP1, and that for AMP2 can also be explained in the same way.

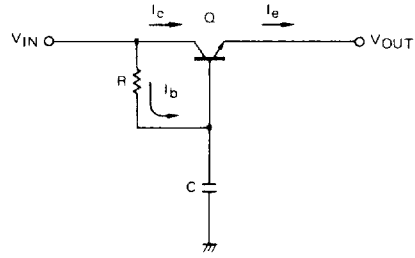
3.4 Filter Circuit

The ratio between the ripple voltage in power supply and its output is called the supply voltage rejection ratio (SVR).

For better supply voltage rejection ratio, the μPC1318AV uses a filter. The filter circuit consists of Q_{17}, Q_{21}, R_{19}, R_{23} and external capacitor for stabilizing the internal bias circuit.

Fig. 3 shows the basic circuit for this ripple filter to explain its operation.

Fig. 3. Basic Ripple Filter Circuit



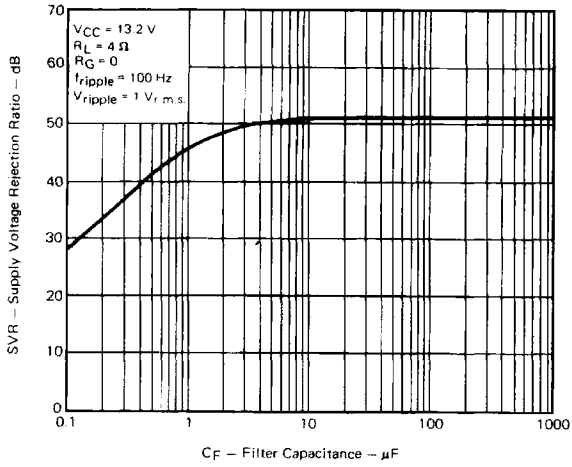
Provided that the DC current amplification factor for transistor Q is h_{FE}, the following expression can be satisfied:

$$I_e = I_b (1 + h_{FE})$$

That is to say, the current through resistor R contributing to ripple removal is $1/(1 + h_{FE})$ times of the actual load current, so the apparent capacitance C, becomes $(1 + h_{FE})$ times greater than real, thus increasing the filter effect.

Fig. 4 shows the relationship between the ripple frequency and external capacitance C_F to the μPC1318AV.

Fig. 4 SVR vs. C_F Characteristics



3.5 Stand-by Switch Circuit

The stand-by switch circuit consists of Q_{21} laid between the V_{CC} line and the filter circuit; Q_{24} and Q_{27}, which control the constant-current circuit at output stage; and Q_{18}, Q_{19}, Q_{20}, and Q_{22}, which drive these switches.

When the voltage of the control terminal (pin 9) is low level (1.5 V or less), Q_{23} turns off. Therefore Q_{24} and Q_{27} turn off to stop the flow of bias current into the output stage. At the same time, Q_{21} turns off to stop also the flow of bias current into the input stage. At the result, amplifier system becomes non-operational.

When the voltage of the control terminal (pin 9) is high level (3.5 V or more), Q_{23} turns on. Therefore Q_{24} and Q_{27} turn on and bias current flow into the output stage. At the same time, Q_{21} turns on and bias current flow into the input stage. At the result, amplifier system becomes operational.

The stand-by switch circuit for AMP1 is explained above; that for AMP2 can also be explained in the same way.

In addition, 100 μA is sufficient as a current inputted to the control terminal (pin 9) to obtain the high level. Therefore, control terminals of four μPC1318AVs can be connected in parallel to a I/O port of standard microprocessors.

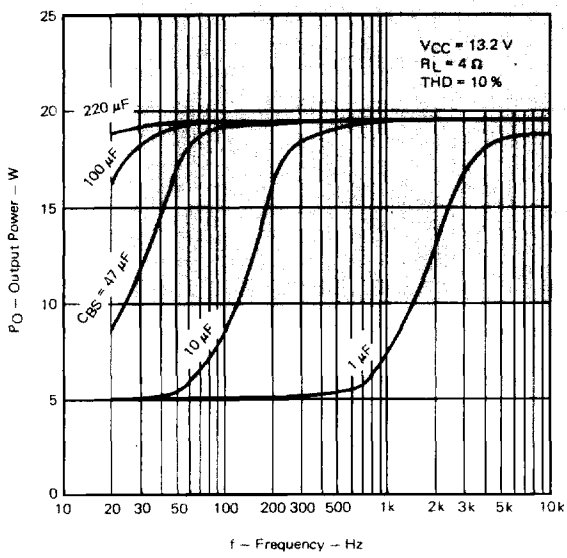
3.6 Bootstrap Circuit

A part of the output signal is fed back to the internal bias circuit through the bootstrap capacitor, so that the loss of the output voltage on the upper side is equal to $V_{CE(sat)}$ of output power transistor Q_{38} (Q_{138}). This circuit, in other words, provides larger output power under the same conditions. If the bootstrap circuit is not available, that is, if pins 8 and 14 (10) are short-circuited, the upper side loss (V_{LOSS}) can be obtained by the following expression:

$$V_{LOSS} = V_{BEQ38} + V_{BEQ36} + V_{CEQ29} + V_{R40} + V_{R47}$$
$$V_{BEQ138} + V_{BEQ136} + V_{CEQ129} + V_{R140} + V_{R147}$$

The loss thus is larger than $V_{CE(sat)}$ of output power transistor Q_{38} (Q_{138}).
The value of the bootstrap capacitor influences low frequency output power characteristic. (See Fig. 5.)

Fig. 5 P_O vs. f Characteristic

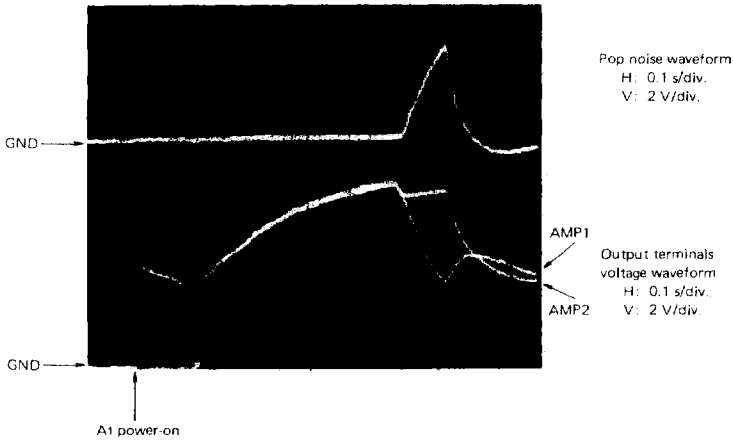


3.7 Pop Noise Reduction Circuit

The pop noise reduction circuit of the μPC1318AV consists of D_{11} (D_{111}), D_{12} (D_{112}), Q_{35} (Q_{135}), Q_{37} (Q_{137}), and D_{15} (D_{115}).

In an amplifier for BTL operation, such as the μPC1318AV, pop noise is caused by the steep change in voltage between output terminals before the output terminal voltage reaches to the half of supply voltage. The μPC1318AV uses the above circuit to loosen the voltage changes (V_{O1}, V_{O2}) of output terminals for AMP1 and AMP2 and to make these changes equal ($V_{O1} = V_{O2}$ = Filter voltage + 6 V_{BE}), thus pop noise is reduced. Fig. 6 shows the change (pop noise) in the voltage between output terminals and also the changes of each output terminal voltages after μPC1318AV is turned on.

Fig. 6 Pop Noise and Output Terminal Voltage Changes



Pop noise is generated after about 0.6 second from power-on, because the voltage of the NF terminal voltage of AMP2 is higher than that of AMP1 by down of voltage in resistor R_{201}, so AMP2 starts operating earlier than AMP1. However, pop noise generated in this point is very low.

4. VOLTAGE GAIN SETTING

4.1 Principle of Operation

Fig. 7 shows the circuit configuration of the μPC1318AV. AMP1 and AMP2 operate as a non-inverting amplifier, respectively. The input signal to AMP2 is generated by dividing the output from AMP2 with resistors r_3 and r_4, and the values of the AMP1's output division ratio $r_4/(r_3 + r_4)$ and AMP2's voltage gain $r_1/(r_2 + r_4)$ become 1. The outputs of AMP2 and AMP1 therefore have the same level but inverse phases.(See the following expression.)

If the voltage gains of AMP1 and AMP2 are A_{V1} and A_{V2}, respectively, they can be expressed as follows:

$$A_{V1} = 20 \text{ Log } (r_1/r_2) \quad (\text{Where } r_2 \ll r_1)$$
$$A_{V2} = 20 \text{ Log } (r_1/r_2)$$

Input signal to AMP2, V_{i2} can be expressed as follows, using AMP1's output voltage:

$$V_{i2} = [r_4/(r_3 + r_4)] \times V_{O1}$$

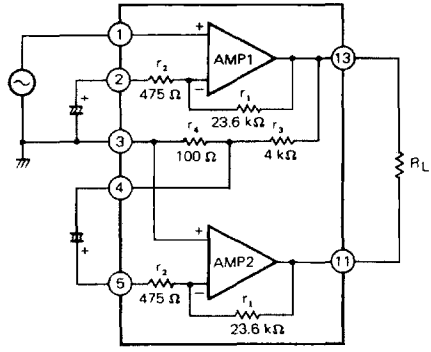
Therefore output voltage from AMP2, V_{O2} can be obtained as follows:

$$V_{O2} = -V_{O1} [r_4/(r_3 + r_4)] \times [r_1/(r_2 + r_4)]$$
$$\fallingdotseq -V_{O1}$$

The total voltage gain, A_V can therefore be obtained as shown below:

$$A_V = A_{V1} \times 2$$
$$= 20 \text{ Log } (r_1/r_2) + 6 \text{ (dB)}$$

Fig. 7 μPC1318AV Circuit Configuration



(Resistors r_1 through r_4 are built into this IC.)

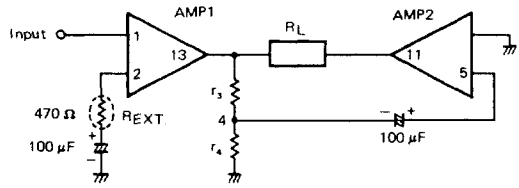
4.2 How to Set Voltage Gain

This IC is designed to use at 40 dB voltage gain so the external components are most reduced. But A_V can be set down to 34 dB with a external resistor as shown in Fig. 8. The modified point is shown by dotted circle and it is a additional component. Other external components are as same as the standard application. The voltage gain A_V of this IC decrease as increase of the value of external resistor $R_{EXT.}$ as shown in Fig. 9. The voltage gain in this case can be obtained by the following expression:

$$A_V = 20 \text{ Log } [r_1/(r_2 + R_{EXT.})] + 6 \text{ (dB)}$$

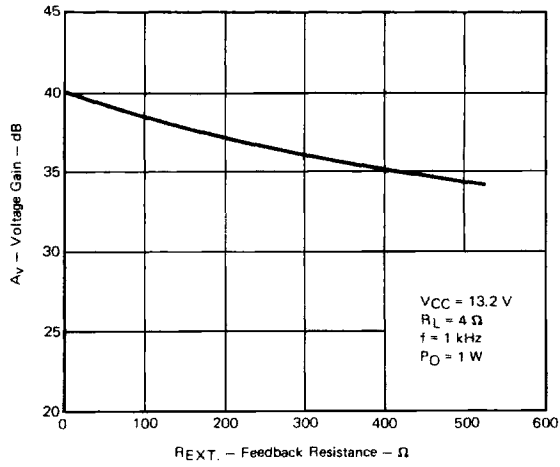
Fig. 9 shows the actual A_V vs. $R_{EXT.}$ characteristic.

Fig. 8 How to Set Voltage Gain (A_V = 34 dB)



THD = 0.045 %
SVR = 54 dB

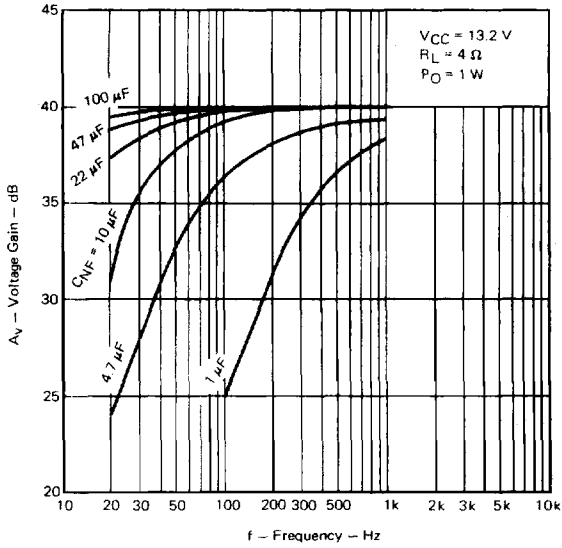
Fig. 9 A_V vs. $R_{EXT.}$ Characteristic



4.3 Low Frequency Band Characteristic of Voltage Gain

The low frequency band characteristic of voltage gain can be determined by the value of coupling capacitor C_{NF}. Fig. 10 shows the A_v vs. f characteristic.

Fig. 10 A_V vs. f Characteristic



5. NOTICE FOR USE

- One-point earthing is ideal, but if this is impossible, keep the input loop out of the output loop.
- The R, C circuit network of output terminal prevent oscillation. Mylar capacitor with good temperature and high-frequency characteristic is recommended as C.
- When this IC is unstable due to the high impedance of signal source, connect a capacitor (around 1 000 pF) between the input terminal (pin 1) and ground (pin 3).
- Do not use this IC at less than 34 dB. Oscillation may otherwise occur.
- Surely use the silicon grease and keep fastening torque for the screw in the range of 5 to 8 kg-cm.