

# FAN7930C

## Critical Conduction Mode PFC Controller

### Features

- PFC-Ready Signal
- Input Voltage Absent Detection
- Maximum Switching Frequency Limitation
- Internal Soft-Start and Startup without Overshoot
- Internal Total Harmonic Distortion (THD) Optimizer
- Precise Adjustable Output Over-Voltage Protection
- Open-Feedback Protection and Disable Function
- Zero-Current Detector (ZCD)
- 150µs Internal Startup Timer
- MOSFET Over-Current Protection (OCP)
- Under-Voltage Lockout with 3.5V Hysteresis
- Low Startup and Operating Current
- Totem-Pole Output with High State Clamp
- +500/-800mA Peak Gate Drive Current
- 8-Pin SOP

### Applications

- Adapter
- Ballast
- LCD TV, CRT TV
- SMPS

### Description

The FAN7930C is an active power factor correction (PFC) controller for boost PFC applications that operate in critical conduction mode (CRM). It uses a voltage-mode PWM that compares an internal ramp signal with the error amplifier output to generate a MOSFET turn-off signal. Because the voltage-mode CRM PFC controller does not need rectified AC line voltage information, it saves the power loss of an input voltage sensing network necessary for a current-mode CRM PFC controller.

FAN7930C provides over-voltage protection (OVP), open-feedback protection, over-current protection (OCP), input-voltage-absent detection, and under-voltage lockout protection (UVLO). The PFC-ready pin can be used to trigger other power stages when PFC output voltage reaches the proper level with hysteresis. The FAN7930C can be disabled if the INV pin voltage is lower than 0.45V and the operating current decreases to a very low level. Using a new variable on-time control method, THD is lower than the conventional CRM boost PFC ICs.

### Related Resources

[AN-8035 — Design Consideration for Boundary Conduction Mode PFC Using FAN7930](#)

### Ordering Information

| Part Number | Operating Temperature Range | Top Mark | Package                            | Packing Method |
|-------------|-----------------------------|----------|------------------------------------|----------------|
| FAN7930CM   | -40 to +125°C               | FAN7930C | 8-Lead Small Outline Package (SOP) | Rail           |
| FAN7930CMX  |                             |          |                                    | Tape & Reel    |



## Pin Configuration

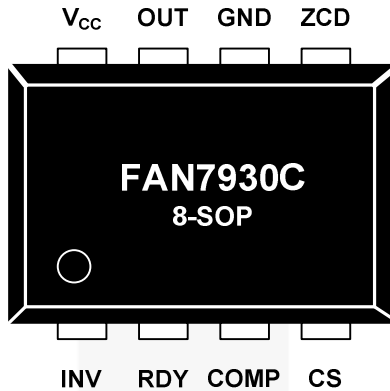


Figure 3. Pin Configuration (Top View)

## Pin Definitions

| Pin # | Name            | Description   |
|-------|-----------------|---|
| 1     | INV             | This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V.  |
| 2     | RDY             | This pin is used to detect PFC output voltage reaching a pre-determined value. When output voltage reaches 89% of rated output voltage, this pin is pulled HIGH, which is an (open-drain) output type.                                |
| 3     | COMP            | This pin is the output of the transconductance error amplifier. Components for the output voltage compensation should be connected between this pin and GND.  |
| 4     | CS              | This pin is the input of the over-current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise. |
| 5     | ZCD             | This pin is the input of the zero-current detection block. If the voltage of this pin goes higher than 1.5V, then goes lower than 1.4V, the MOSFET is turned on.  |
| 6     | GND             | This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.  |
| 7     | OUT             | This pin is the gate drive output. The peak sourcing and sinking current levels are +500mA and -800mA, respectively. For proper operation, the stray inductance in the gate driving path must be minimized.                           |
| 8     | V <sub>CC</sub> | This is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.   |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol           | Parameter   | Min.                              | Max.  | Unit |
|------------------|---|-----------------------------------|-------|------|
| $V_{CC}$         | Supply Voltage  |                                   | $V_Z$ | V    |
| $I_{OH}, I_{OL}$ | Peak Drive Output Current                                     | -800                              | +500  | mA   |
| $I_{CLAMP}$      | Driver Output Clamping Diodes $V_O > V_{CC}$ or $V_O < -0.3V$ | -10                               | +10   | mA   |
| $I_{DET}$        | Detector Clamping Diodes                                      | -10                               | +10   | mA   |
| $V_{IN}$         | Error Amplifier Input, Output, ZCD and RDY Pin <sup>(1)</sup> | -0.3                              | 8.0   | V    |
|                  | CS Input Voltage <sup>(2)</sup>                               | -10.0                             | 6.0   |      |
| $T_J$            | Operating Junction Temperature                                |                                   | +150  | °C   |
| $T_A$            | Operating Temperature Range                                   | -40                               | +125  | °C   |
| $T_{STG}$        | Storage Temperature Range                                     | -65                               | +150  | °C   |
| ESD              | Electrostatic Discharge Capability                            | Human Body Model, JESD22-A114     | 2.5   | kV   |
|                  |   | Charged Device Model, JESD22-C101 | 2.0   |      |

### Notes:

- When this pin is supplied by external power sources by accident, its maximum allowable current is 50mA.
- In case of DC input, acceptable input range is -0.3V~6V: within 100ns -10V~6V is acceptable, but electrical specifications are not guaranteed during such a short time.

## Thermal Impedance

| Symbol        | Parameter  | Min. | Max. | Unit |
|---------------|--|------|------|------|
| $\Theta_{JA}$ | Thermal Resistance, Junction-to-Ambient <sup>(3)</sup> | 150  |      | °C/W |

### Note:

- Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

## Electrical Characteristics

$V_{CC} = 14V$ ,  $T_A = -40^{\circ}C \sim +125^{\circ}C$ , unless otherwise specified.

| Symbol                         | Parameter   | Conditions   | Min.  | Typ.  | Max.  | Units |
|--------------------------------|---|--|-------|-------|-------|-------|
| <b>V<sub>CC</sub> Section</b>  |   |  |       |       |       |       |
| V <sub>START</sub>             | Start Threshold Voltage                                   | V <sub>CC</sub> Increasing                         | 11    | 12    | 13    | V     |
| V <sub>STOP</sub>              | Stop Threshold Voltage                                    | V <sub>CC</sub> Decreasing                         | 7.5   | 8.5   | 9.5   | V     |
| HY <sub>UVLO</sub>             | UVLO Hysteresis   |  | 3.0   | 3.5   | 4.0   | V     |
| V <sub>Z</sub>                 | Zener Voltage   | I <sub>CC</sub> =20mA                              | 20    | 22    | 24    | V     |
| V <sub>OP</sub>                | Recommended Operating Range                               |  | 13    |       | 20    | V     |
| <b>Supply Current Section</b>  |   |  |       |       |       |       |
| I <sub>START</sub>             | Startup Supply Current                                    | V <sub>CC</sub> =V <sub>START</sub> -0.2V          |       | 120   | 190   | μA    |
| I <sub>OP</sub>                | Operating Supply Current                                  | Output Not Switching                               |       | 1.5   | 3.0   | mA    |
| I <sub>DOP</sub>               | Dynamic Operating Supply Current                          | 50kHz, C <sub>I</sub> =1nF                         |       | 2.5   | 4.0   | mA    |
| I <sub>OPDIS</sub>             | Operating Current at Disable                              | V <sub>INV</sub> =0V                               | 90    | 160   | 230   | μA    |
| <b>Error Amplifier Section</b> |   |  |       |       |       |       |
| V <sub>REF1</sub>              | Voltage Feedback Input Threshold1                         | T <sub>A</sub> =25°C                               | 2.465 | 2.500 | 2.535 | V     |
| ΔV <sub>REF1</sub>             | Line Regulation   | V <sub>CC</sub> =14V~20V                           |       | 0.1   | 10.0  | mV    |
| ΔV <sub>REF2</sub>             | Temperature Stability of V <sub>REF1</sub> <sup>(4)</sup> |  |       | 20    |       | mV    |
| I <sub>EA,BS</sub>             | Input Bias Current  | V <sub>INV</sub> =1V~4V                            | -0.5  |       | 0.5   | μA    |
| I <sub>EAS,SR</sub>            | Output Source Current                                     | V <sub>INV</sub> =V <sub>REF</sub> -0.1V           |       | -12   |       | μA    |
| I <sub>EAS,SK</sub>            | Output Sink Current                                       | V <sub>INV</sub> =V <sub>REF</sub> +0.1V           |       | 12    |       | μA    |
| V <sub>EAH</sub>               | Output Upper Clamp Voltage                                | V <sub>INV</sub> =1V, V <sub>CS</sub> =0V          | 6.0   | 6.5   | 7.0   | V     |
| V <sub>EAZ</sub>               | Zero-Duty Cycle Output Voltage                            |  | 0.9   | 1.0   | 1.1   | V     |
| g <sub>m</sub>                 | Transconductance <sup>(4)</sup>                           |  | 90    | 115   | 140   | μmho  |
| <b>Maximum On-Time Section</b> |   |  |       |       |       |       |
| t <sub>ON,MAX1</sub>           | Maximum On-Time Programming 1                             | T <sub>A</sub> =25°C, V <sub>ZCD</sub> =1V         | 35.5  | 41.5  | 47.5  | μs    |
| t <sub>ON,MAX2</sub>           | Maximum On-Time Programming 2                             | T <sub>A</sub> =25°C,<br>I <sub>ZCD</sub> =0.469mA | 11.2  | 13.0  | 14.8  | μs    |
| <b>Current-Sense Section</b>   |   |  |       |       |       |       |
| V <sub>CS</sub>                | Current-Sense Input Threshold Voltage Limit               |  | 0.7   | 0.8   | 0.9   | V     |
| I <sub>CS,BS</sub>             | Input Bias Current  | V <sub>CS</sub> =0V~1V                             | -1.0  | -0.1  | 1.0   | μA    |
| t <sub>CS,D</sub>              | Current-Sense Delay to Output <sup>(4)</sup>              | dV/dt=1V/100ns,<br>from 0V to 5V                   |       | 350   | 500   | ns    |

Continued on the following page...

## Electrical Characteristics

$V_{CC} = 14V$ ,  $T_A = -40^{\circ}C \sim +125^{\circ}C$ , unless otherwise specified.

| Symbol   | Parameter   | Conditions                           | Min.  | Typ.  | Max.  | Units       |
|--|---|--------------------------------------|-------|-------|-------|-------------|
| <b>Zero-Current Detect Section</b>                         |   |                                      |       |       |       |             |
| $V_{ZCD}$  | Input Voltage Threshold <sup>(4)</sup>                  |                                      | 1.35  | 1.50  | 1.65  | V           |
| $HY_{ZCD}$   | Detect Hysteresis <sup>(4)</sup>                        |                                      | 0.05  | 0.10  | 0.15  | V           |
| $V_{CLAMPH}$   | Input High Clamp Voltage                                | $I_{DET}=3mA$                        | 5.5   | 6.2   | 7.5   | V           |
| $V_{CLAMPL}$   | Input Low Clamp Voltage                                 | $I_{DET}= -3mA$                      | 0     | 0.65  | 1.00  | V           |
| $I_{ZCD,BS}$   | Input Bias Current                                      | $V_{ZCD}=1V \sim 5V$                 | -1.0  | -0.1  | 1.0   | $\mu A$     |
| $I_{ZCD,SR}$   | Source Current Capability <sup>(4)</sup>                | $T_A=25^{\circ}C$                    |       |       | -4    | mA          |
| $I_{ZCD,SK}$   | Sink Current Capability <sup>(4)</sup>                  | $T_A=25^{\circ}C$                    |       |       | 10    | mA          |
| $t_{ZCD,D}$  | Maximum Delay From ZCD to Output Turn-On <sup>(4)</sup> | $dV/dt=-1V/100ns$ ,<br>from 5V to 0V | 100   |       | 200   | ns          |
| <b>Output Section</b>                                      |   |                                      |       |       |       |             |
| $V_{OH}$   | Output Voltage High                                     | $I_O=-100mA$ , $T_A=25^{\circ}C$     | 9.2   | 11.0  | 12.8  | V           |
| $V_{OL}$   | Output Voltage Low                                      | $I_O=200mA$ , $T_A=25^{\circ}C$      |       | 1.0   | 2.5   | V           |
| $t_{RISE}$   | Rising Time <sup>(4)</sup>                              | $C_{IN}=1nF$                         |       | 50    | 100   | ns          |
| $t_{FALL}$   | Falling Time <sup>(4)</sup>                             | $C_{IN}=1nF$                         |       | 50    | 100   | ns          |
| $V_{O,MAX}$  | Maximum Output Voltage                                  | $V_{CC}=20V$ , $I_O=100\mu A$        | 11.5  | 13.0  | 14.5  | V           |
| $V_{O,UVLO}$   | Output Voltage with UVLO Activated                      | $V_{CC}=5V$ , $I_O=100\mu A$         |       |       | 1     | V           |
| <b>Restart / Maximum Switching Frequency Limit Section</b> |   |                                      |       |       |       |             |
| $t_{RST}$  | Restart Timer Delay                                     |                                      | 50    | 150   | 300   | $\mu s$     |
| $f_{MAX}$  | Maximum Switching Frequency <sup>(4)</sup>              |                                      | 250   | 300   | 350   | kHz         |
| <b>RDY Pin</b>   |   |                                      |       |       |       |             |
| $I_{RDY,SK}$   | Output Sink Current                                     |                                      | 1     | 2     | 4     | mA          |
| $V_{RDY,SAT}$  | Output Saturation Voltage                               | $I_{RDY,SK}=2mA$                     |       | 320   | 500   | mV          |
| $I_{RDY,LK}$   | Output Leakage Current                                  | Output High Impedance                |       |       | 1     | $\mu A$     |
| <b>Soft-Start Timer Section</b>                            |   |                                      |       |       |       |             |
| $t_{SS}$   | Internal Soft-Soft <sup>(4)</sup>                       |                                      | 3     | 5     | 7     | ms          |
| <b>UVLO Section</b>  |   |                                      |       |       |       |             |
| $V_{RDY}$  | Output Ready Voltage                                    |                                      | 2.166 | 2.240 | 2.314 | V           |
| $HY_{RDY}$   | Output Ready Hysteresis                                 |                                      |       | 0.189 |       | V           |
| <b>Protections</b>   |   |                                      |       |       |       |             |
| $V_{OVP}$  | OVP Threshold Voltage                                   | $T_A=25^{\circ}C$                    | 2.620 | 2.675 | 2.730 | V           |
| $HY_{OVP}$   | OVP Hysteresis  | $T_A=25^{\circ}C$                    | 0.120 | 0.175 | 0.230 | V           |
| $V_{EN}$   | Enable Threshold Voltage                                |                                      | 0.40  | 0.45  | 0.50  | V           |
| $HY_{EN}$  | Enable Hysteresis                                       |                                      | 0.050 | 0.10  | 0.15  | V           |
| $T_{SD}$   | Thermal Shutdown Temperature <sup>(4)</sup>             |                                      | 125   | 140   | 155   | $^{\circ}C$ |
| $T_{HYS}$  | Hysteresis Temperature of TSD <sup>(4)</sup>            |                                      |       | 60    |       | $^{\circ}C$ |

### Note:

4. These parameters, although guaranteed by design, are not production tested.

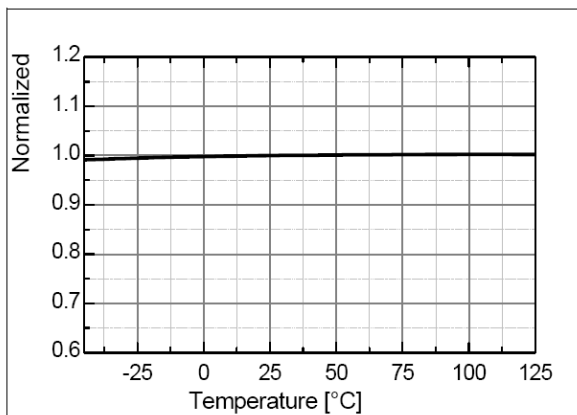
### Comparison of FAN7530 and FAN7930C

| Function                            | FAN7530  | FAN7930C                   | FAN7930C Advantages  |
|-------------------------------------|----------|----------------------------|--|
| PFC Ready Pin                       | None     | Integrated                 | <ul style="list-style-type: none"> <li>▪ No External Circuit for PFC Output UVLO</li> <li>▪ Reduce Power Loss and BOM Cost Caused by PFC Out UVLO Circuit</li> <li>▪ Versatile Open-Drain Pin</li> </ul> |
| Frequency Limit                     | None     | Integrated                 | <ul style="list-style-type: none"> <li>▪ Abnormal CCM Operation Prohibited</li> <li>▪ Abnormal Inductor Current Accumulation can be Prohibited</li> </ul>  |
| V <sub>IN</sub> -Absent Detection   | None     | Integrated                 | <ul style="list-style-type: none"> <li>▪ Increase System Reliability by testing for input supply voltage</li> <li>▪ Guarantee Stable Operation at Short Electric Power Failure</li> </ul>                |
| Soft-Start and Overshoot Prevention | None     | Integrated                 | <ul style="list-style-type: none"> <li>▪ Reduce Voltage and Current Stress at Startup</li> <li>▪ Eliminate Audible Noise due to Unwanted OVP Triggering</li> </ul>                                       |
| THD Optimizer                       | External | Internal                   | <ul style="list-style-type: none"> <li>▪ No External Resistor is Needed</li> </ul>   |
| TSD                                 | None     | 140°C with 60°C Hysteresis | <ul style="list-style-type: none"> <li>▪ Stable and Reliable TSD Operation</li> <li>▪ Converter Temperature Range Limited Range</li> </ul>   |

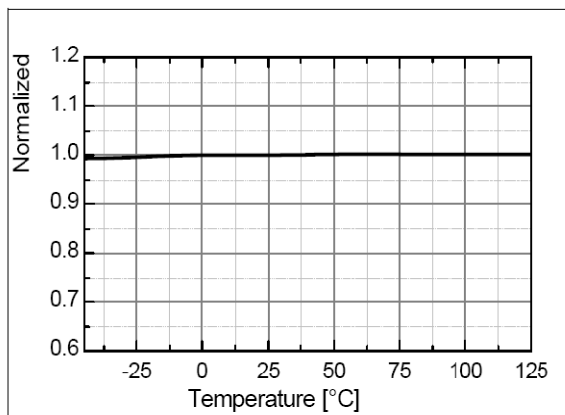
### Comparison between FAN7930 and FAN7930C

| Function                   | FAN7930 | FAN7930C   | FAN7930C Remark   |
|----------------------------|---------|------------|---|
| RDY Threshold              | 2.240V  | 2.240V     | <ul style="list-style-type: none"> <li>▪ If PFC rated output voltage is assumed 390V:<br/>           FAN7930: V<sub>RDY_HIGH</sub> trigger voltage = 349V<br/>           V<sub>RDY_LOW</sub> trigger voltage = 256V<br/>           FAN7930C: V<sub>RDY_HIGH</sub> trigger voltage = 349V<br/>           V<sub>RDY_LOW</sub> trigger voltage = 320V</li> </ul> |
| RDY Hysteresis             | 0.600V  | 0.189V     |   |
| Control Range Compensation | None    | Integrated |   |

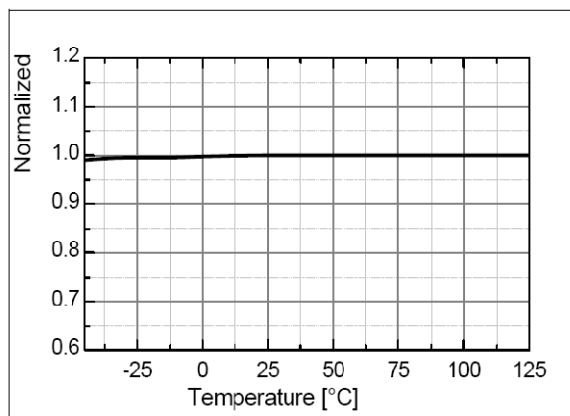
## Typical Performance Characteristics



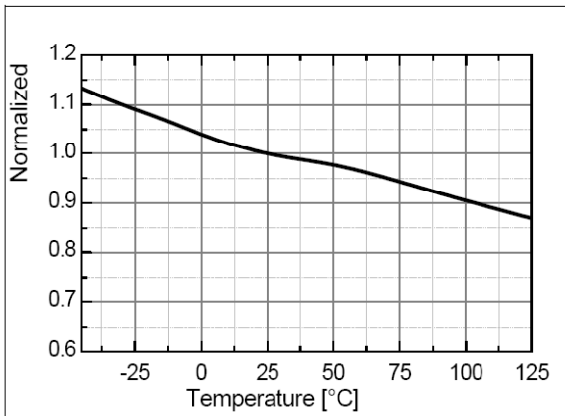
**Figure 4. Voltage Feedback Input Threshold 1 (V<sub>REF1</sub>) vs. T<sub>A</sub>**



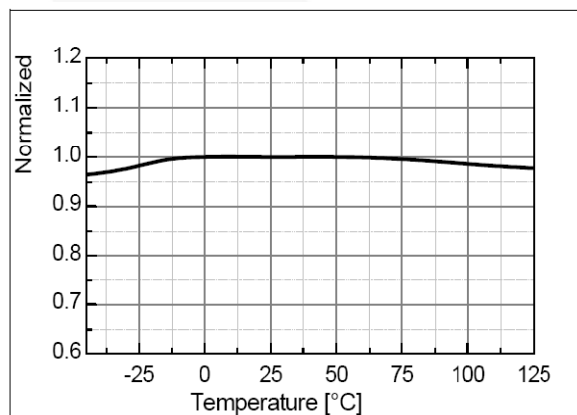
**Figure 5. Start Threshold Voltage (V<sub>START</sub>) vs. T<sub>A</sub>**



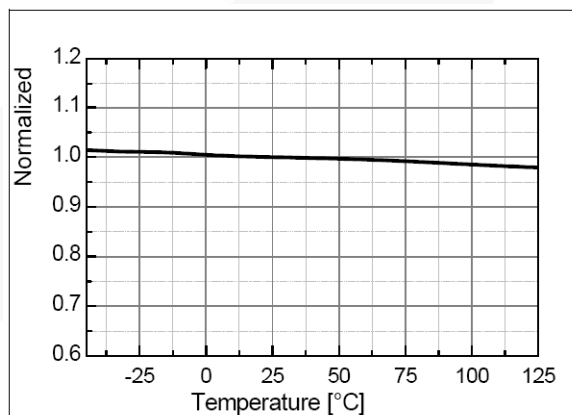
**Figure 6. Stop Threshold Voltage (V<sub>STOP</sub>) vs. T<sub>A</sub>**



**Figure 7. Startup Supply Current (I<sub>START</sub>) vs. T<sub>A</sub>**



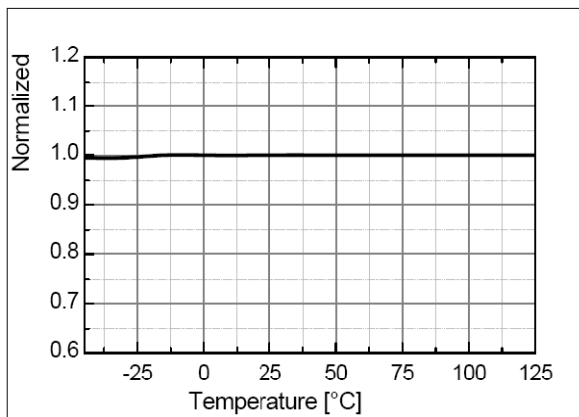
**Figure 8. Operating Supply Current (I<sub>OP</sub>) vs. T<sub>A</sub>**



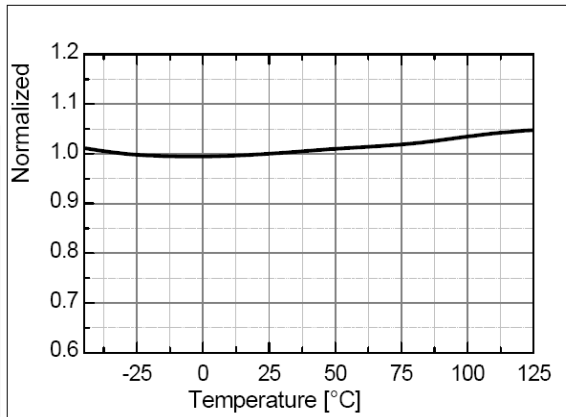
**Figure 9. Output Upper Clamp Voltage (V<sub>EAH</sub>) vs. T<sub>A</sub>**



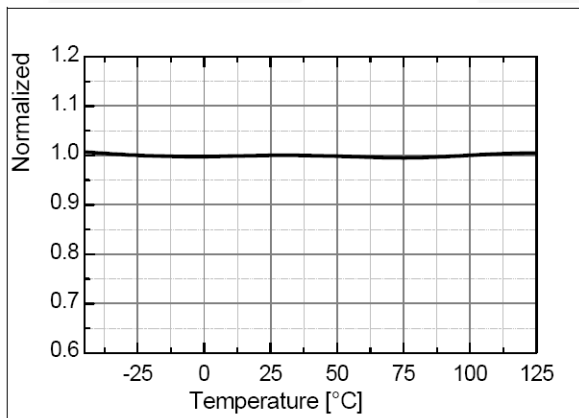
## Typical Performance Characteristics



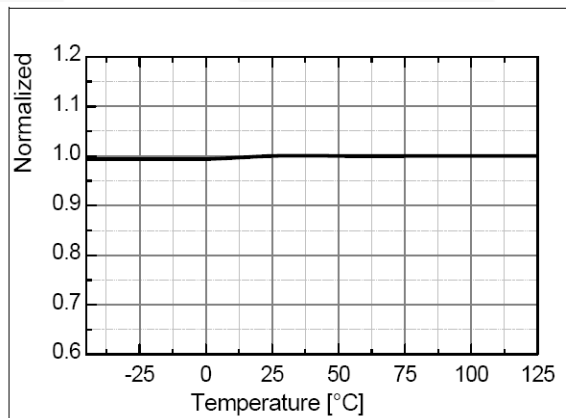
**Figure 10. Zero Duty Cycle Output Voltage ( $V_{EA2}$ ) vs.  $T_A$**



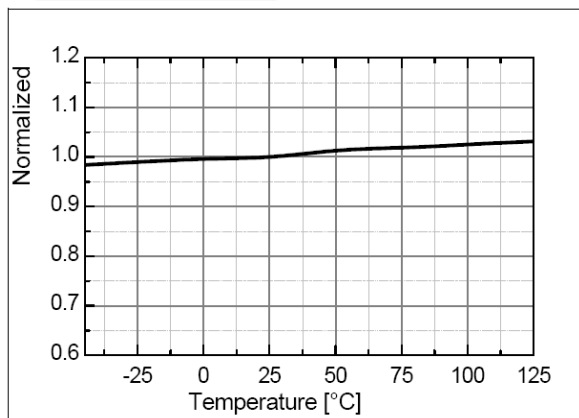
**Figure 11. Maximum On-Time Program 1 ( $t_{ON,MAX1}$ ) vs.  $T_A$**



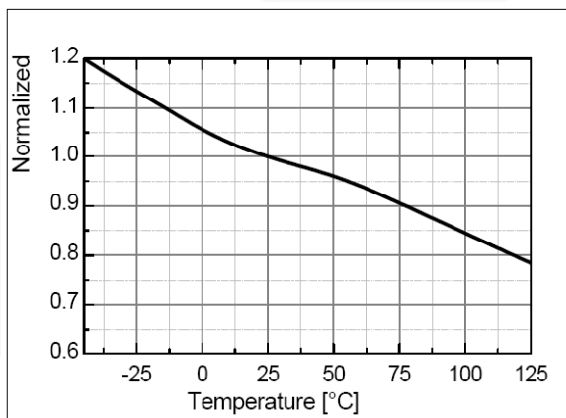
**Figure 12. Maximum On-Time Program 2 ( $t_{ON,MAX2}$ ) vs.  $T_A$**



**Figure 13. Current-Sense Input Threshold Voltage Limit ( $V_{CS}$ ) vs.  $T_A$**



**Figure 14. Input High Clamp Voltage ( $V_{CLAMPH}$ ) vs.  $T_A$**



**Figure 15. Input Low Clamp Voltage ( $V_{CLAMP_L}$ ) vs.  $T_A$**

Typical Performance Characteristics

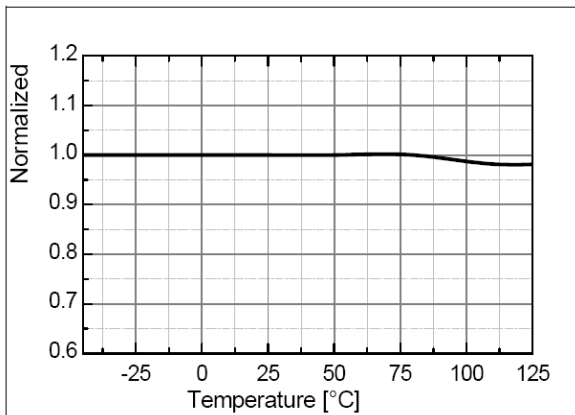


Figure 16. Output Voltage High (V<sub>OH</sub>) vs. T<sub>A</sub>

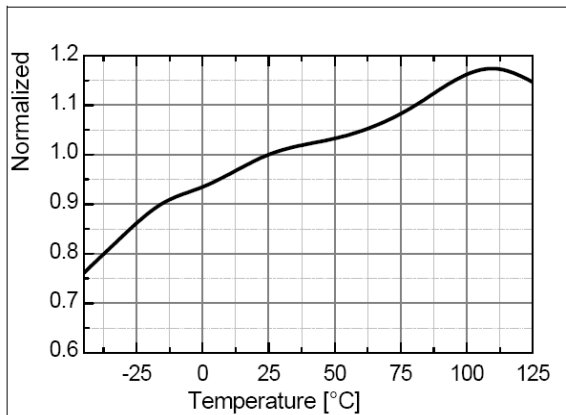


Figure 17. Output Voltage Low (V<sub>OL</sub>) vs. T<sub>A</sub>

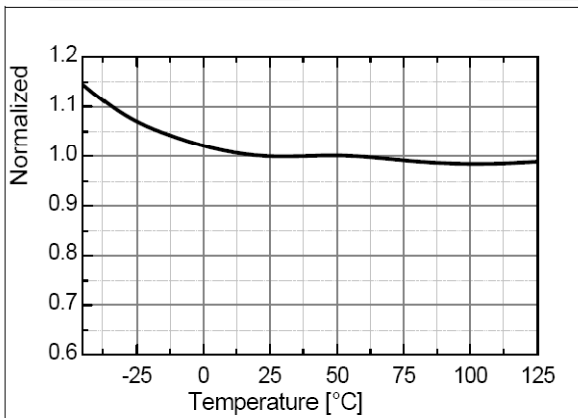


Figure 18. Restart Timer Delay (t<sub>RST</sub>) vs. T<sub>A</sub>

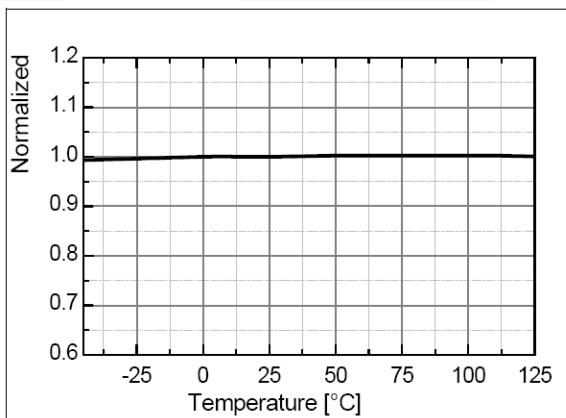


Figure 19. Output Ready Voltage (V<sub>RDY</sub>) vs. T<sub>A</sub>

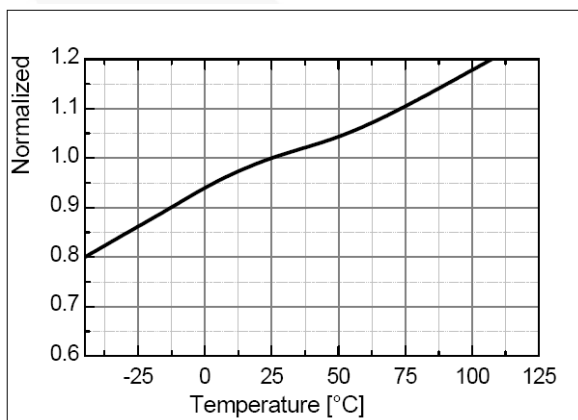


Figure 20. Output Saturation Voltage (V<sub>RDY,SAT</sub>) vs. T<sub>A</sub>

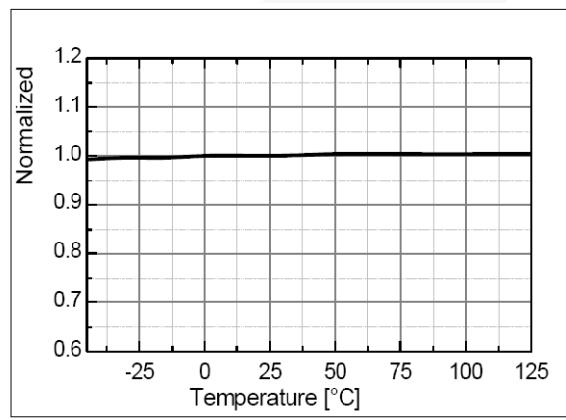


Figure 21. OVP Threshold Voltage (V<sub>OVP</sub>) vs. T<sub>A</sub>

## Applications Information

**1. Startup:** Normally, supply voltage ( $V_{CC}$ ) of a PFC block is fed from the additional power supply, which can be called standby power. Without this standby power, auxiliary winding for zero current detection can be used as a supply source. Once the supply voltage of the PFC block exceeds 12V, internal operation is enabled until the voltage drops to 8.5V. If  $V_{CC}$  exceeds  $V_Z$ , 20mA current is sinking from  $V_{CC}$ .

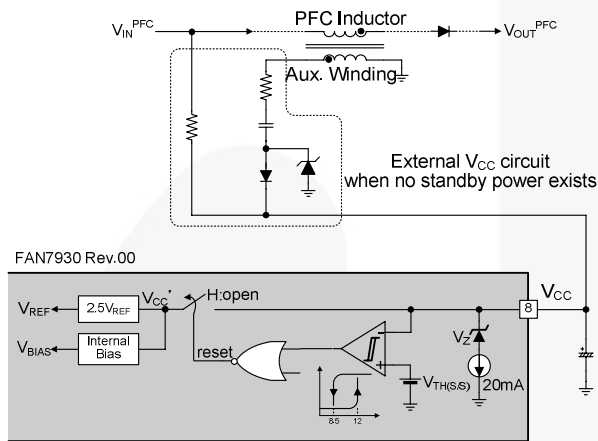


Figure 22. Startup Circuit

**2. INV Block:** Scaled-down voltage from the output is the input for the INV pin. Many functions are embedded based on the INV pin: transconductance amplifier, output OVP comparator, disable comparator, and output UVLO comparator.

For the output voltage control, a transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage-controlled current source) aids the implementation of the OVP and disable functions. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. To cancel down the line input voltage effect on power factor correction, the effective control response of the PFC block should be slower than the line frequency and this conflicts with the transient response of controller. Two-pole one-zero type compensation may be used to meet both requirements.

The OVP comparator shuts down the output drive block when the voltage of the INV pin is higher than 2.675V and there is 0.175V hysteresis. The disable comparator disables operation when the voltage of the inverting input is lower than 0.35V and there is 100mV hysteresis. An external small-signal MOSFET can be used to disable the IC, as shown in Figure 23. The IC operating current decreases to reduce power consumption if the IC is disabled. **Error! Reference source not found.** is the timing chart of the internal circuit near the INV pin when rated PFC output voltage is 390V<sub>DC</sub> and  $V_{CC}$  supply voltage is 15V.

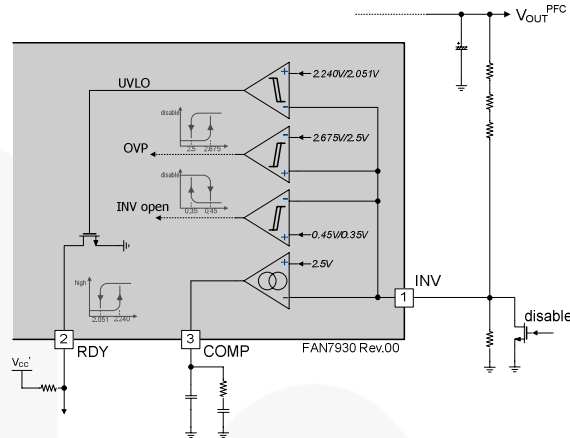


Figure 23. Circuit Around INV Pin

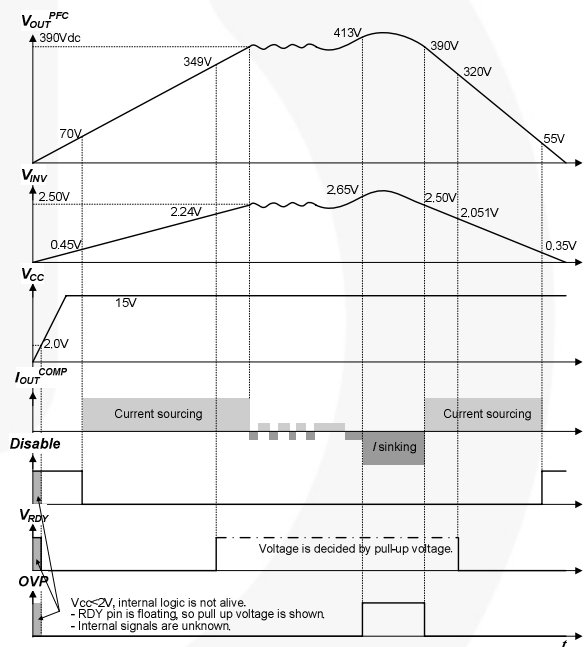
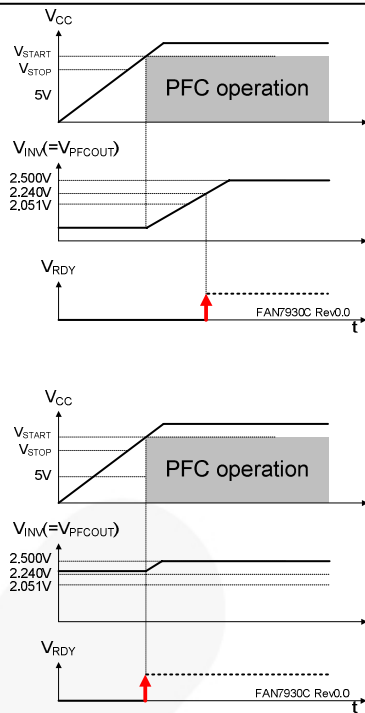
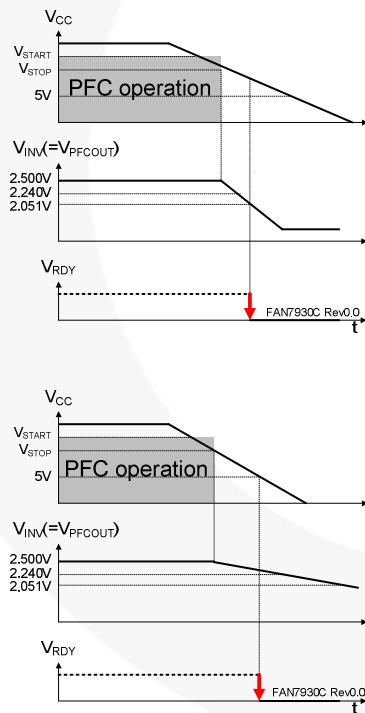


Figure 24. Timing Chart for INV Block

**3. RDY Output:** When the INV voltage is higher than 2.24V, RDY output is triggered HIGH and lasts until the INV voltage is lower than 2.051V. When input AC voltage is quite high, for example 240V<sub>AC</sub>, PFC output voltage is always higher than RDY threshold, regardless of boost converter operation. In this case, the INV voltage is already higher than 2.24V before PFC  $V_{CC}$  touches  $V_{START}$ ; however, RDY output is not triggered to HIGH until  $V_{CC}$  touches  $V_{START}$ . After boost converter operation stops, RDY is not pulled LOW because the INV voltage is higher than the RDY threshold. When  $V_{CC}$  of the PFC drops below 5V, RDY is pulled LOW even though PFC output voltage is higher than threshold. The RDY pin output is open drain, so needs an external pull-up resistor to supply the proper power source. The RDY pin output remains floating until  $V_{CC}$  is higher than 2V.



**Figure 25. Two Cases of RDY Triggered HIGH**



**Figure 26. Two Cases of RDY Triggered LOW**

**4. Zero-Current Detection:** Zero-current detection (ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. When the power switch turns on, negative voltage is induced at the auxiliary winding due to the opposite winding direction

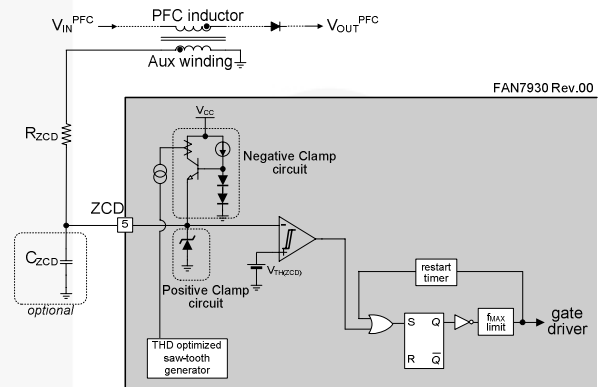
(see Equation 1). Positive voltage is induced (see Equation 2) when the power switch turns off.

$$V_{AUX} = -\frac{T_{AUX}}{T_{IND}} \cdot V_{AC} \quad (1)$$

$$V_{AUX} = \frac{T_{AUX}}{T_{IND}} \cdot (V_{PFCOUT} - V_{AC}) \quad (2)$$

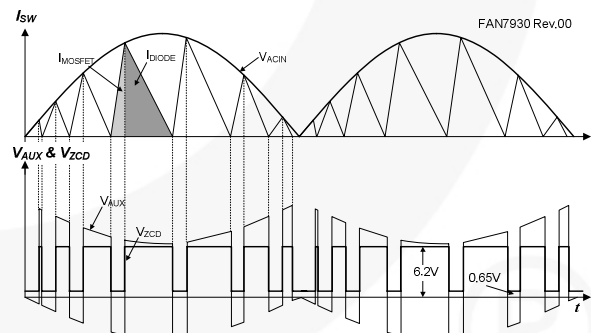
where:

- $V_{AUX}$  is the auxiliary winding voltage;
- $T_{IND}$  is boost inductor turns;
- $T_{AUX}$  auxiliary winding turns;
- $V_{AC}$  is input voltage for PFC converter; and
- $V_{OUT\_PFC}$  is output voltage from the PFC converter.



**Figure 27. Circuit Near ZCD**

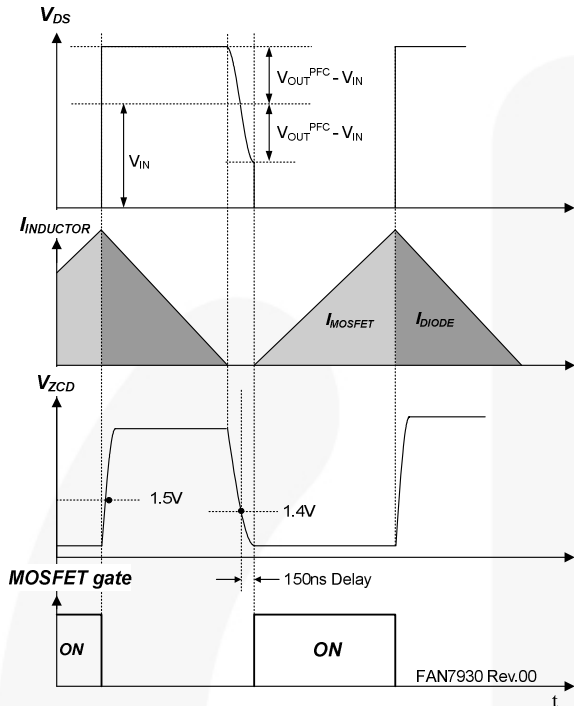
Because auxiliary winding voltage can swing from negative to positive voltage, the internal block in ZCD pin has both positive and negative voltage clamping circuits. When the auxiliary voltage is negative, internal circuit clamps the negative voltage at the ZCD pin around 0.65V by sourcing current to the serial resistor between the ZCD pin and the auxiliary winding. When the auxiliary voltage is higher than 6.5V, current is sunk through a resistor from the auxiliary winding to the ZCD pin.



**Figure 28. Auxiliary Voltage Depends on MOSFET Switching**

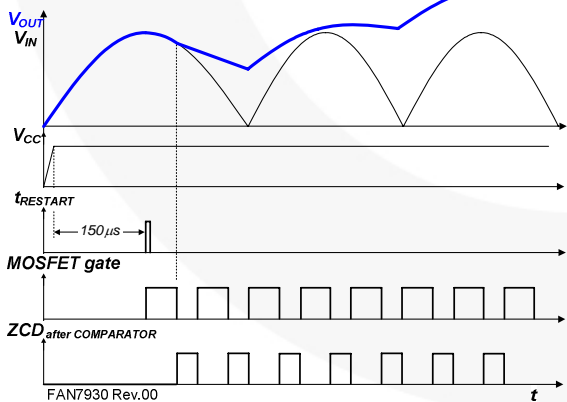
The auxiliary winding voltage is used to check the boost inductor current zero instance. When boost inductor current becomes zero, there is a resonance between boost inductor and all capacitors at the MOSFET drain pin: including  $C_{OSS}$  of the MOSFET; an external capacitor at the D-S pin to reduce the voltage rising and falling slope of the MOSFET; a parasitic capacitor at inductor; and so on to improve performance. Resonated voltage is reflected to the auxiliary winding and can be used for detecting zero current of boost inductor and

valley position of MOSFET voltage stress. For valley detection, a minor delay by the resistor and capacitor is needed. A capacitor increases the noise immunity at the ZCD pin. If ZCD voltage is higher than 1.5V, an internal ZCD comparator output becomes HIGH and LOW when the ZCD goes below 1.4V. At the falling edge of comparator output, internal logic turns on the MOSFET.



**Figure 29. Auxiliary Voltage Threshold**

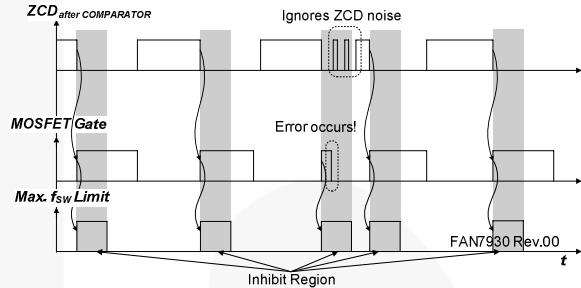
When no ZCD signal is available, the PFC controller cannot turn on the MOSFET, so the controller checks every switching off time and forces MOSFET turn on when the off time is longer than 150μs. This is called the restart timer, which triggers MOSFET turn-on at startup and may be used at the input voltage zero-cross period.



**Figure 30. Restart Timer at Startup**

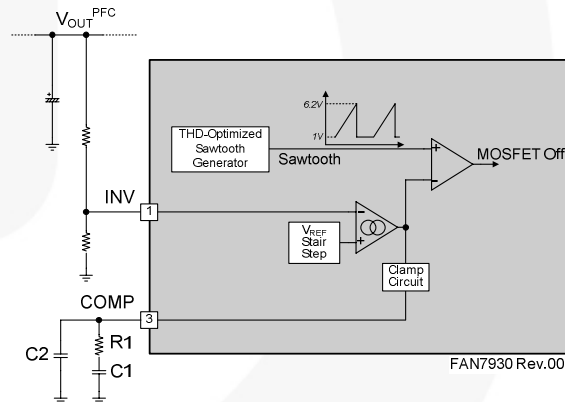
Because the MOSFET turn-on depends on the ZCD input, switching frequency may increase to higher than several megahertz due to the miss-triggering or noise on the nearby ZCD pin. If the switching frequency is higher than needed for critical conduction mode (CRM), operation mode shifts to continuous conduction mode (CCM). In CCM, unlike CRM where the boost inductor

current is reset to zero at the next switch on; inductor current builds up at every switching cycle and can be raised to very high current that exceeds the current rating of the power switch or diode. This can seriously damage the power switch and result in burn down. To avoid this, maximum switching frequency limitation is embedded. If ZCD signal is applied again within 3.3μs after the previous rising edge of gate signal, this signal is ignored internally and FAN7930C waits for another ZCD signal. This slightly degrades the power factor performance at light load and high input voltage.



**Figure 31. Maximum Switching Frequency Limit Operation**

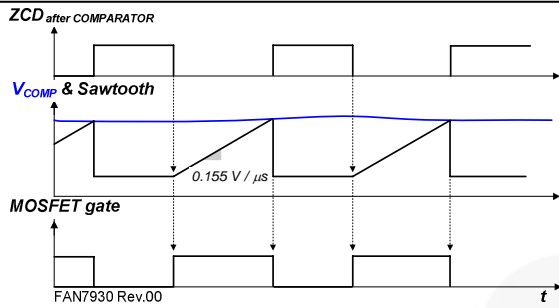
**5. Control:** The scaled output is compared with the internal reference voltage and sinking or sourcing current is generated from the COMP pin by the transconductance amplifier. The error amplifier output is compared with the internal sawtooth waveform to give proper turn-on time based on the controller.



**Figure 32. Control Circuit**

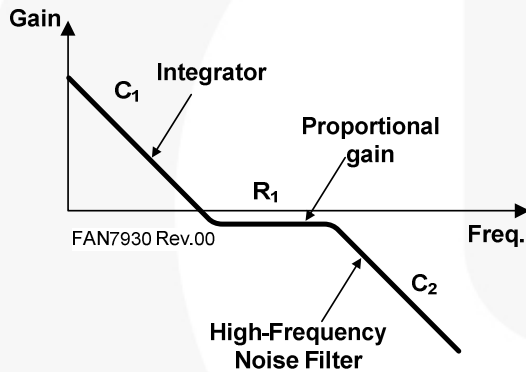
Unlike a conventional voltage-mode PWM controller, FAN7930C turns on the MOSFET at the falling edge of ZCD signal. On-instance is determined by the external signal and the turn-on time lasts until the error amplifier output ( $V_{COMP}$ ) and sawtooth waveform meet. When load is heavy, output voltage decreases, scaled output decreases, COMP voltage increases to compensate low output, turn-on time lengthens to give more inductor turn-on time, and increased inductor current raises the output voltage. This is how PFC negative feedback controller regulates output.

The maximum of  $V_{COMP}$  is limited to 6.5V, which dictates the maximum turn-on time, and switching stops when  $V_{COMP}$  is lower than 1.0V.



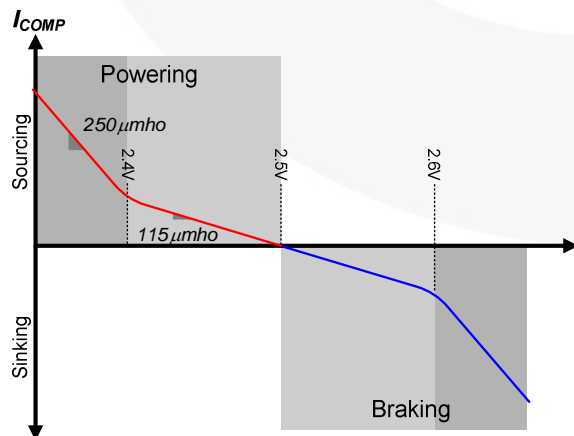
**Figure 33. Turn-On Time Determination**

The roles of PFC controller are regulating output voltage and input current shaping to increase power factor. Duty control based on the output voltage should be fast enough to compensate output voltage dip or overshoot. For the power factor, however, the control loop must not react to the fluctuating AC input voltage. These two requirements conflict; therefore, when designing a feedback loop, the feedback loop should be least 10 times slower than AC line frequency. That slow response is made by C1 at compensator. R1 makes gain boost around operation region and C2 attenuates gain at higher frequency. Boost gain by R1 helps raise the response time and improves phase margin.



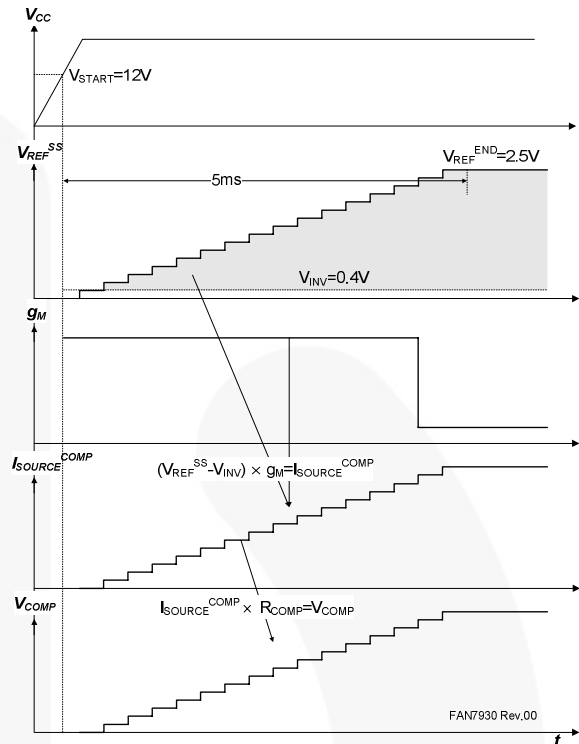
**Figure 34. Compensators Gain Curve**

For the transconductance error amplifier side, gain changes based on differential input. When the error is large, gain is large to make the output dip or peak to suppress quickly. When the error is small, low gain is used to improve power factor performance.



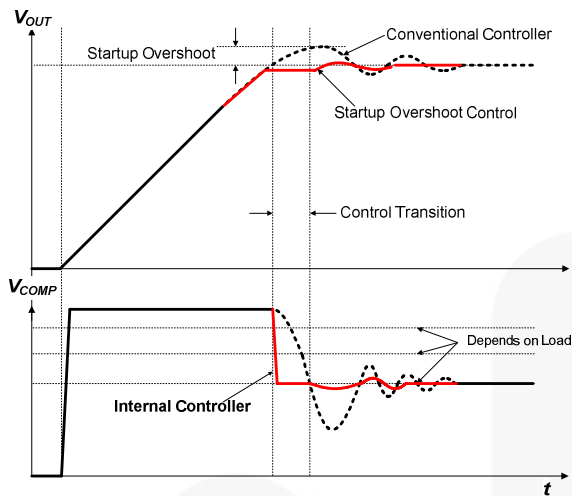
**Figure 35. Gain Characteristic**

**6. Soft-Start:** When  $V_{CC}$  reaches  $V_{START}$ , the internal reference voltage is increased like a stair step for 5ms. As a result,  $V_{COMP}$  is also raised gradually and MOSFET turn-on time increases smoothly. This reduces voltage and current stress on the power switch during startup.



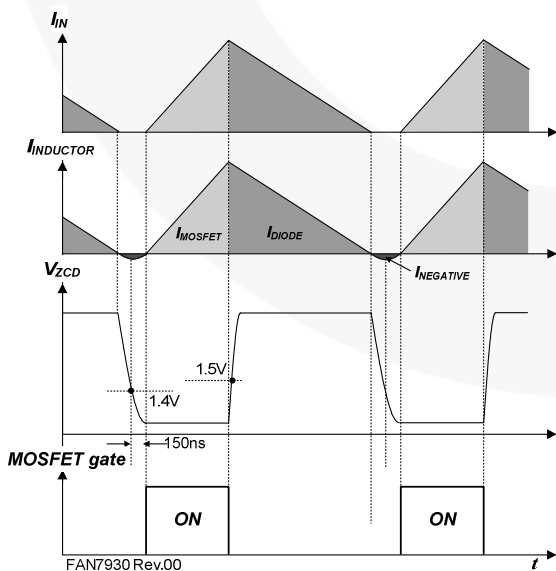
**Figure 36. Soft-Start Sequence**

**7. Startup without Overshoot:** Feedback control speed of PFC is quite slow. Due to the slow response, there is a gap between output voltage and feedback control. That is why over-voltage protection (OVP) is critical at the PFC controller and voltage dip caused by fast load changes from light to heavy is diminished by a bulk capacitor. OVP is easily triggered at startup phase. Operation on and off by OVP at startup may cause audible noise and can increase voltage stress at startup, which is normally higher than in normal operation. This operation is better when soft-start time is very long. However, too much startup time enlarges the output voltage building time at light load. FAN7930C has overshoot avoidance at startup. During startup, the feedback loop is controlled by an internal proportional gain controller and, when the output voltage reaches the rated value, it switches to an external compensator after a transition time of 30ms. This internal proportional gain controller eliminates overshoot at startup and an external conventional compensator takes over successfully afterward.

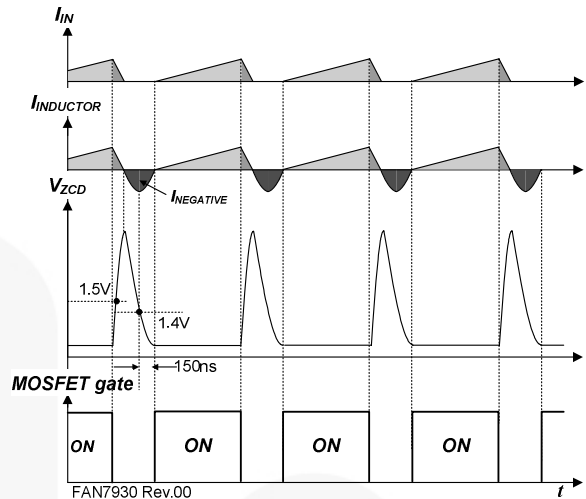


**Figure 37. Startup Control without Overshoot**

**8. THD Optimization:** Total Harmonic Distortion (THD) is the factor that dictates how closely input current shape matches sinusoidal form. The turn-on time of the PFC controller is almost constant over one AC line period due to the extremely low feedback control response. The turn-off time is determined by the current decrease slope of the boost inductor made by the input voltage and output voltage. Once inductor current becomes zero, resonance between  $C_{OSS}$  and the boost inductor makes oscillating waveforms at the drain pin and auxiliary winding. By checking the auxiliary winding voltage through the ZCD pin, the controller can check the zero current of boost inductor. At the same time, a minor delay is inserted to determine the valley position of drain voltage. The input and output voltage difference is at its maximum at the zero cross point of AC input voltage. The current decrease slope is steep near the zero cross region and more negative inductor current flows during a drain voltage valley detection time. Such a negative inductor current cancels down the positive current flows and input current becomes zero, called “zero-cross distortion” in PFC.

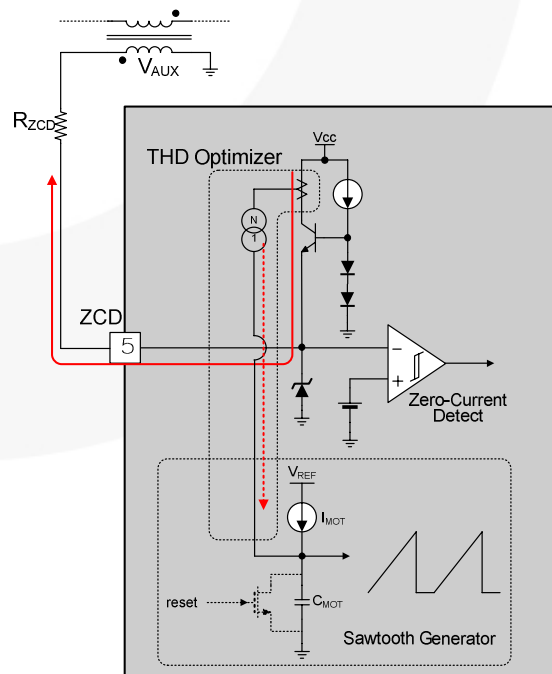


**Figure 38. Input and Output Current Near Input Voltage Peak**

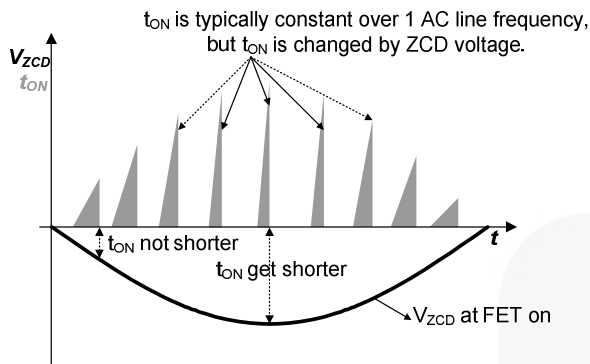


**Figure 39. Input and Output Current Near Input Voltage Peak Zero Cross**

To improve this, lengthened turn-on time near the zero cross region is a well-known technique, though the method may vary and may be proprietary. FAN7930C optimizes this by sourcing current through the ZCD pin. Auxiliary winding voltage becomes negative when the MOSFET turns on and is proportional to input voltage. The negative clamping circuit of ZCD outputs the current to maintain the ZCD voltage at a fixed value. The sourcing current from the ZCD is directly proportional to the input voltage. Some portion of this current is applied to the internal sawtooth generator, together with a fixed-current source. Theoretically, the fixed-current source and the capacitor at sawtooth generator determine the maximum turn-on time when no current is sourcing at ZCD clamp circuit and available turn-on time gets shorter proportional to the ZCD sourcing current.



**Figure 40. Circuit of THD Optimizer**



**Figure 41. Effect of THD Optimizer**

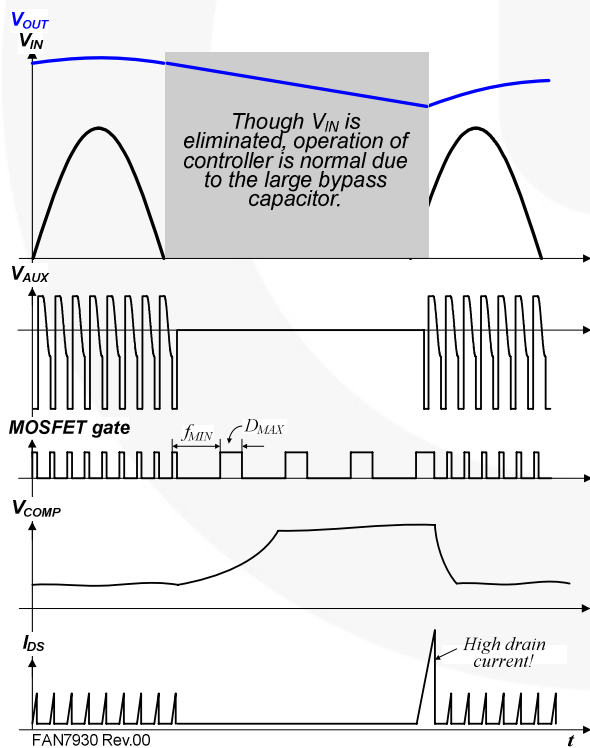
By THD optimizer, turn-on time over one AC line period is proportionally changed, depending on input voltage. Near zero cross, lengthened turn-on time improves THD performance.

**9.  $V_{IN}$  Absent Detection:** To save power loss caused by input voltage sensing resistors and to optimize THD, the FAN7930C omits AC input voltage detection. Therefore, no information about AC input is available from the internal controller. In many cases, the  $V_{CC}$  of PFC controller is supplied by a independent power source, like standby power. In this scheme, some mismatch may exist. For example, when the electric power is

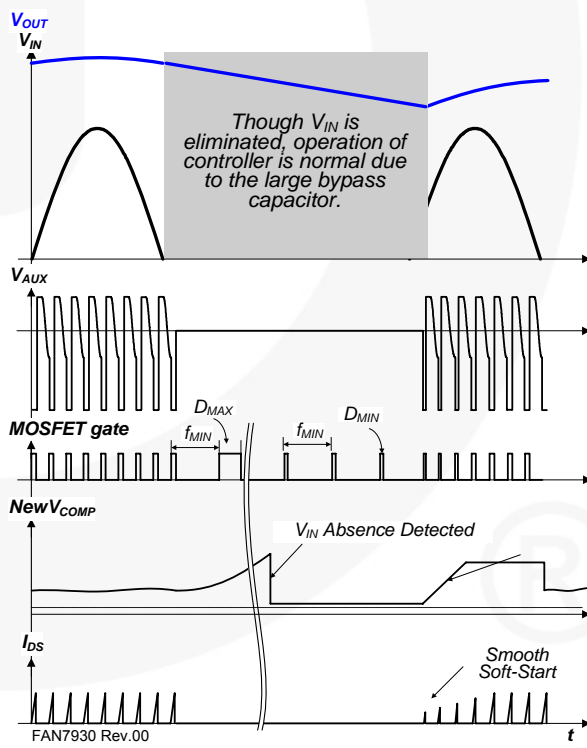
suddenly interrupted during two or three AC line periods;  $V_{CC}$  is still live during that time, but output voltage drops because there is no input power source. Consequently, the control loop tries to compensate for the output voltage drop and  $V_{COMP}$  reaches its maximum. This lasts until AC input voltage is live again. When AC input voltage is live again, high  $V_{COMP}$  allows high switching current and more stress is put on the MOSFET and diode. To protect against this, FAN7930C checks if the input AC voltage exists. If input does not exist, soft-start is reset and waits until AC input is live again. Soft-start manages the turn-on time for smooth operation when it detects AC input is applied again and applies less voltage and current stress on startup.

**10. Current Sense:** The MOSFET current is sensed using an external sensing resistor for over-current protection. If the CS pin voltage is higher than 0.8V, the over-current protection comparator generates a protection signal. An internal RC filter of 40kΩ and 8pF is included to filter switching noise.

**11. Gate Driver Output:** FAN7930C contains a single totem-pole output stage designed for a direct drive of the power MOSFET. The drive output is capable of up to +500/-800mA peak current with a typical rise and fall time of 50ns with 1nF load. The output voltage is clamped to 13V to protect the MOSFET gate even if the  $V_{CC}$  voltage is higher than 13V.



**Figure 42. Operation without  $V_{IN}$  Absent Circuit**



**Figure 43. Operation with  $V_{IN}$  Absent Circuit**



## PCB Layout Guide

PFC block normally handles high switching current and the voltage low energy signal path can be affected by the high energy path. Cautious PCB layout is mandatory for stable operation.

1. The gate drive path should be as short as possible. The closed-loop that runs from the gate driver, MOSFET gate, and MOSFET source to ground of PFC controller should be as close as possible. This is also crossing point between power ground and signal ground. Power ground path from the bridge diode to the output bulk capacitor should be short and wide. The sharing position between power ground and signal ground should be only at one position to avoid ground loop noise. Signal path of PFC controller should be short and wide for external components to contact.
2. PFC output voltage sensing resistor is normally high to reduce current consumption. This path can be affected by external noise. To reduce noise potential at the INV pin, a shorter path for output sensing is recommended. If a shorter path is not possible, place some dividing resistors between PFC output and the INV pin — closer to the INV pin is better. Relative high voltage close to the INV pin can be helpful.
3. ZCD path is recommended close to auxiliary winding from boost inductor and to the ZCD pin. If that is difficult, place a small capacitor (below 50pF) to reduce noise.
4. The switching current sense path should not share with another path to avoid interference. Some additional components may be needed to reduce the noise level applied to the CS pin.

5. A stabilizing capacitor for  $V_{CC}$  is recommended as close as possible to the  $V_{CC}$  and ground pins. If it is difficult, place the SMD capacitor as close to the corresponding pins as possible.

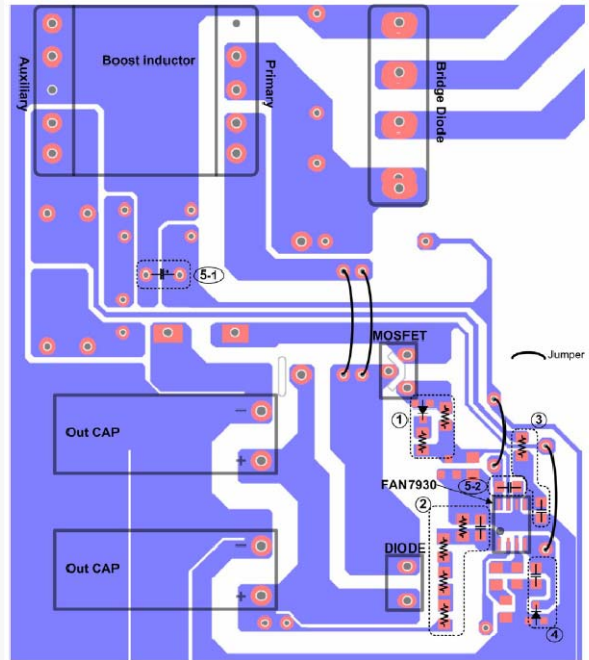


Figure 44. Recommended PCB Layout



## 2. Transformer

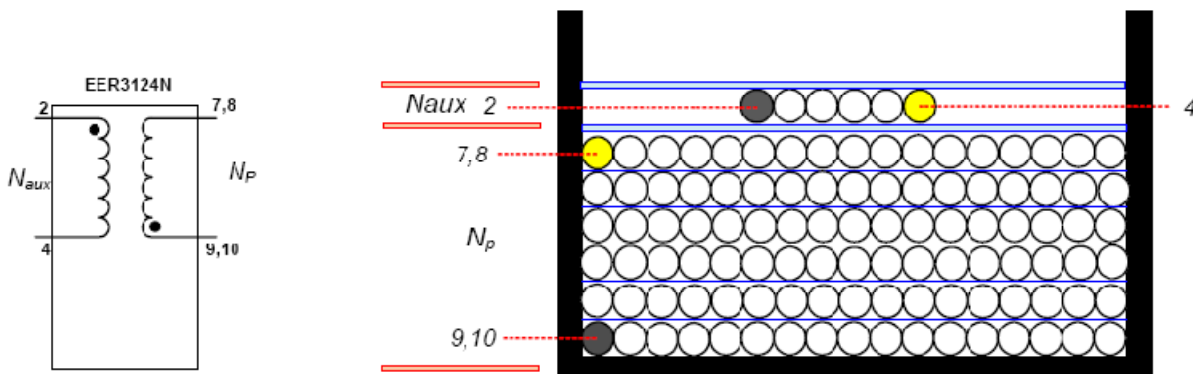


Figure 46. Transformer Schematic Diagram

## 3. Winding Specification

| Position | No   | Pin (S → F)  | Wire    | Turns | Winding Method   | Barrier Tape |     |    |
|----------|--|--------------|---------|-------|------------------|--------------|-----|----|
|          |  |              |         |       |                  | TOP          | BOT | Ts |
| Bottom   | N <sub>p</sub>                                   | 9, 10 → 7, 8 | 0.1φ×50 | 49    | Solenoid Winding |              |     | 1  |
|          | Insulation: Polyester Tape t = 0.025mm, 3 Layers |              |         |       |                  |              |     |    |
| Top      | N <sub>AUX</sub>                                 | 2 → 4        | 0.3φ    | 6     | Solenoid Winding |              |     |    |
|          | Insulation: Polyester Tape t = 0.025mm, 4 Layers |              |         |       |                  |              |     |    |

## 4. Electrical Characteristics

|            | Pin          | Specification | Remark     |
|------------|--------------|---------------|------------|
| Inductance | 9, 10 → 7, 8 | 230μH ±7%     | 100kHz, 1V |

## 5. Core & Bobbin

Core: EER3124, Samhwa (PL-7) (Ae=97.9mm<sup>2</sup>)

Bobbin: EER3124

## 6. Bill of Materials

| Part #           | Value                    | Note                   | Part #              | Value     | Note  |
|------------------|--------------------------|------------------------|---------------------|-----------|---|
| <b>Resister</b>  |                          |                        | <b>Switch</b>       |           |   |
| R101             | 1M $\Omega$              | 1W                     | Q101                | FCPF20N60 | 20A, 600V, SuperFET                                 |
| R102             | 330k $\Omega$            | 1/2W                   | <b>Diode</b>        |           |   |
| R103             | 10k $\Omega$             | 1W                     | D101                | 1N4746    | 1W, 18V, Zener Diode                                |
| R104             | 30k $\Omega$             | 1/4W                   | D102                | UF4004    | 1A, 400V Glass Passivated High-Efficiency Rectifier |
| R107             | 10k $\Omega$             | 1/4W                   | D103                | 1N4148    | 1A, 100V Small-Signal Diode                         |
| R108             | 4.7k $\Omega$            | 1/4W                   | D104                | 1N4148    | 1A, 100V Small-Signal Diode                         |
| R109             | 47k $\Omega$             | 1/4W                   | D105                |           | 8A, 600V, General-Purpose Rectifier                 |
| R110             | 10k $\Omega$             | 1/4W                   | D106                |           | 3A, 600V, General-Purpose Rectifier                 |
| R111             | 0.80k $\Omega$           | 5W                     |                     |           |   |
| R112, 113, 114   | 3.9k $\Omega$            | 1/4W                   | IC101               | FAN7930C  | CRM PFC Controller                                  |
| R115             | 75k $\Omega$             | 1/4W                   |                     |           |   |
| <b>Capacitor</b> |                          |                        | <b>Fuse</b>         |           |   |
| C101             | 220nF/275V <sub>AC</sub> | Box Capacitor          | FS101               | 5A/250V   |   |
| C102             | 680nF/275V <sub>AC</sub> | Box Capacitor          | <b>NTC</b>          |           |   |
| C103             | 0.68 $\mu$ F/630V        | Box Capacitor          | TH101               | 5D-15     |   |
| C104             | 12nF/50V                 | Ceramic Capacitor      | <b>Bridge Diode</b> |           |   |
| C105             | 100nF/50V                | SMD (1206)             | BD101               |           | 15A, 600V   |
| C107             | 33 $\mu$ F/50V           | Electrolytic Capacitor | <b>Line Filter</b>  |           |   |
| C108             | 220nF/50V                | Ceramic Capacitor      | LF101               | 23mH      |   |
| C109             | 47nF/50V                 | Ceramic Capacitor      | <b>Transformer</b>  |           |   |
| C110             | 1nF/50V                  | Ceramic Capacitor      | T1                  | EER3124   | Ae=97.9mm <sup>2</sup>                              |
| C112             | 47nF/50V                 | Ceramic Capacitor      | <b>ZNR</b>          |           |   |
| C111             | 220 $\mu$ F/450V         | Electrolytic Capacitor | ZNR101              | 10D471    |   |
| C114             | 2.2nF/450V               | Box Capacitor          |                     |           |   |
| C115             | 2.2nF/450V               | Box Capacitor          |                     |           |   |

Physical Dimensions

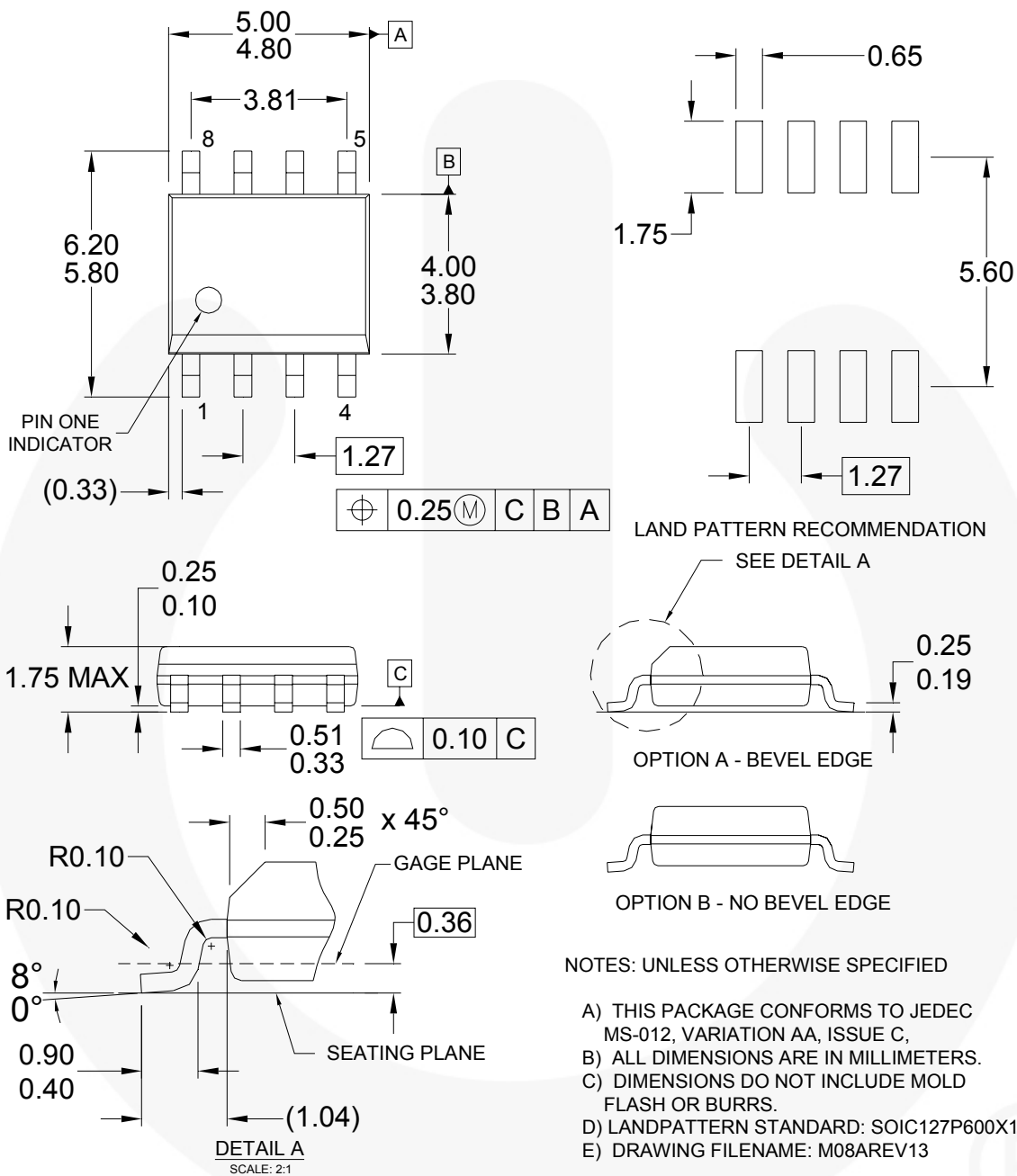


Figure 47. 8-Lead Small Outline Package (SOP)


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FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

### PRODUCT STATUS DEFINITIONS

#### Definition of Terms

| Datasheet Identification | Product Status        | Definition  |
|--------------------------|-----------------------|---|
| Advance Information      | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.   |
| Preliminary              | First Production      | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production       | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.   |
| Obsolete                 | Not In Production     | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.  |

Rev. I50