FAN8004

5-CH Motor Driver

Features

- 4-CH Balanced Transformerless (BTL) Driver
- 1-CH (Forward Reverse) Control DC Motor Driver
- Operating Supply Voltage (4.5V ~ 13.2V)
- Built-in Thermal Shut Down Circuit (TSD)
- Built-in Under Voltage Lockout Circuit (UVLO)
- Built-in Over Voltage Protection Circuit (OVP)
- Built-in Mute Circuit (CH1, CH2, CH3 and CH4)
- Built-in Normal OP-AMP
- Built-in 5V Regulator With Reset

Description

The FAN8004 is a monolithic integrated circuit suitable for a 5-CH motor driver which drives the tracking actuator, focus actuator, sled motor, spindle motor, and tray motor of the CDP/DVDP/MDP system.

48-QFP-1010E

Typical Applications

- Compact Disc Player
- Mini Disc Player
- Digital Video Disk Player

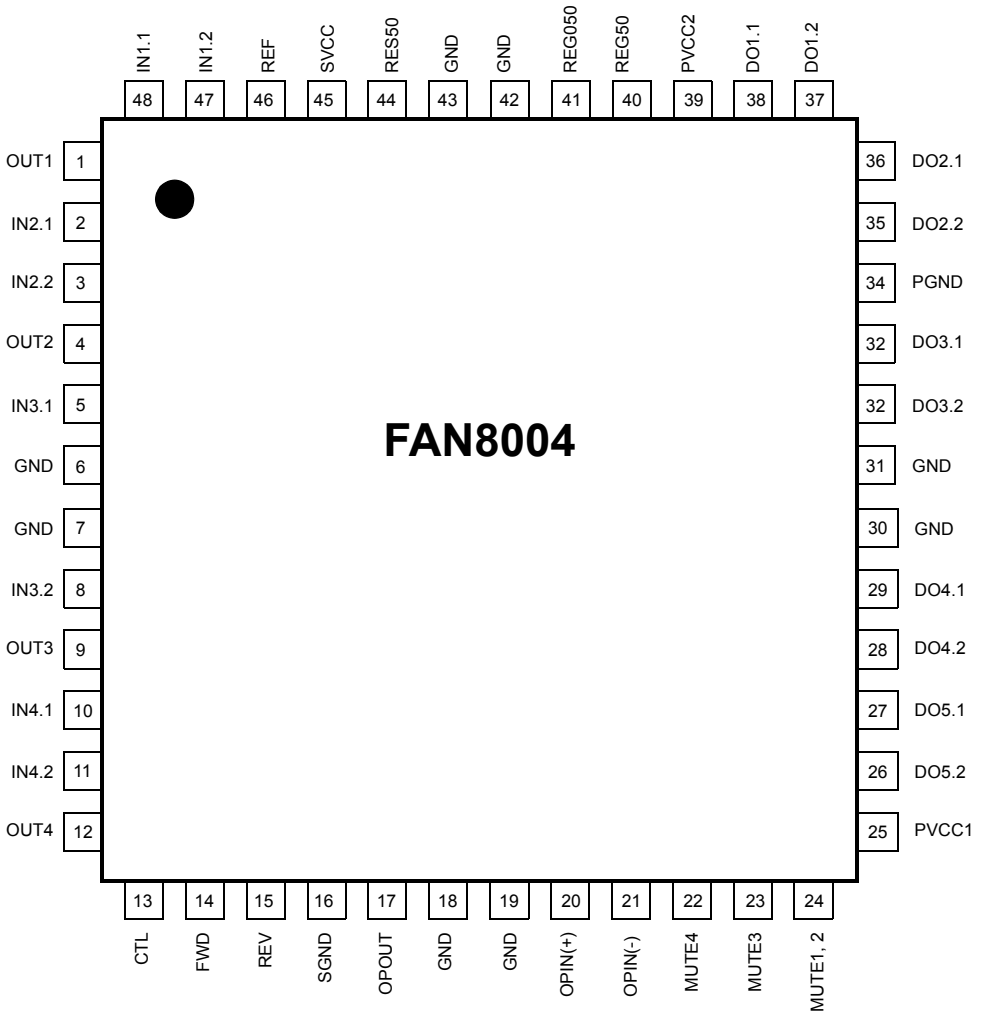
Ordering Information

Device	Package	Operating Temp.
FAN8004	48-QFP-1010E	-35°C ~ +85°C
FAN8004_NL[note1]	48-QFP-1010E	-35°C ~ +85°C

Notes:

1. NL: Lead-free type

Pin Assignments



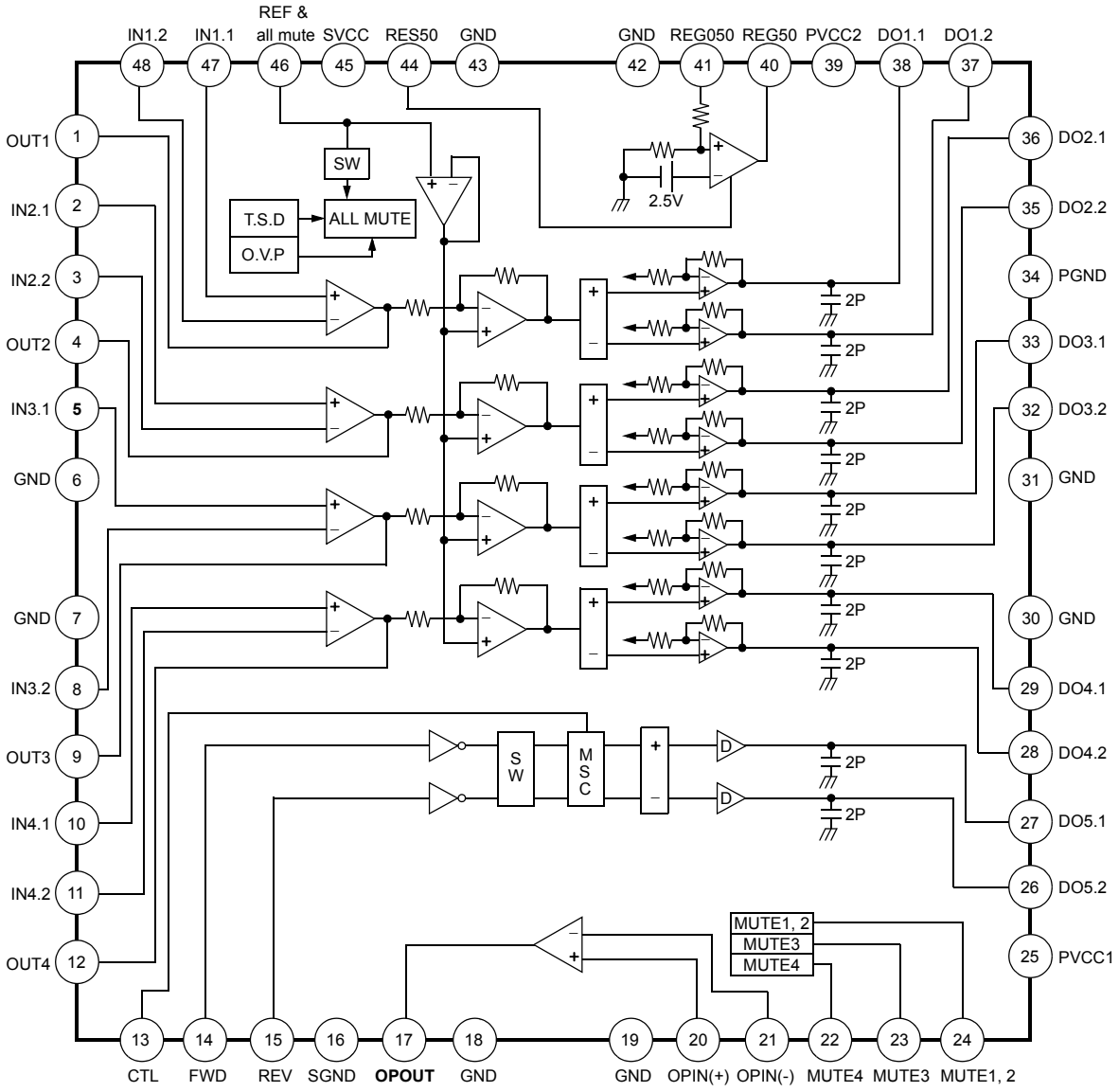
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	OUT1	O	CH 1 OP-AMP Output
2	IN2.1	I	CH 1 OP-AMP Input (+)
3	IN2.2	I	CH 2 OP-AMP Input (-)
4	OUT2	O	CH 2 OP-AMP Output
5	IN3.1	I	CH 3 OP-AMP Input (+)
6	GND	-	Ground
7	GND	-	Ground
8	IN3.2	I	CH 3 OP-AMP Input (-)
9	OUT3	O	CH 3 OP-AMP Output
10	IN4.1	I	CH 4 OP-AMP Input (+)
11	IN4.2	I	CH 4 OP-AMP Input (-)
12	OUT4	O	CH 4 OP-AMP output
13	CTL	I	CH 5 Motor Speed Control
14	FWD1	I	CH 5 Forward Input
15	REW1	I	CH 5 Reverse Input
16	SGND	-	Signal Ground
17	OPOUT	O	Opamp Output
18	GND	-	Ground
19	GND	-	Ground
20	OPIN(+)	I	OP-AMP Input (+)
21	OPIN(-)	I	OP-AMP Input (-)
22	MUTE4	I	CH 4 Mute
23	MUTE3	I	CH 3 Mute
24	MUTE1, 2	I	CH 1, CH 2 Mute
25	PVCC1	-	Power Supply Voltage (For CH 5)
26	DO5.2	O	CH 5 Drive Output
27	DO5.1	O	CH 5 Drive Output
28	DO4.2	O	CH 4 Drive Output
29	DO4.1	O	CH 4 Drive Output
30	GND	-	Ground
31	GND	-	Ground
32	DO3.2	O	CH 3 Drive Output
33	DO3.1	O	CH 3 Drive Output
34	PGND	-	Power Ground
35	DO2.2	O	CH 2 Drive Output
36	DO2.1	O	CH 2 Drive Output
37	DO1.2	O	CH 1 Drive Output
38	DO1.1	O	CH 1 Drive Output
39	PVCC2	-	Power Supply Voltage (For CH 1, CH 2, CH 3, CH 4)

Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Description
40	REG50	O	Regulator Output
41	REG050	O	Regulator 5V Output
42	GND	-	Ground
43	GND	-	Ground
44	RES50	I	Regulator Reset
45	SVCC	-	Signal Supply Voltage
46	REF	I	Bias Voltage Input
47	IN1.1	I	CH 1 OP-AMP Input (+)
48	IN1.2	I	CH 1 OP-AMP Input (-)

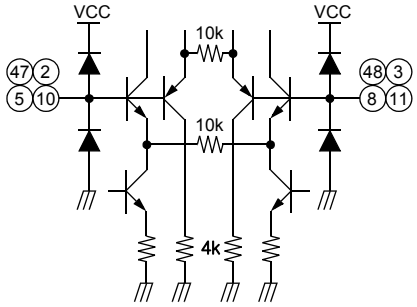
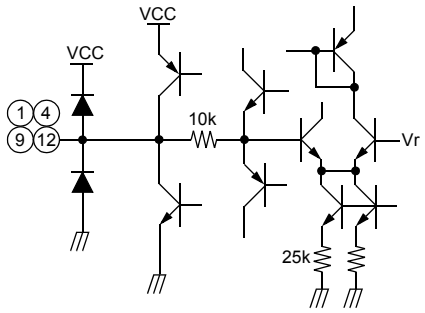
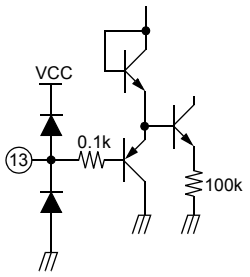
Internal Block Diagram



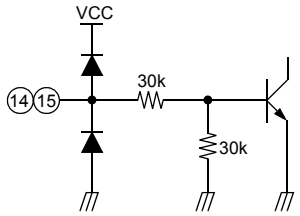
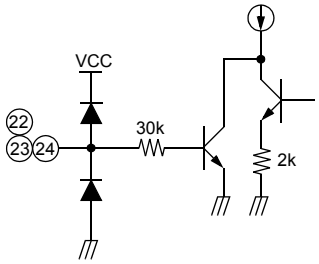
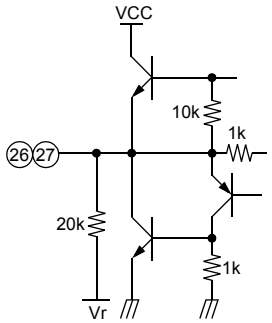
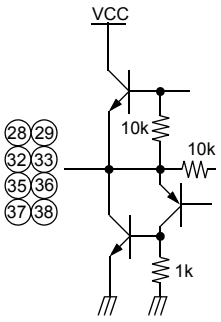
Note:

1. SW = Logic switch
2. MSC = Motor speed control
3. D = Output driver

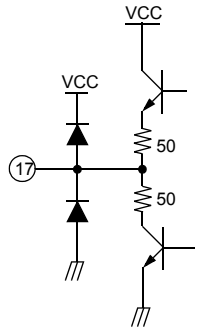
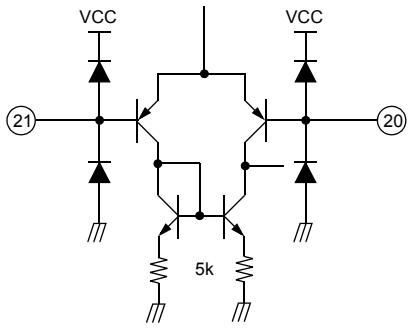
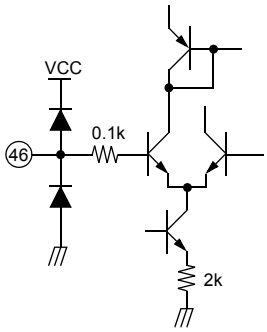
Equivalent Circuits

Description	Pin No.	Internal Circuit
Input OPIN (+) OPIN (–)	47, 2, 5, 10 48, 3, 8. 11	
INPUT OPOUT	1, 4, 9, 12	
CTL	13	

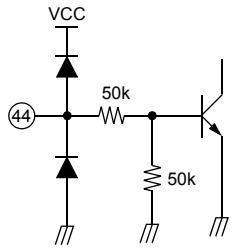
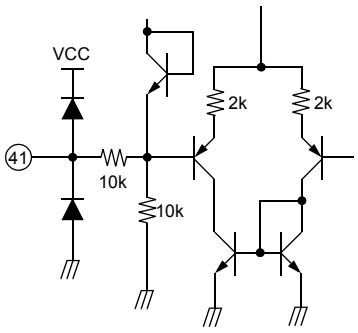
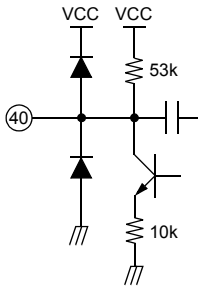
Equivalent Circuits (Continued)

Description	Pin No.	Internal Circuit
Logic Drive FWD Input REV Input	14 15	
CH Mute	22, 23, 24	
Logic Drive Output	26, 27	
4-CH Drive Output	28, 29 32, 33 35, 36 37, 38	

Equivalent Circuits (Continued)

Description	Pin No.	Internal Circuit
Normal OPOUT	17	
Normal OPIN(+) OPIN(-)	20 21	
Ref	46	

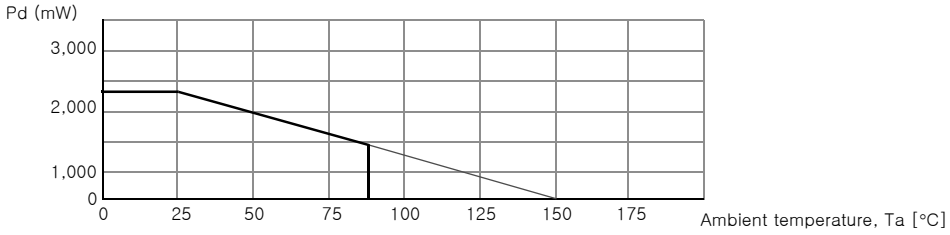
Equivalent Circuits (Continued)

Description	Pin No.	Internal Circuit
RES50	44	
REG050	41	
REG50	40	

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	V_{CCMAX}	18	V
Power Dissipation	P_D	2.3 note	W
Operating Temperature	T_{OPR}	-35 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C
Maximum Output Current	I_{OMAX}	1	A

Note:
1. When mounted on 70mm × 70mm × 1.6mm PCB.
2. Power dissipation reduces 18.4mW / °C for using above Ta=25°C.
3. Do not exceed Pd and SOA.



Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal Supply Voltage	SV_{CC}	4.5	-	13.2	V
Power Supply Voltage	PV_{CC1}	4.5	-	13.2	V
Power Supply Voltage	PV_{CC2}	4.5	-	13.2	V

Electrical Characteristics (Ta = 25°C)

(SV_{CC}=PV_{CC1}=PV_{CC2}=8V, Ta=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent Circuit Current	I_{CC}	under no-load	10	14	18	mA
All Mute On Current	$I_{MUTE\ ALL}$	Pin 46=GND	-	8	10	mA
All Mute On Voltage	$V_{MON\ ALL}$	Pin 46=Variation	-	-	0.5	V
All Mute Off Voltage	$V_{MOFF\ ALL}$	Pin 46=Variation	2	-	-	V
CH Mute On Voltage	$V_{MON\ CH}$	Pin 22, 23, 24=Variation	2	-	-	V
CH Mute Off Voltage	$V_{MOFF\ CH}$	Pin 22, 23, 24=Variation	-	-	0.5	V
DRIVER PART (R_L=8Ω)						
Input Offset Voltage	V_{IO}	-	-20	-	+20	mV
Output Offset Voltage	V_{OO}	V_{IN}=2.5V	-50	-	+50	mV
Maximum Output Voltage 1	V_{OM1}	V_{CC}=8V, R_L=8Ω	4.7	5.5	-	V
Maximum Output Voltage 2	V_{OM2}	V_{CC}=13V, R_L=24Ω	7	9	-	V
Closed-loop Voltage Gain	A_{VF}	V_{IN}=0.1V_{RMS}	9	10.5	12	dB
Ripple Rejection Ratio[note1]	RR	V_{IN}=0.1V_{RMS}, f=120kHz	-	50	-	dB
Slew Rate[note1]	SR	Square, Vout=2Vp-p, f=120kHz	-	0.8	-	V/μs
NORMAL OPAMP PART						
Input Offset Voltage	V_{OF1}	-	-10	-	+10	mV
Input Bias Current	I_{B1}	-	-	-	300	nA
High Level Output Voltage	V_{OH1}	-	6	6.8	-	V
Low Level Output Voltage	V_{OL1}	-	-	1.0	1.8	V
Output Sink Current	I_{SINK1}	R_L=50Ω	10	40	-	mA
Output Source Current	$I_{SOURCE1}$	R_L=50Ω	10	40	-	mA
Open Loop Voltage Gain[note1]	GV_{O1}	V_{IN}=-75dB, f=1kHz	-	75	-	dB
Ripple Rejection Ratio[note1]	R_{R1}	V_{IN}=-20dB, f=120kHz	-	65	-	dB
Slew Rate[note1]	S_{R1}	Square, Vout=2Vp-p, f=120kHz	-	1	-	V/μs
Common Mode Rejection Ratio[note1]	CM_{RR1}	V_{IN}=-20dB, f=1kHz	-	80	-	dB

Note:

1.Guaranteed field. (No EDS/ Final test .)

Electrical Characteristics (Continued)

(SV_{CC}=PV_{CC1}=PV_{CC2}=8V, Ta=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
INPUT OPAMP PART						
Input Offset Voltage	V_{OF2}	-	-10	-	+10	mV
Input Bias Current	I_{B2}	-	-	-	400	nA
High Level Output Voltage	V_{OH2}	-	7	7.7	-	V
Low Level Output Voltage	V_{OL2}	-	-	0.2	0.5	V
Output Sink Current	I_{SINK2}	-	500	800	-	μA
Output Source Current	$I_{SOURCE2}$	-	500	800	-	μA
Open Loop Voltage Gain[note1]	GV_{O2}	V_{IN} = -75dB, f =1kHz	-	80	-	dB
Slew Rate[note1]	SR2	Square, Vout=2Vp-p, f=120kHz	-	1	-	V/μs
Common Mode Rejection Ratio[note1]	CMRR2	V_{IN} = -20dB, f=1kHz	-	80	-	dB
5V REGULATOR PART						
Regulator Output Voltage	Vreg	I_L= 100mA	4.75	5	5.25	V
Load Regulation	DV_{R1}	I_L= 0→200mA	-40	0	+10	mV
Line Regulation	DV_{CC}	I_L=200mA, V_{CC}=6V →9V	-20	0	+30	mV
Reset On Voltage	Reson	-	-	-	0.5	V
Reset Off Voltage	Resoff	-	2	-	-	V
TRAY, CHANGER DRIVER PART(R_L=45Ω)						
Input High Level Voltage	V_{IH}	-	2	-	-	V
Input Low Level Voltage	V_{IL}	-	-	-	0.5	V
Output Voltage 1	V_{O1}	V_{CC}=8V, V_{CTL}=3.5V, R_L=8Ω	5.3	5.6	5.9	V
Output Voltage 2	V_{O2}	V_{CC}=8V, V_{CTL}=3.5V, R_L=45Ω	5.2	6.0	6.8	V
Output Voltage 3	V_{O3}	V_{CC}=13V, V_{CTL}=4.5V, R_L=45Ω	7.5	8.5	9.5	V
Output Load Regulation	DV_{R1}	-	-	300	700	mV
Output Offset Voltage 1	V_{OO1}	V_{IN}=5V, 5V	-10	-	+10	mV
Output Offset Voltage 2	V_{OO2}	V_{IN}=0V, 0V	-10	-	+10	mV

Note:

1.Guaranteed field. (No EDS/ Final test .)

Application Information

1. Reference Input & Mute

Pin 46 (REF) uses the reference input pin or the all mute input pin a reference input block circuit.

- Reference input
  In the case of external reference input, the applied voltage range must be between 2[V] and 6.5[V] at V_{CC}=8[V].
- All mute input
  Using the all mute function pin, the applied voltage condition is as follows.

All Mute On Voltage	Below 0.5[V]	Mute Function Operation
All Mute Off Voltage	Above 2.0[V]	Normal Operation

2. Separated Channel Mute Function

These pins are used for the individual channel mute operation.

- When the mute pins (pin22, 23 and 24) are high level, the mute circuits are activated so that the output circuit is muted.
- When the voltage of the mute pins (pin22, 23 and 24) are low level, the mute circuit is stopped and output circuits operate normally.
- If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuits are muted.
  - Mute 1, 2 (pin 24)-CH1, 2 mute control input pin.
  - Mute 3 (pin 23)-CH3 mute control input pin.
  - Mute 4 (pin 22)-CH4 mute control input pin.

3. Protection Function

- Thermal shutdown (TSD)
  If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuit is mute. The TSD circuit is temperature hysteresis about 25°C.
- Under voltage lockout (UVLO) and over voltage protection (OVP)
  It is designed to mute operate the internal bias by the function of UVLO and OVP, when the power supply voltage falls below 3.5[V] or above 20[V].

4. Regulator & Reset Function

The regulator and reset circuits are as illustrated in Figure 1.
where R1=R2.

- The external circuit is composed of the transistor, KSB772 and a capacitor, about 33[mF]. The capacitor is used as a ripple eliminator and should have good temperature characteristics.
- The regulator output voltage (pin 41) is decided as follows.
  Vout = 2 × 2.5 = 5[V] (where R1=R2)
- When the voltage of pin 44 (Vreset) is at 5[V], regulator output voltage(pin 41) is 5[V], and if 0[V], the output voltage of pin 41 is 0[V].

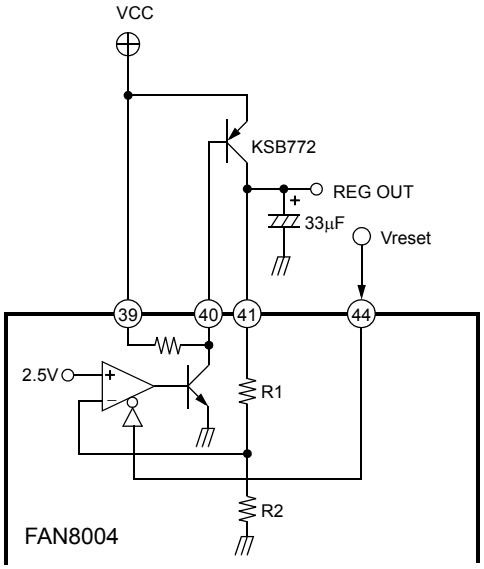
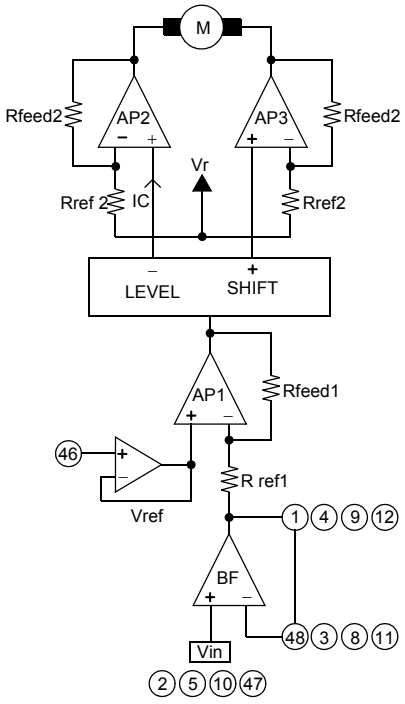


Figure 1. Regulator circuit

5. Focus, Tracking Actuator, Spindle, Sled Motor Drive Part

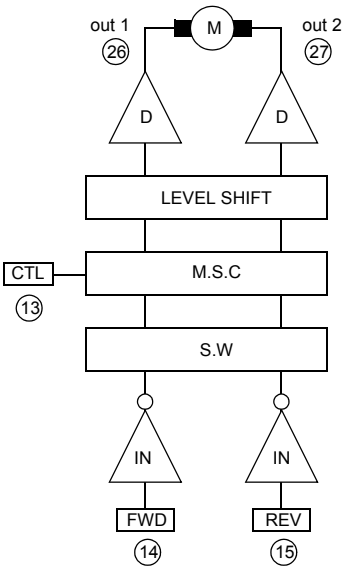


- The voltage, Vref is the reference voltage given by the external bias voltage of pin 46.
- The input signal (Vin) through pin 2, 5, 10 and 47 are by the AP1 amplified one times (Rref1=Rfeed1) and then fed to the level shift.
- The level shift produces the current due to the difference between the input signal and the arbitrary reference signal. The current produced as +ΔI and -ΔI are fed into the output amplifier. Where output amplifier (AP2, 3) gain is two times (all Rref2 = Rfeed2).
- If you desire to change the gain, the input buffer amplifier (BF) can be used.
- The output stage is the balanced transformerless (BTL) driver.

- The bias voltage Vr is expressed as below;

$$Vr = \frac{V_{CC} - V_{BE}}{2}[V]$$

6. Tray, Change Motor Drive Part



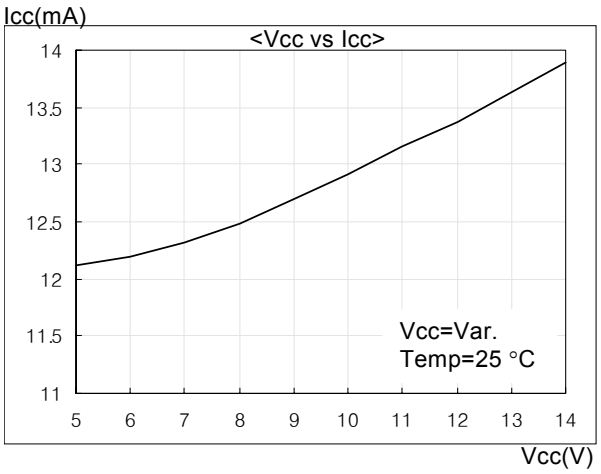
- Rotational Direction Control
  The forward and reverse rotational direction is controlled by FWD (pin 14), and REV (pin 15) inputs. Conditions are as follows.

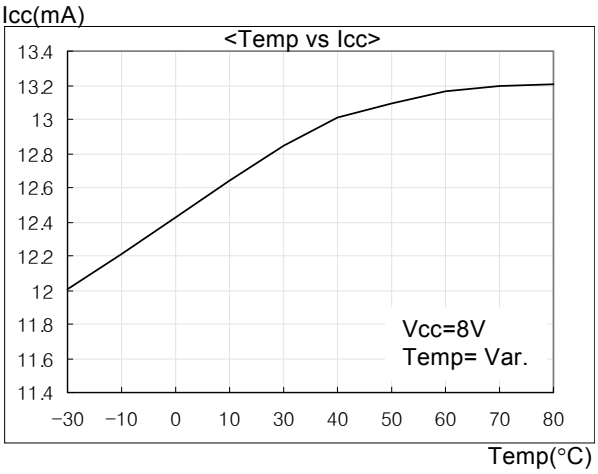
INPUT		OUTPUT		
FWD	REV	OUT 1	OUT 2	State
H	H	Vr	Vr	Brake
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	Vr	Vr	Brake

- Where Vris (V_{CC}-Vbe) / 2 = 3.65V (at V_{CC} = 8V)
- Motor Speed Control
  - The almost maximum torque is obtained when it is used with the pins 13 (CTL) open.
  - If the torque of the motor is too low, then the applied voltage at pins 13 (CTL) is 0[V].
  - When motor speed controlled, the applied voltage of the pins 13 (CTL) is between 0 and 4V.
    Also, if speed control is constant , the applied voltage of the pins 13 (CTL) is between 4 and 5V.
  - This IC's applied maximum voltage is 6V when V_{CC} is 8V.
  - You must not use the applied CTL voltage above 5.8V when Vcc is 8V, and 3V when V_{CC} is 5V.

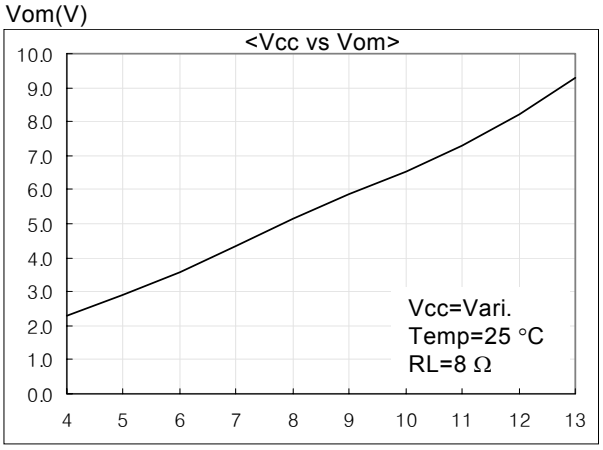
Typical Performance Characteristics

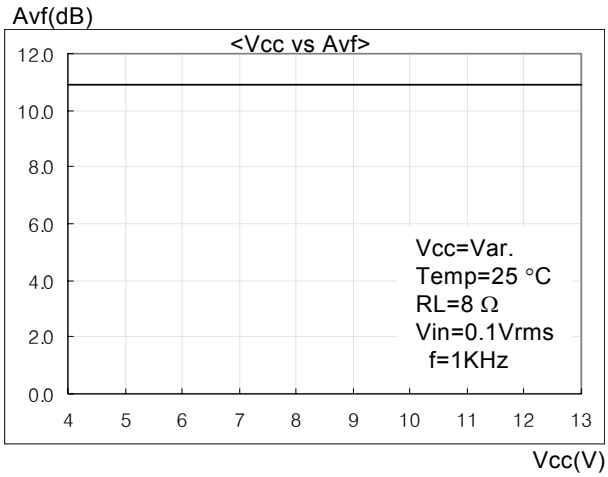
Total circuit

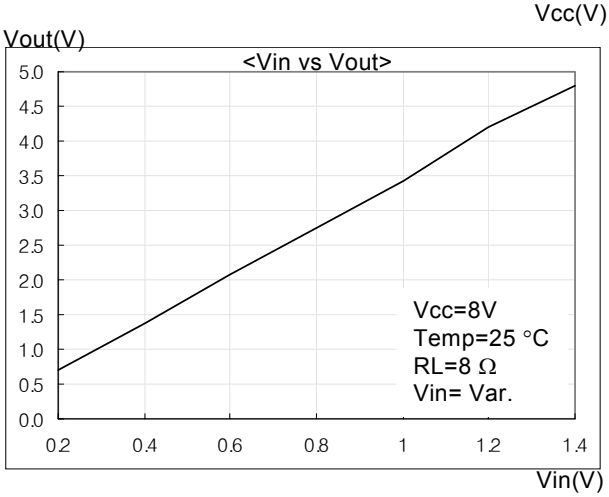


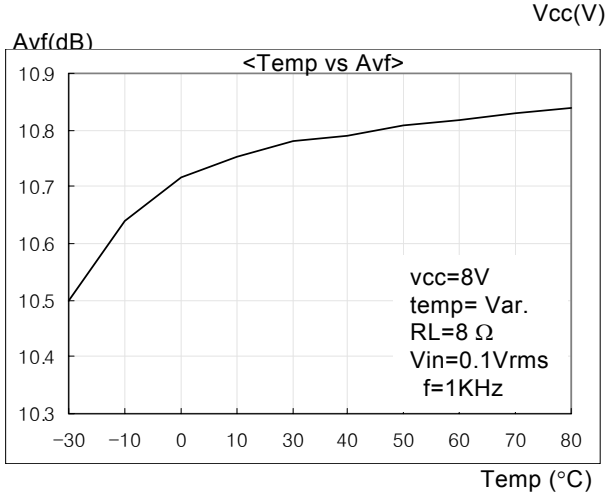


Focus, Tracking, Spindle, Sled drive part

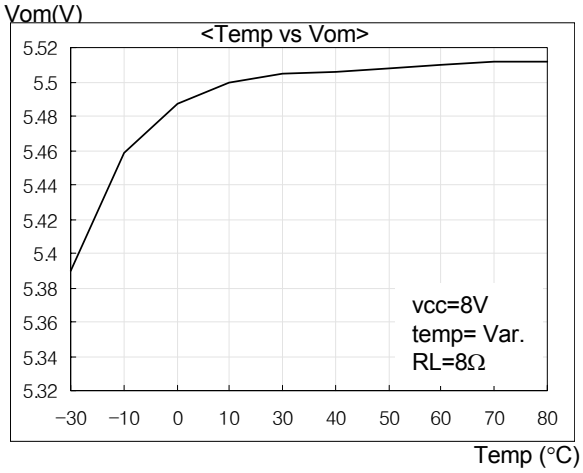




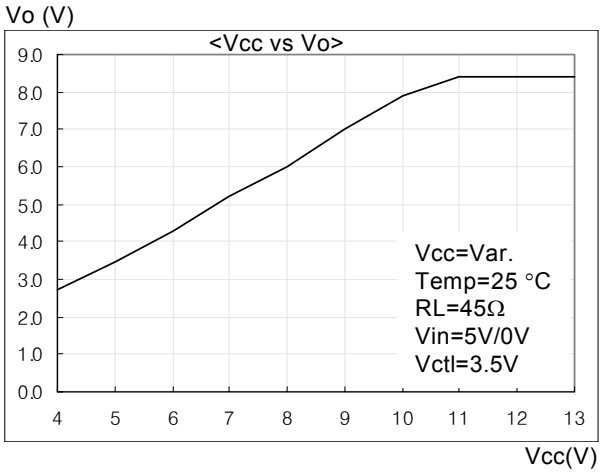


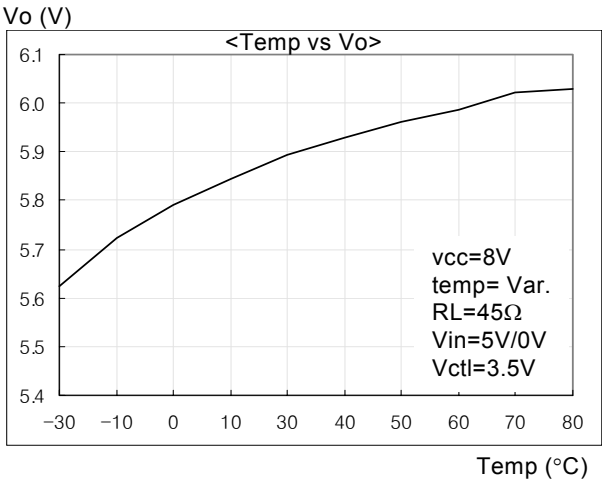


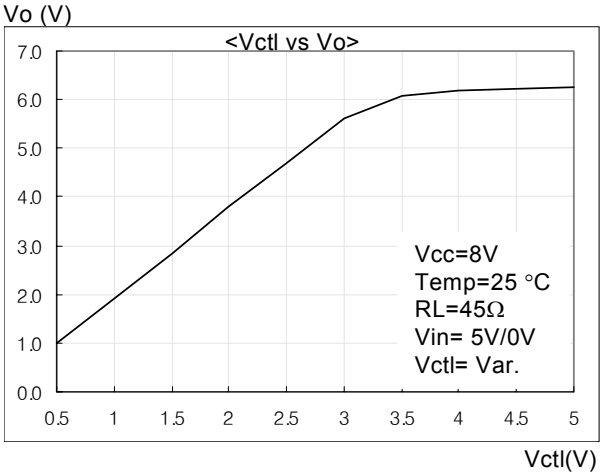
Typical Performance Characteristics (Continued)

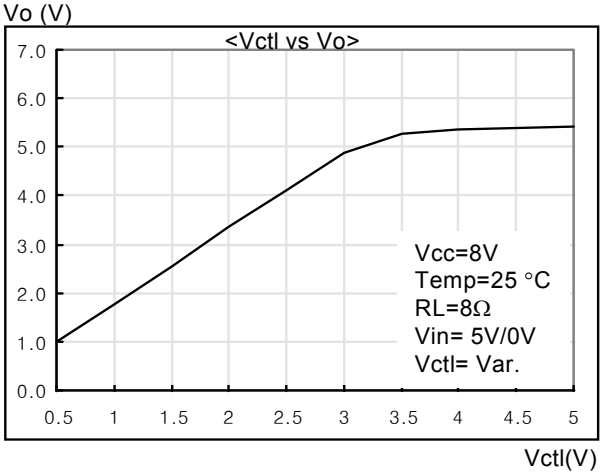


Tray Drive Part



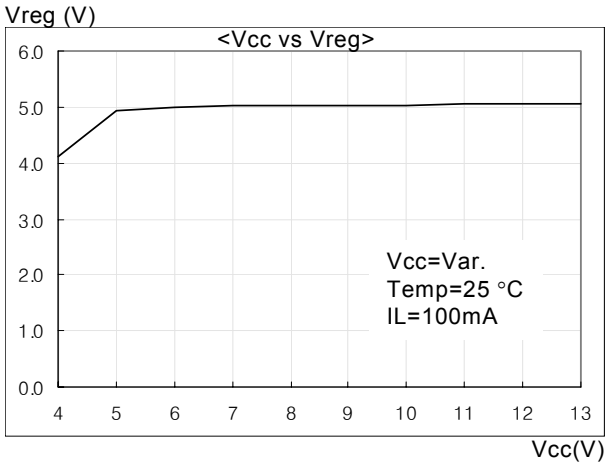


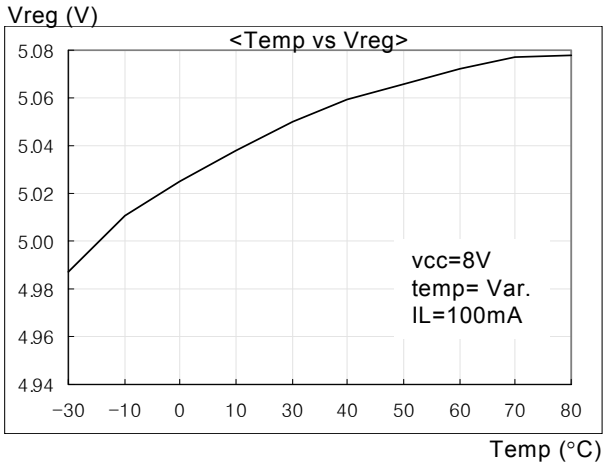




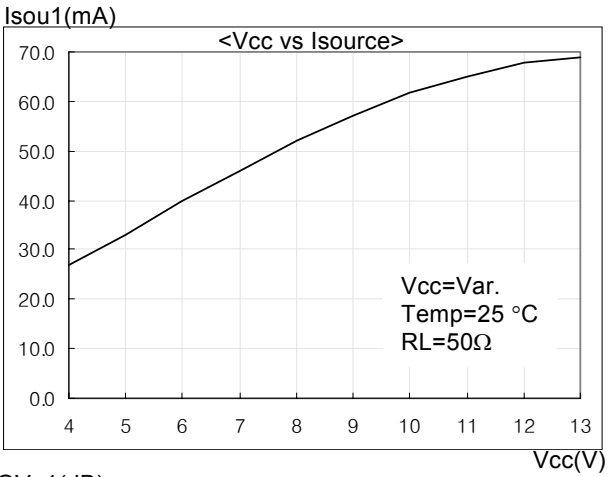
Typical Performance Characteristics (Continued)

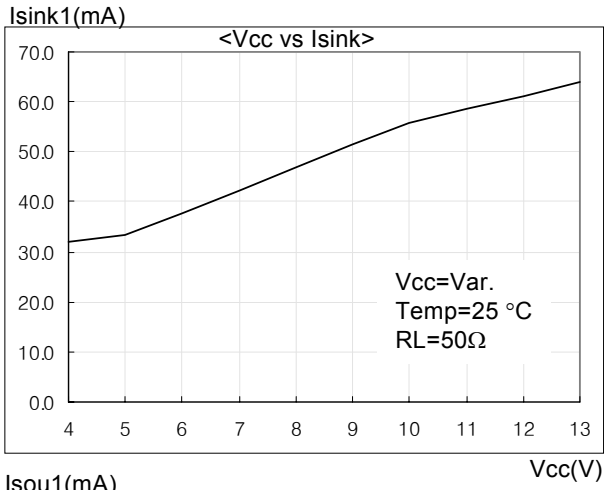
Regulator Part

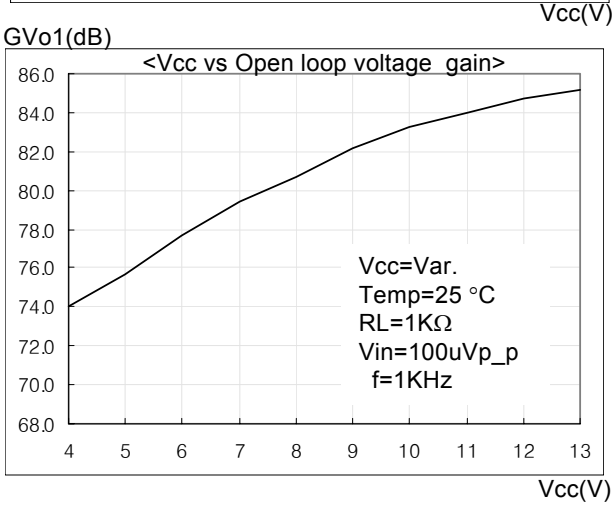


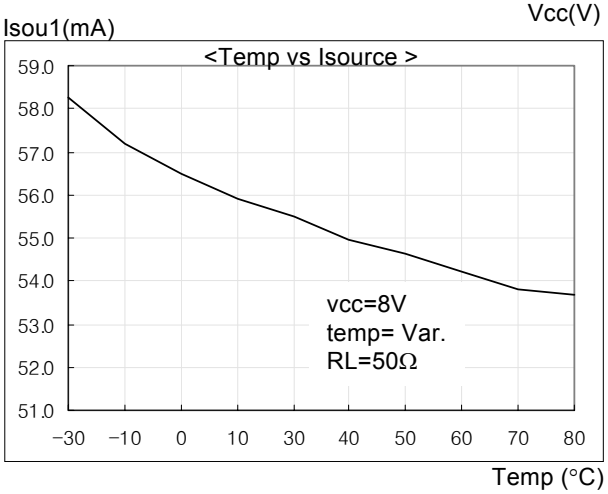


Normal OP-AMP Part

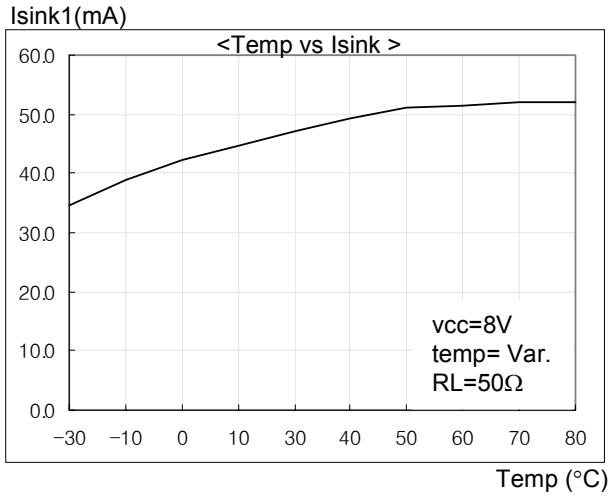




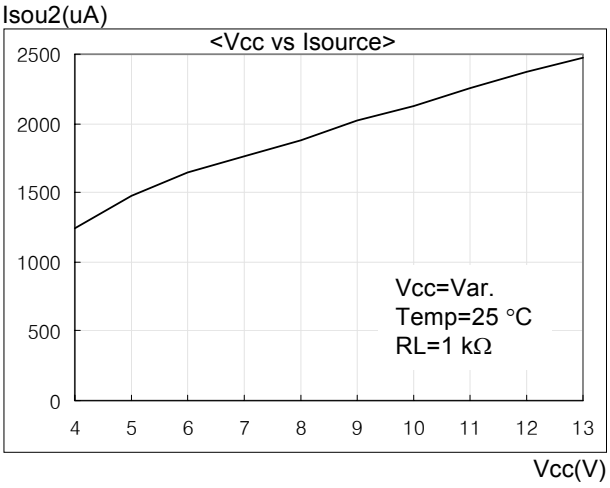


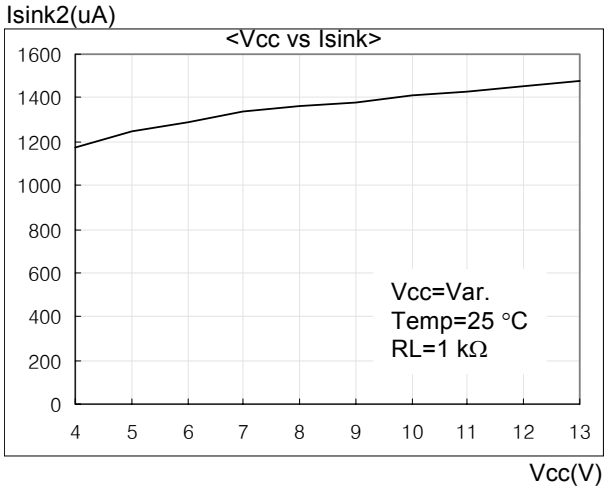


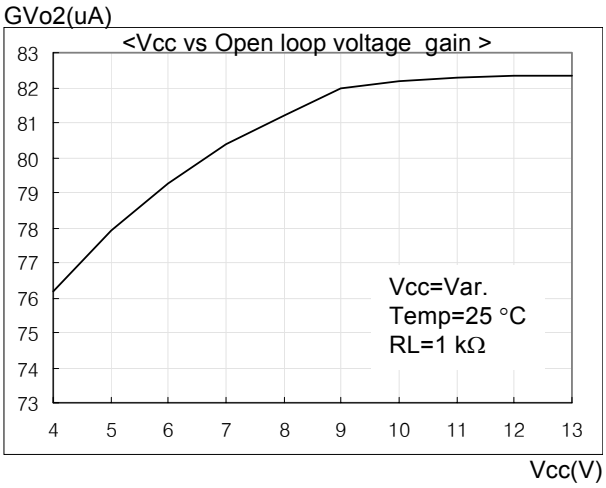
Typical Performance Characteristics (Continued)



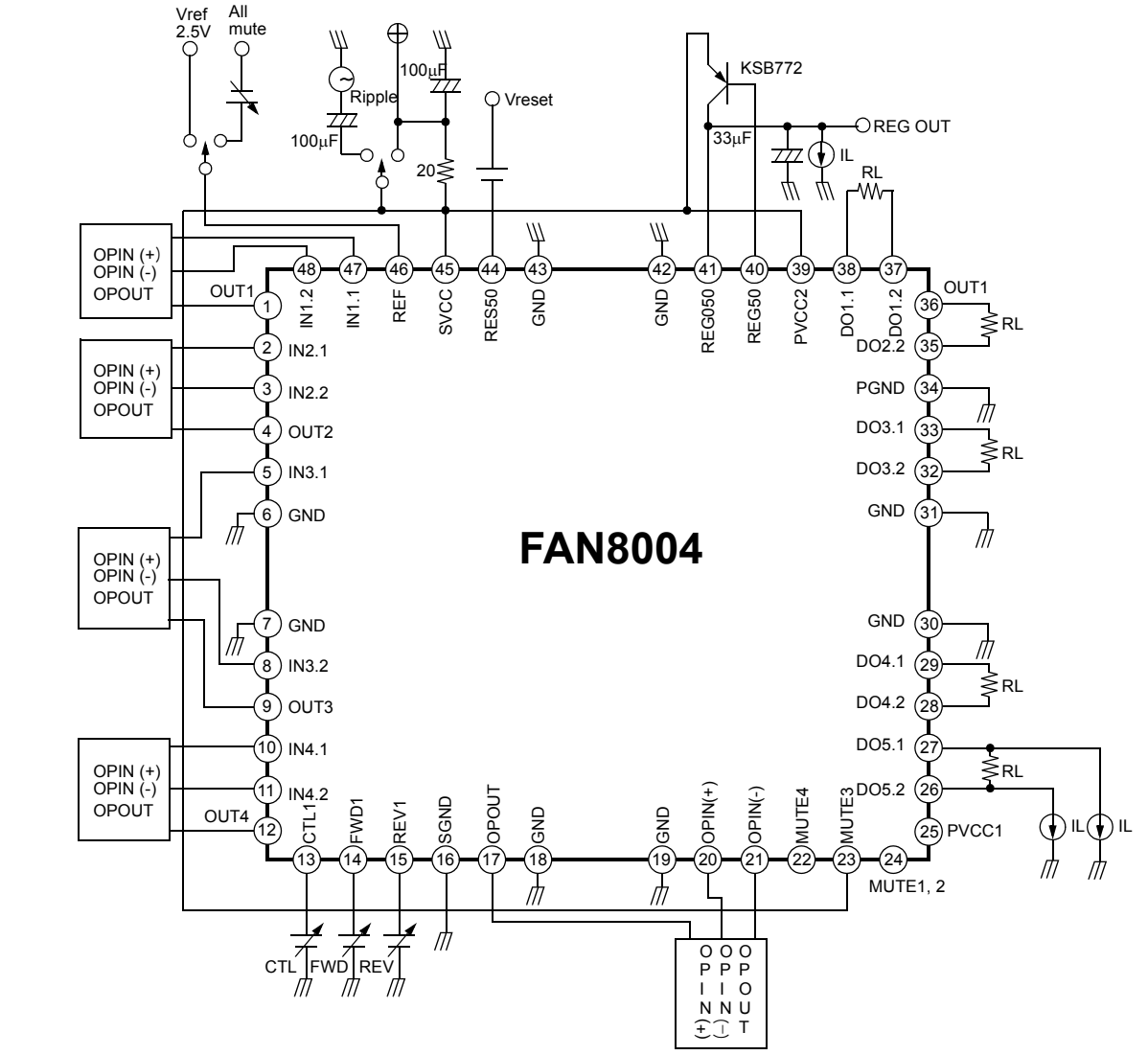
Input Op-Amp Part

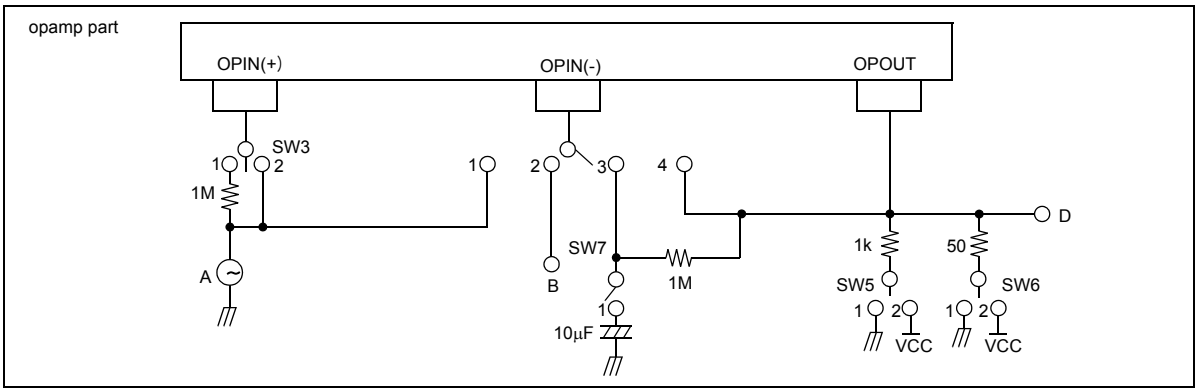






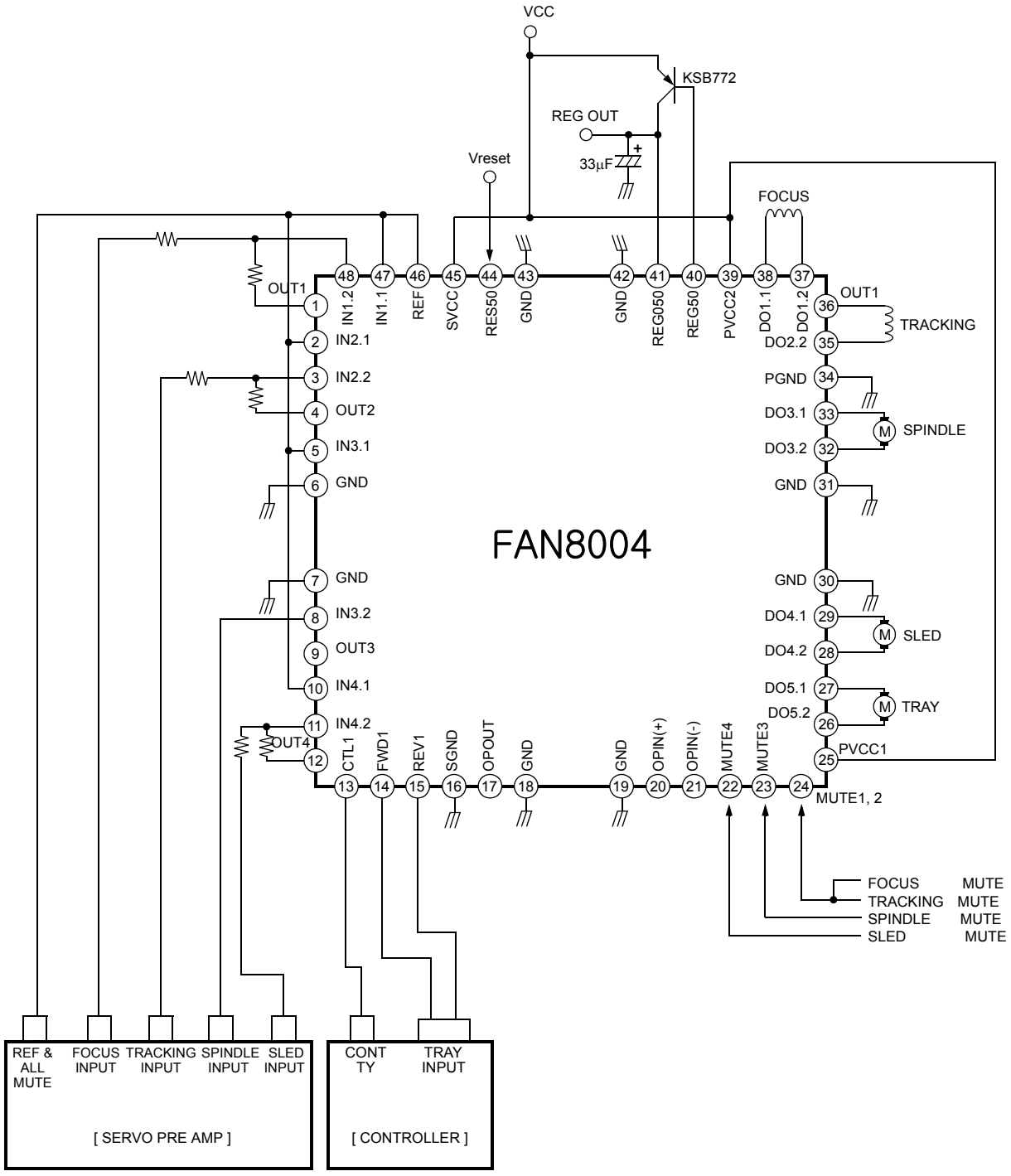
Test Circuit





Typical Application Circuit

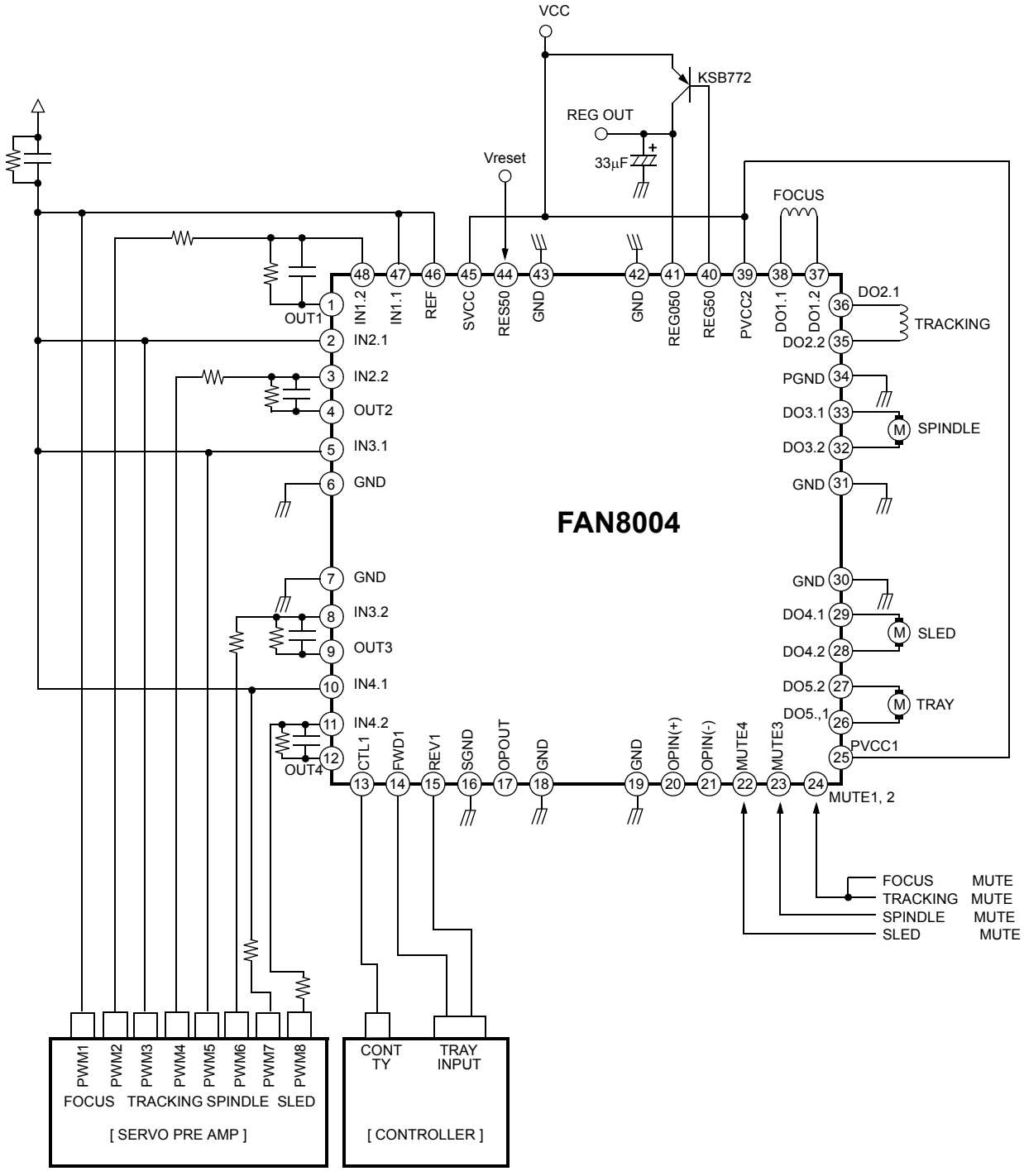
(Voltage Mode Contol)



Notes:
Cont: Controlle
TY: Tray

Typical Application Circuit

(Differential moad control)



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