FAN8039D3

5-CH Motor Driver

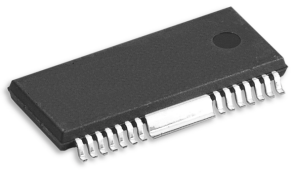
Features

- 1 Phase, Full-wave, Linear DC Motor Driver
- Built-in 5-CH Balanced TransFormerless (BTL) Driver
- Built-in thermal shut down circuit (TSD)
- Built-in Variable Regulator With Power Tr.
- Buiil-in Power Save Circuit
- Built-in stand by mode circuit
- Wide Operating Supply Voltage : 4.5 ~ 13.2V

Description

The FAN8039D3 is a monolithic integrated circuit suitable for a 5-ch motor driver which drives the tracking actuator, focus actuator, sled motor, tray motor, , spindle motor of the DVDP/CAR-CD systems.

28-SSOPH-375



Preliminary Specification

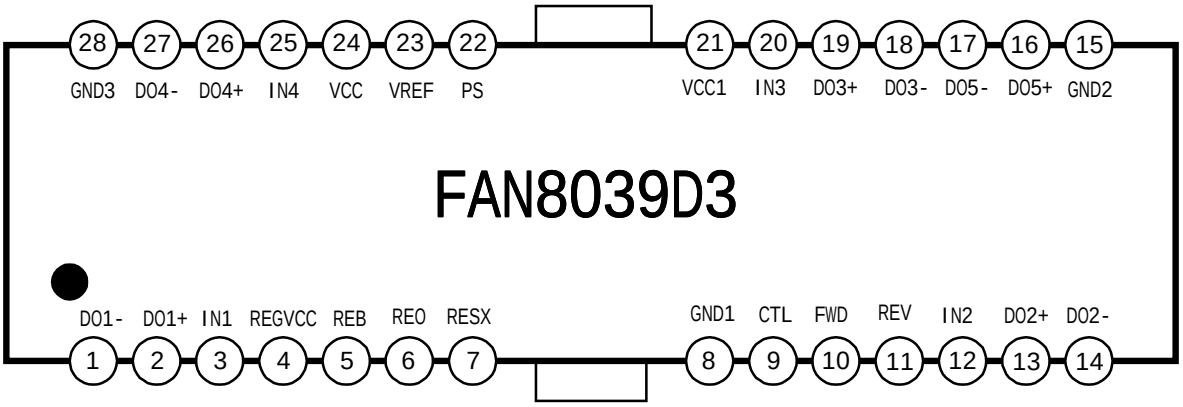
Typical Applications

- Compact disk player
- Video compact disk player
- Car compact disk player
- Mixing with compact disk player and mini disk player
- DVDP

Ordering Information

Device	Package	Operating Temp.
FAN8039D3	28-SSOPH-375	–35°C ~ +85°C

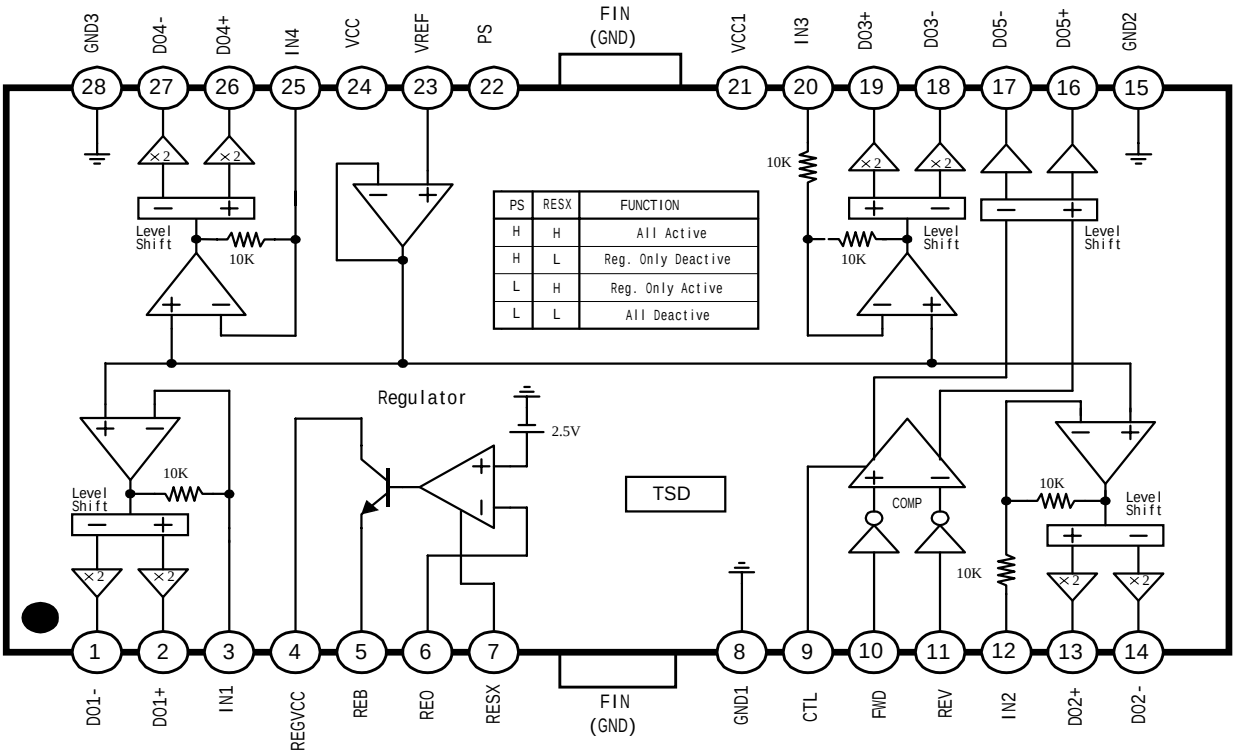
Pin Assignments



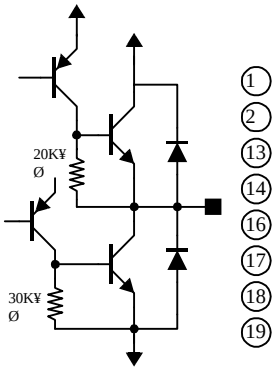
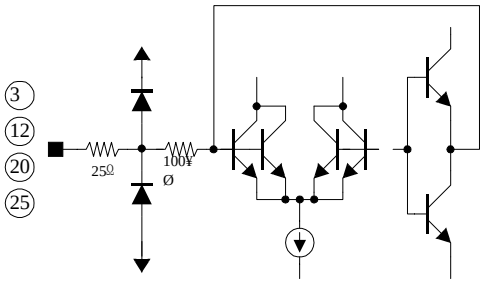
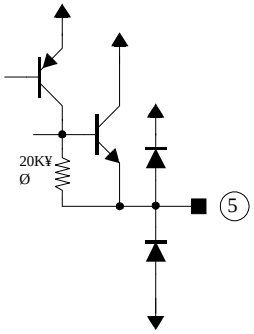
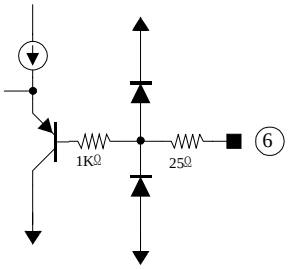
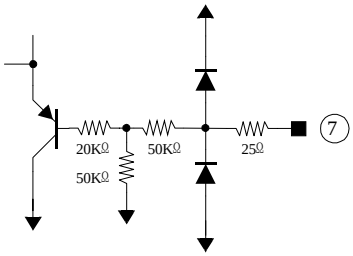
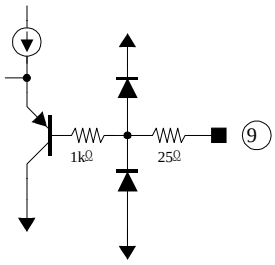
Pin Definitions

NO	Symbol	Description	NO	Symbol	Description
1	DO1-	CH1 Drive Output (-)	15	GND2	Power Ground1 (CH 2,3,5)
2	DO2-	CH1 Drive Output (+)	16	DO5+	CH5 Drive Output (+)
3	IN1	CH1 Input1	17	DO5-	CH5 Drive Output(-)
4	REGVOC	Regulator Supply Voltage	18	DO3-	CH3 Drive Output(-)
5	REB	Regulator Output	19	DO3+	CH3 Drive Output (+)
6	REO	Regulator Feedback Input	20	IN3	CH3 Drive Input
7	RESX	Regulator Reset	21	VCC1	Supply Voltage1
8	GND1	Signal Ground	22	PS	Power Save
9	CTL	CH5 Motor Speed Control	23	VREF	Bias Voltage
10	FWD	CH5 Forward Input	24	VOC	Supply Voltage
11	REV	CH5 Reverse Input	25	IN4	CH4 Input2
12	IN2	CH2 Drive Output	26	DO4+	CH4 Drive Output (+)
13	DO2+	CH2 Drive Output (+)	27	DO4-	CH4 Drive Output (-)
14	DO2-	CH2 Drive Output (-)	28	GND3	Power Ground2 (CH 1,4)

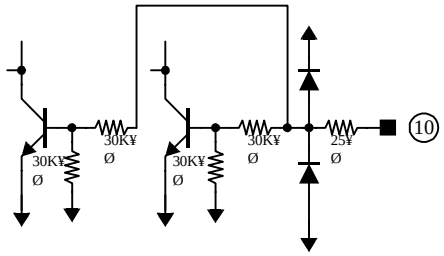
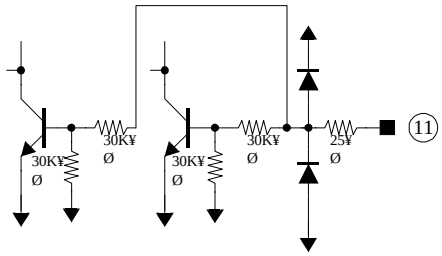
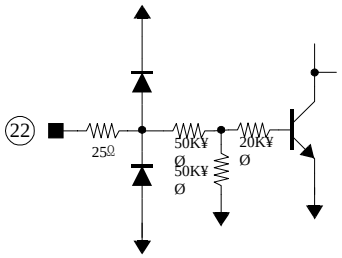
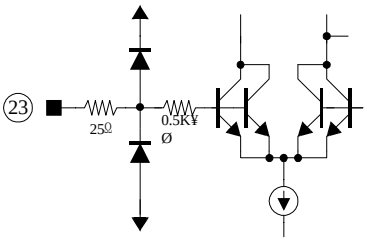
Internal Block Diagram



Equivalent Circuits

Btl Drver Output	Btl Drive Input
	
Regulator Output	**Regulator Feedback Input**
	
Regulator Reset	**Motor Speed Control**
	

Equivalent Circuits (Continued)

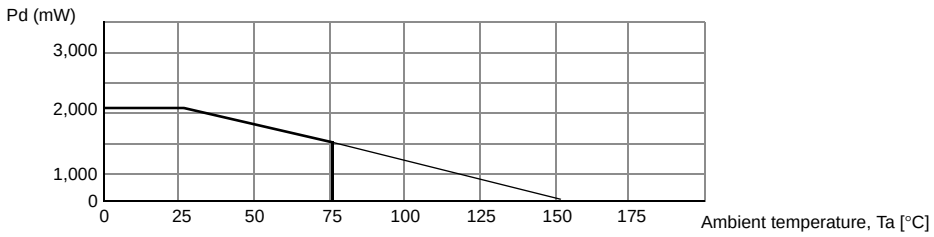
Foward Input	Reverse Input
	
Power Save	**Bias Voltage**
	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	V_{CC}	18	V
Power dissipation	P_D	2.0[note]	W
Operating temperature	T_{OPR}	–35 ~ +85	°C
Storge temperature	T_{STG}	–55 ~ +150	°C
Maximum output current	I_{OMAX}	1	A

Notes:

1. When mounted on 70mm × 70mm × 1.6mm PCB
2. Power dissipation reduces 24mW/°C for using above Ta = 25°C
3. Do not exceed P_D and SOA (Safe Operating Area)



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{CC}	4.5	-	13.2	V

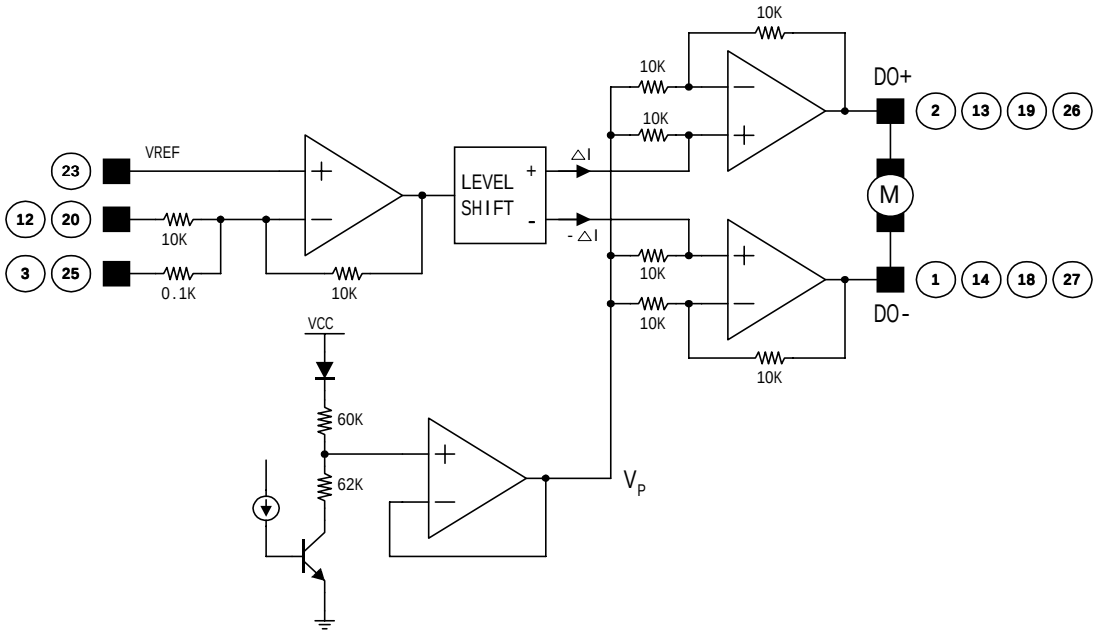
Electrical Characteristics

(SV_{CC} = PV_{CC1} = PV_{CC2} = 8V, T_A = 25°C, unless otherwise specified)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Quiescent circuit current	I_{CCQ}	Under no - load	-	20	-	mA
Power save on current	I_{PS}	Pin7=GND	-	1	2	mA
Power save on voltage	V_{PSON}	Pin7=Variation	-	-	0.5	V
Power save off voltage	V_{PSOFF}	Pin7=Variation	2	-	-	V
VARIABLE REGULATOR PART						
Load regulation	ΔV_{RL}	I_L = 0mA → 200mA	-40	0	10	mV
Line regulation	ΔV_{CC}	I_L = 200mA, V_{CC}=6V → 9V	-20	0	30	mV
Regulator output voltage 1	V_{REG1}	I_L = 100mA	4.75	5	5.25	V
Regulator output voltage 2	V_{REG2}	I_L = 100mA	3.135	3.3	3.465	V
BLT DRIVER PART						
Output offset voltage	V_{OO}	V_{IN}=2.5V	-40	0	40	mV
Maximum output voltage1	V_{OM1}	V_{CC}=Vcc1=8V, RL = 12Ω	5.5	6.5	-	V
Maximum output voltage2	V_{OM2}	V_{CC}=Vcc1=13V, RL = 24Ω	10.5	11.5	-	V
Close loop voltage gain	A_{VF}	V_{IN}=0V, 1Vrms, f = $1K^{HZ}$	10.5	12	13.5	dB
Slew rate	SR	V_{OUT}=$4V_{P-P}$, f = $120K^{HZ}$, Square	-	2	-	V/µs
LOADING MOTOR DRIVER PART						
Input high level voltage	V_{IH}	-	2	-	-	V
Input low level voltage	V_{IL}	-	-	-	0.5	V
Output voltage1	V_{O1}	V_{CC}=V_{CC}1=8V, V_{CTL}=OPEN, RL=12Ω	5.5	6.5	-	V
Output voltage2	V_{O2}	V_{CC}=V_{CC}1=12V, V_{CTL}=OPEN, RL=24Ω	9.5	10.5	-	V
Output offset voltage1	V_{OO1}	V_{IN}=5V , 5V	-40	-	40	mV
Output offset voltage2	V_{OO2}	V_{IN}=0V , 0V	-40	-	40	mV

Application Information

1. Driver (Except For Loading Motor Driver)



The voltage, VREF is the reference voltage given by the external bias voltage of the pin #23. The input signal (VIN) through pin #12,20 is amplified by 10k/10k times and then fed to the level shift. The level shift produces the current due to the difference between the input signal and the arbitary reference signal. The current produced as +°,I and -°,I is fed into the driver Amp. The driver Amp. operates the power TR. of the output stage as the 2 times gain(1+10k/10k) according to the state of the input signal.

$$V_{IN} = V_{REF} + \Delta V \Delta I = \frac{\Delta V}{10K}$$

$$DO+ = V_P + \Delta I \bullet 10K \bullet \left(1 + \frac{10K}{10K}\right) = V_P + 2\Delta V$$

$$DO- = V_P - \Delta I \bullet 10K \bullet \left(1 + \frac{10K}{10K}\right) = V_P - 2\Delta V$$

$$V_{OUT} = (DO+) - (DO-) = 4\Delta V$$

$$GAIN = 20\log\left(\frac{V_{OUT}}{\Delta V}\right) = 12dB$$

If it is desired to change the gain, then the pin #3 or 25 can be used.

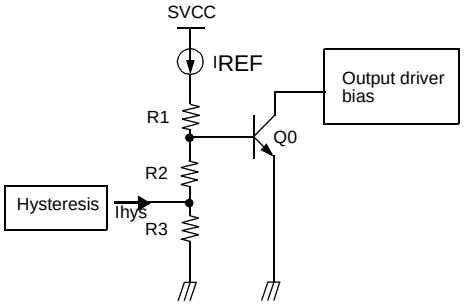
The output stage is the balanced transformerless (BTL) driver.

The bias voltage VP is expressed as

$$V_P = (VCC - V_{BE} - V_{CE(SAT)}) \times \frac{62K}{60K + 62K} + V_{CE(SAT)}$$

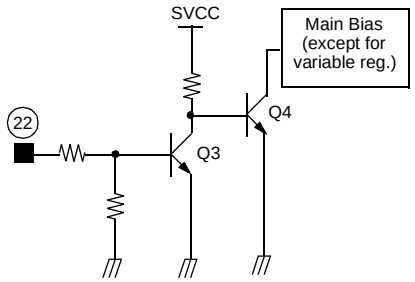
$$= \frac{VCC - V_{BE} - V_{CE(SAT)}}{1.97} + V_{CE(SAT)}$$

2. Thermal Shutdown



- When the chip temperature reaches to 175°C, then the TSD circuit is activated.
- This shuts down the bias current of the output drivers, and all the output drivers are in cut-off state. Thus the chip temperature begins to decrease.
- when the chip temperature falls to 150°C, the TSD circuit is deactivated and the output drivers are normally operated.
- The TSD circuit has the hysteresis temperature of 25°C.

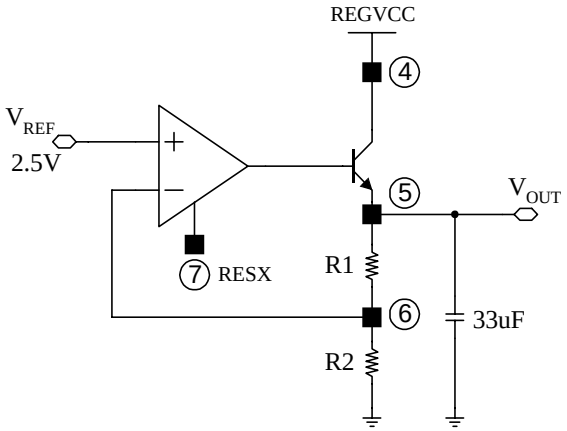
3. Power Save Function



- When the pin21 is high, the TR Q3 is turned on and Q4 is off, so the bias circuit is enabled. On the other hand, when the pin21 is Low (GND) , the TR Q3 is turned off and Q4 is on, so the bias circuit is disabled.
- That is, this function will cause all the circuit blocks of the chip except for the variable regulator to be in the off state. thus the low power quiescent state is established
- Truth table is as follows;

Pin#22	FAN8039
High	Power Save Off
Low	Power Save On

4. Variable Regulator

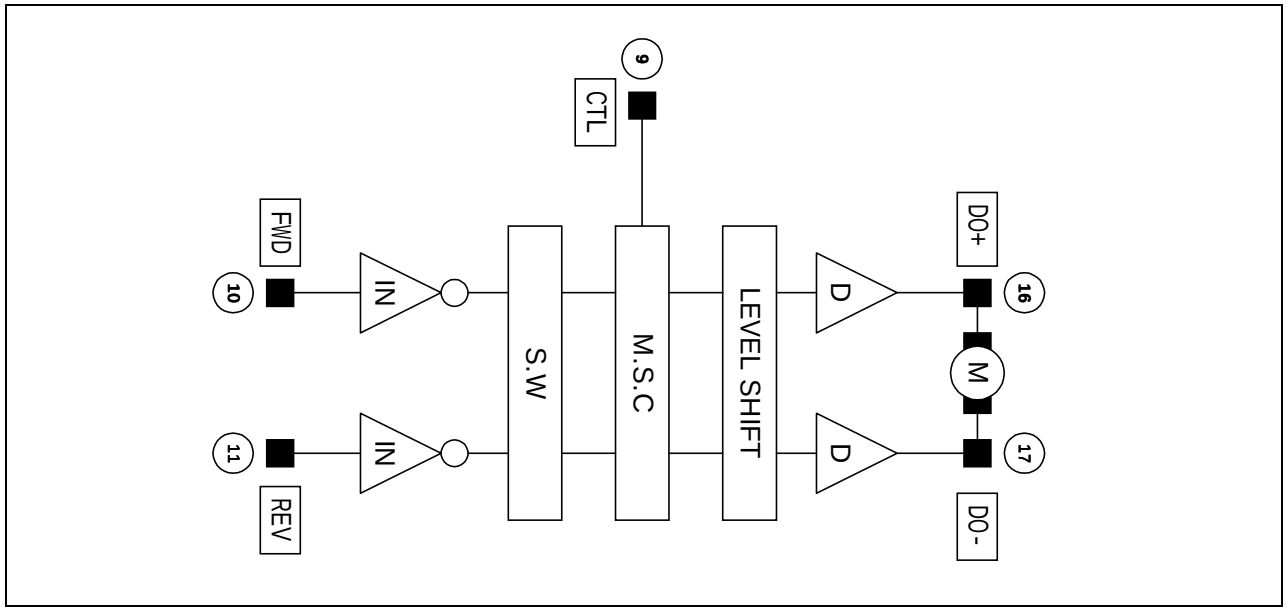


The VREF is the output voltage of the referenced biasing circuit and is the reference voltage of the regulator. (VREF=2.5V) The external circuit is composed of a capacitor, 33uF, which is used as a ripple eliminator The output voltage, VOUT is decided as follows

.

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) = 2.5 \times 2 = 5V (R1 = R2)$$

5. Tray, Changer, Panel Motor Drive Part

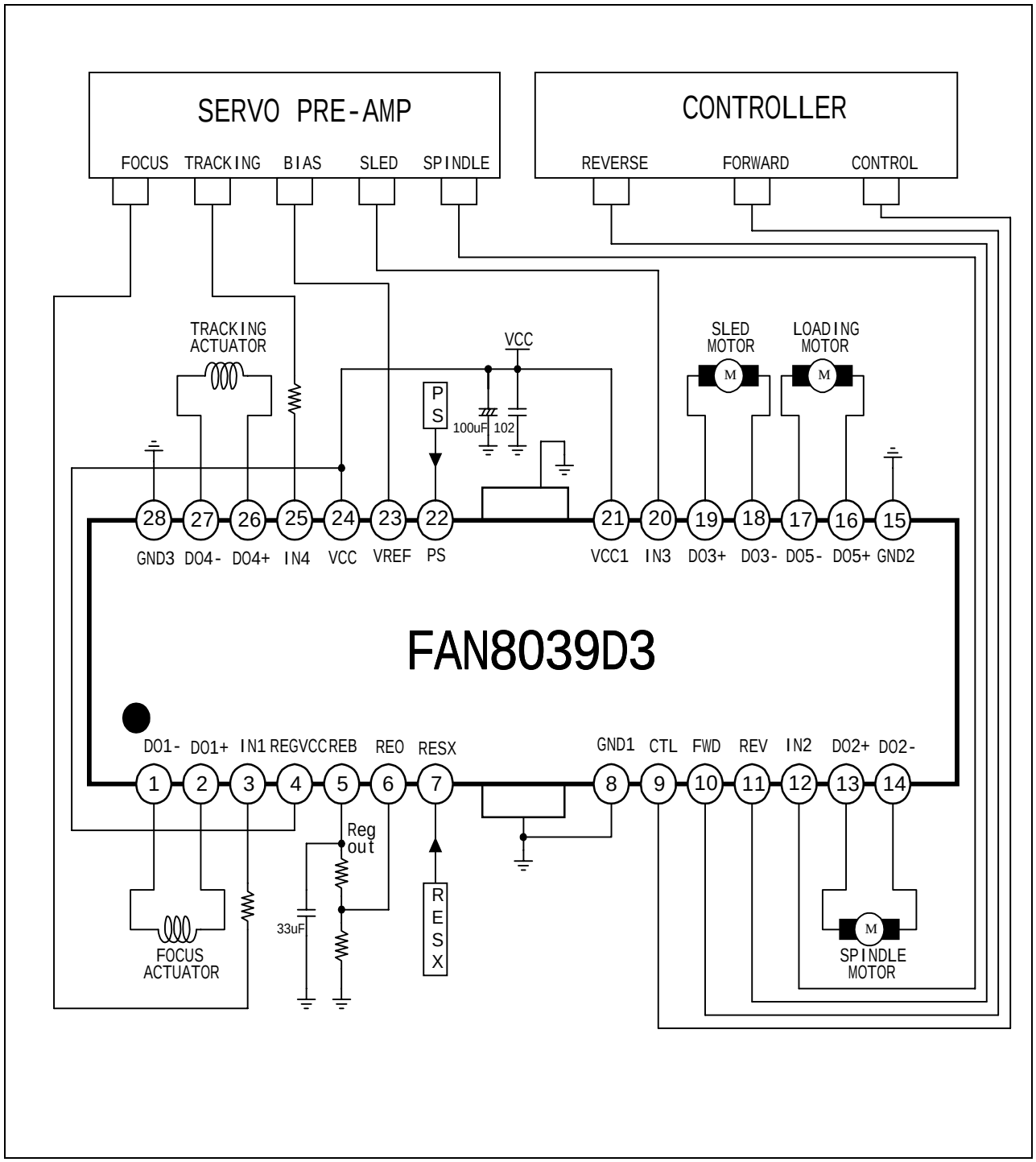


- Rotational direction control (S.W)
- The forward and reverse rotational direction is controlled by FWD(pin #10) and REV(pin #11) and the input conditions are as follow.
- VP(Power reference voltage) is approximately about 3.75V at VCC=8V according to equation (1).
- Motor speed control (M.S.C : V_{CC}=V_{CC1}=8V)
- The almost maximum torque is obtained when the pin #20 (CTL) are open.
- If the voltage of the pin #9 (CTL) are between 0 and 3.25V, the differential output voltagE (V(DO+,DO-)) is about two times of the control voltage. Hence, the control to the differential output gain is two.

The control voltage is greater than 3.25V, the output voltage is saturated at the 6.5V because of the output swing limination.

INPUT		OUTPUT		
FWD	REV	DO+	DO-	STATE
H	H	V_P	V_P	Brake
	L	H	L	Forward
L	H	L	H	Reverse
	L	V_P	V_P	Brake

Typical Application Circuits 1



Notes:

1. Radiation pin is connected to the internal GND of the package.
2. Connect the pin to the external GND.