HD49781/NT

Wide Aspect VISS Recording NTSC/PAL 1-Chip VHS Servo

VTR SERVO LSI HD49781 has digital servo functions for drum and capstan motor, as well as analog amplifier. It is a 1-chip device, and therefore can be applied on various types of VTR sets. This IC comes in 56-pin plastic shrink DIP and 56-pin QFP packages. This IC uses serial control method to connect to system controller (microcomputer). By this method, many functions can be entered internally, and the number of external components and wirings can be reduced.

Features

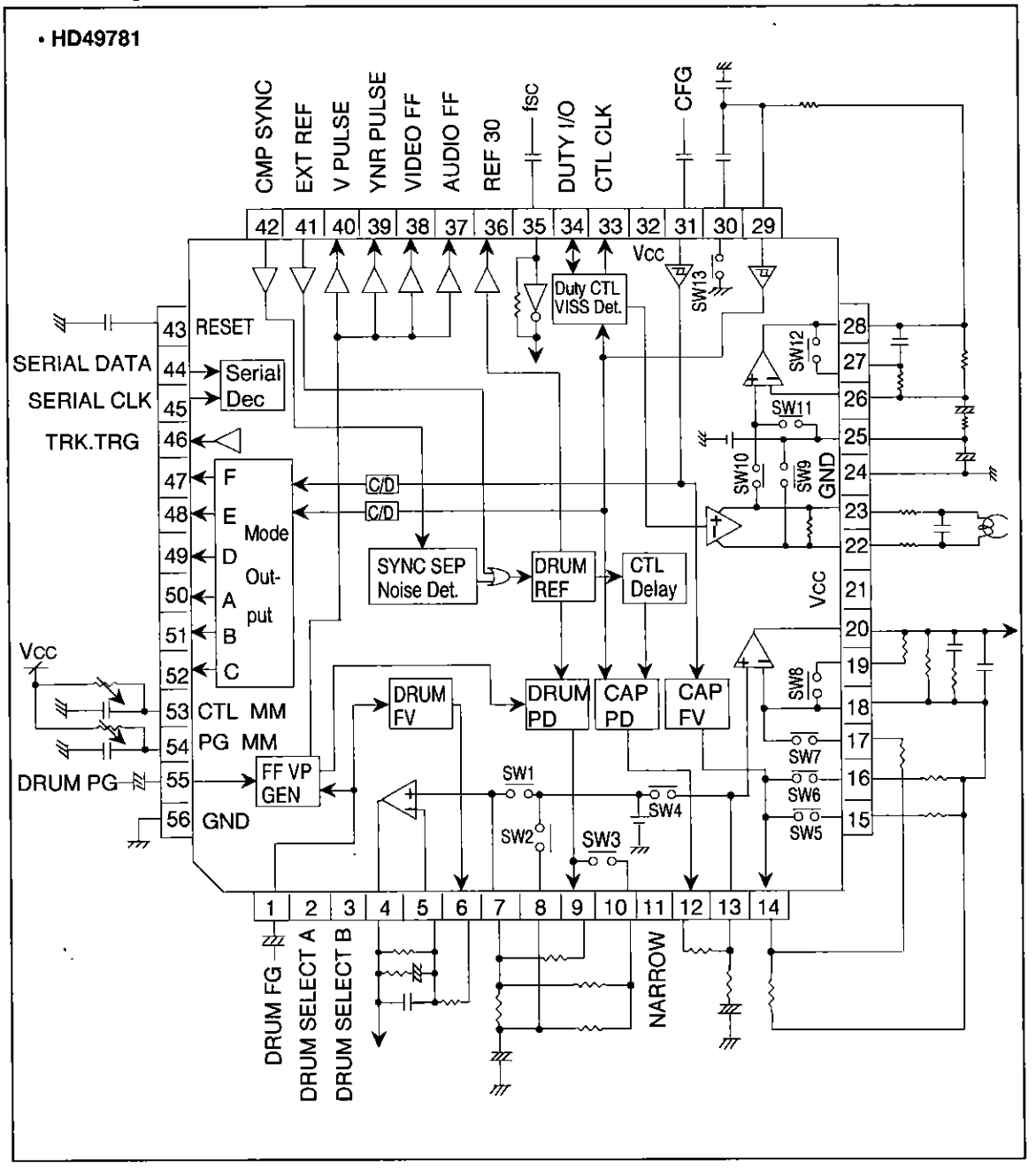
- PAL/NTSC 1-chip.
- By changing the corresponding mask ROM, CFG (capstan frequency generator), DFG (drum frequency generator) and HEAD SW timing can be set to satisfy the particular set's specifications.
- In previous versions, there are only VISS recording and rewriting function, and VISS detection function. For this IC, wide aspect VISS recording and rewriting function are added.
- In VASS function mode, recording and rewriting can be performed.
- With CMOS analog technology, CFG, DFG and DPG Schmitt amplifier, and analog switch are included.
- Uses synchronized serial bus with microcomputer interface. As the result, it is bussing-common with other Hitachi's ICs, and a less-wiring system can be constructed.

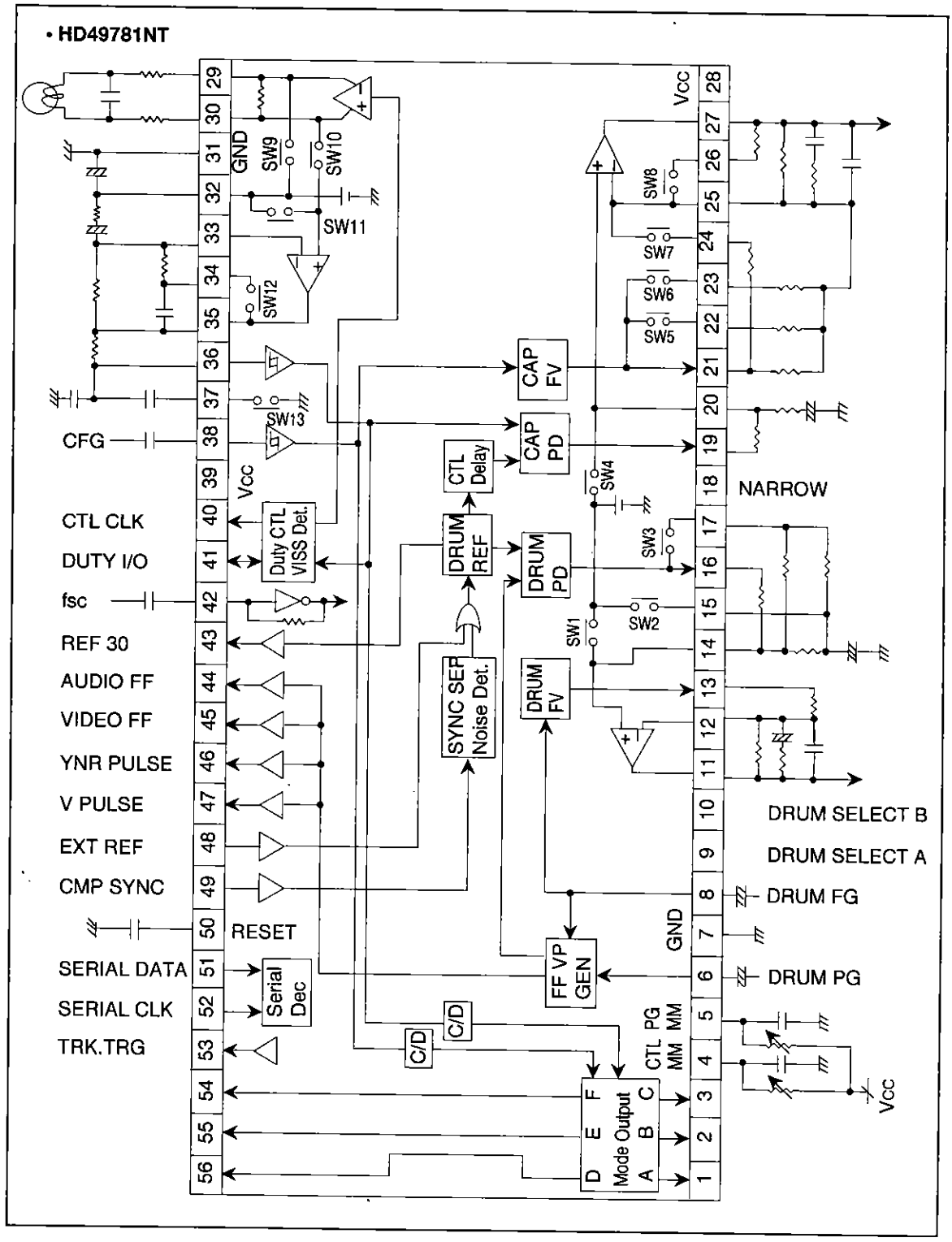
Main Functions

- 2-line serial bus.
- EP-designated Head function.
- VISS/VASS (Wide Aspect VISS Recording)
- Tracking data is controlled by serial bus.
- Digital adjustment of HEAD SW point.
- CTLP AMP Schmitt level is self-switchable.
- Search speed is selectable from 1-time to 63-times in each mode.
- Assemble Mark recording and detecting.
- Search function in Assemble mode.
- YNR PULSE output.
- CTLP AMP gain and frequency characteristics are controlled serial bus.
- Drum and capstan PD-FIX are controlled by serial bus.
- Drum and capstan outputs are controlled by serial bus.
- Field detection.
- Noise detection.
- Feedback f_H-correction.
- V-PULSE output
- V-PULSE polarity is controlled by serial bus.

Home

Block Diagram



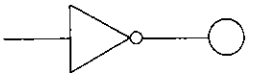

• HD49781NT
GND
SW9
SW10
SW11
SW12
SW13
CFG
Vcc
CTL CLK
DUTY I/O
fsc
REF 30
AUDIO FF
VIDEO FF
YNR PULSE
V PULSE
EXT REF
CMP SYNC
RESET
SERIAL DATA
SERIAL CLK
TRK.TRG
Duty CTL VISS Det.
Serial Dec
C/D
C/D
CTL Delay
DRUM REF
SYNC SEP Noise Det.
CAP FV
CAP PD
DRUM PD
DRUM FV
FF VP GEN
Mode Output
A B C D E F
CTL PG MM
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
NARROW
DRUM SELECT B
DRUM SELECT A
DRUM FG
DRUM PG
Vcc
GND

Pin Function

Pin No. | **Pin Name** | **Function** | **I/O Format**

1, 2, 3 — MODE OUT

	DATA					ADDRESS		
	MSB				LSB	0 1 0 0 0 0 1 1		
Bit	F E D C	B A 9 8	7 6 5 4	3 2 1 0		MODE OUT		
						A PIN 1	B PIN 2	C PIN 3
			0 1					0 1
			0 1				0 1	
			0 1			0 1		

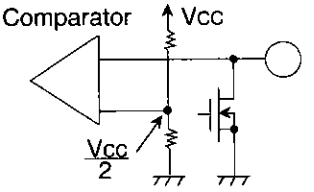


4 — CTL DELAY MM

Time constant: 1 to 40 ms
Note: See time chart
Retriggerable (discharge pulse: approx. 1 ms)

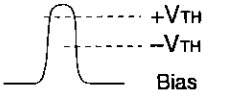
5 — PG MM

Non- retriggerable
Note: See head SW timing



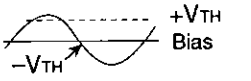
6 — DRUM PG IN

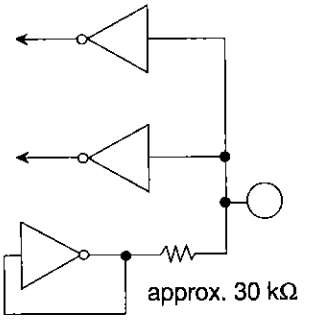
Schmitt input. Internal bias: approx. 2V
Note: See head SW timing



8 — DRUM FG IN

Schmitt input. Internal bias: approx. 2.5 V
Note: See head SW timing





9 — DRUM Select A
10 — B

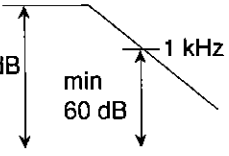
Ternary input
Open = "M"

Pin 9 / Pin 10	H	M	L
H	2 Head ①	2 Head ②	DA4-④
M	DA-4 ①	DA4-②	DA4- ③
L	DA-4 ① TEST	DA-4 ② TEST	DA-4 ③ TEST

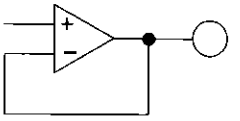
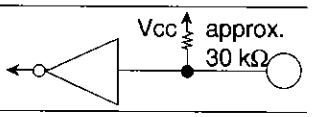
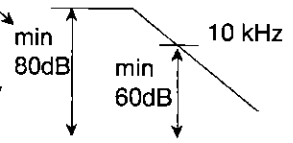
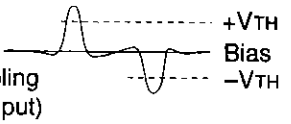
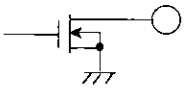
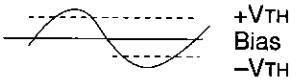
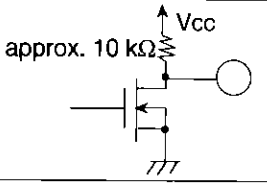
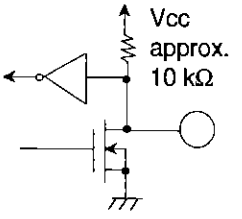
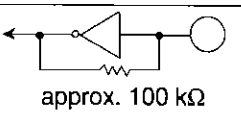
Note: See head SW timing

CAPSTAN MIX Amp
DRUM MIX Amp

– Open Gain → min 75 dB @ 1 kHz, min 60 dB
– No Oscillation at full feedback
– Output D range: 0 to 5 V (No load)
– Output impedance: 2 kΩ max.

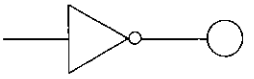
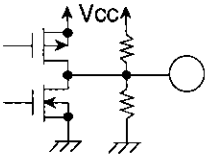
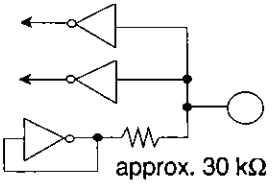
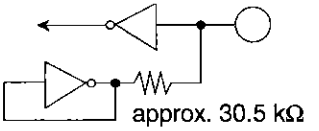
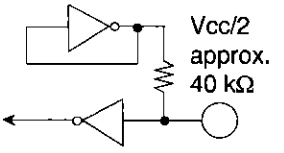
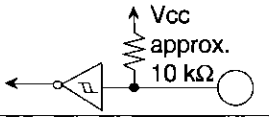
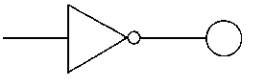


Pin Function (cont)

Pin No.	Pin Name	Function	I/O Format
13 21	DRUM FV out CAP FV out	Switched capacitor DA output Output D range: 0.5 V or less (Lo) to 4.3 V or more (Hi) Output impedance: 100 Ω max	
16 19	DRUM PDout CAP PD out	Switched capacitor DA output Output D range: 0.5 V or less (Lo) to 4.3 V or more (Hi) Output impedance: 100 Ω max	
18	NARROW	Binary input Open = "H" H: Narrow L: Non-Narrow	
29 30	CTL Head ⊖ CTL Head ⊕		
	CTLP Amp	– Open Gain – No oscillation at full feedback – Output D range 0 to 5 V (No Load) – Output impedance: 2 kΩ max	
36	CTLP IN	3-level Schmitt input selection No internal bias (DC coupling CTLP AMP and schmitt input) Note: See CTL schmitt V_{TH}	
37	SW13	Controlled by serial data Note: See serial data table	
38	CFG IN	Schmitt input Internal bias: approx. 2.5 V	
40	CTL CLK	Binary output. Pull up	
41	Duty I/O	Binary input and output. Pull up Note: See Duty I/O	
42	fsc in	Input sensitivity: 150 mVpp min (during fsc) Note: See fsc input circuitry	

Mode / Pin 41	ASBL Mark detection	Duty Mode	VISS Mode
H	No mark	Duty = "0"	VISS not detect
L	Mark	Duty = "1"	VISS detect (Latch)

Pin Function (cont)

Pin No.	Pin Name	Function	I/O Format
43	REF 30	Note: See time chart	
44	AFF	Note: See FF time chart	
45	VFF	Note: See FF time chart	
46	YNR Pulse		
47	V Pulse	Note: See V-Pulse	
48	EXT. Reset	Ternary input Open = "M" Note: See external synchronization	
49	CMP SYNC	Binary input. Digital level input or analog capacitance coupling input.	
50	Power on Reset	During power on, reset so that no current is flowing through CTL Head pin. Insert a capacitor between this pin and ground.	
51	Serial Data	Binary schmitt input. Pull-up Note: See explanation of SSB	
52	Serial CLK		
53	TRK TRG		
54	CFG C/D		
55	CTL C/D		
56	MODE OUT		
	NOISE DET		

DATA				ADDRESS
MSB			LSB	01000011
FEDC	BA98	7654	3210	MODE OUT

				D PIN56	E PIN55	F PIN54
			0		CTL C/D	CFG C/D
			0 1		0	CFG
			1 1		1	CFG
				NOISE DET M-FF		
		0	0	0		
		1	0	1		
		0	1	0		
		1	1	1		

Functional Description

1. Synchronized Serial Bus (SSB)

1.1 Outline

1.1.1 Configuration

This communication technique consists of one serial clock (SCL) and one serial data (SDA) lines. This SSB technique enables multiple ICs to be controlled using a common bus.

1.1.2 Data Length

In this servo IC, the data consists of 8 bits in the address field and 16 bits in the data field.

1.1.3 Operation Description

Data is fetched and stored into the shift registers of the ICs connected to a synchronized serial bus and defined, as described below, by the state of the SDA counter that increments on the falling edge of SDA signal. The SDA counter operates while the SCL clock is high, and is reset while it is low.

• HOLD mode

The system enters the HOLD mode at the second falling edge of SDA data. Data is held in the shift register of an IC until the HOLD mode changes to LATCH mode. This servo IC has four addresses. After one address is being "HOLD"ed, all incoming data from this point of time until the triggering of LATCH pulse is nullified (ignored).

• LATCH mode

The system enters the LATCH mode at the third falling edge of SDA data. Data is then output from the shift register of an IC to the IC control register.

Through the combination of the HOLD and LATCH modes, this servo IC can be synchronized with multiple other ICs by only one-word instruction.

1.2 Format

1.2.1 Timing Chart: In this servo IC, the synchronized serial bus consists of 8 bits in an address block and 16 bits in a data block as shown below. Only the data length (or plus Don't Care) is sent on the transmission side.

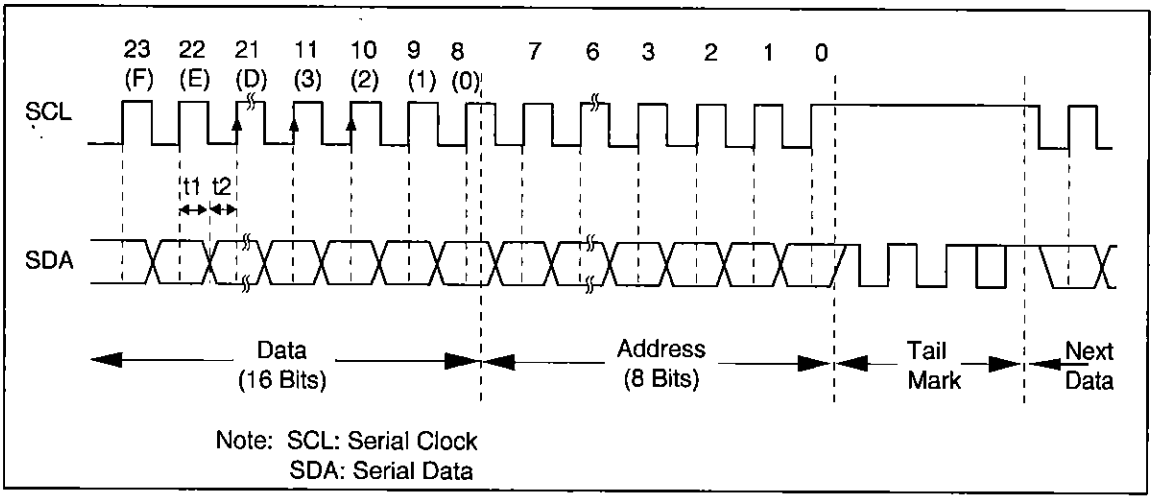


Figure 1 Timing Chart

1.2.2 Tail Mark

• **HOLD mode**

The system enters the HOLD mode at the second falling edge of SDA data while the SCL clock is high. Data is held in the shift register of an IC until the HOLD mode changes to LATCH mode.

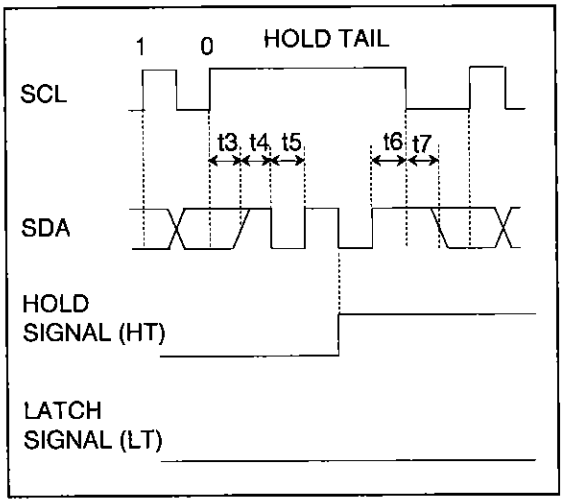


Figure 2 HOLD Mode

• **LATCH mode**

The system enters the LATCH mode at the third falling edge of SDA data while the SCL clock is high. Data is output from the shift register of an IC to the IC control register.

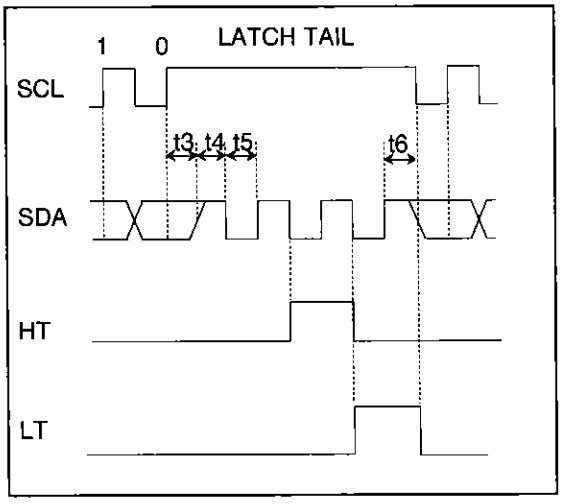


Figure 3 LATCH Mode

1.2.3 Timing (Servo IC only)

$t1 \geq 0.5\ \mu s$, $t2 \geq 0.5\ \mu s$, $t3 \geq 0.5\ \mu s$, $t4 \geq 0.5\ \mu s$
$t5 \geq 0.5\ \mu s$, $t6 \geq 0.5\ \mu s$, $t7 \geq 0.5\ \mu s$

1.3 Examples of Realization Methods of Tail Mark Circuitry

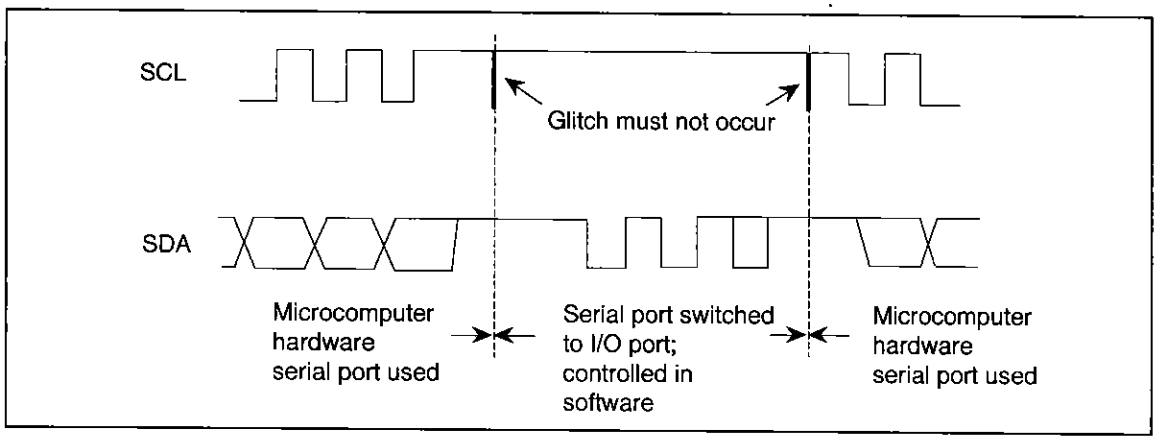


Figure 4 Method 1

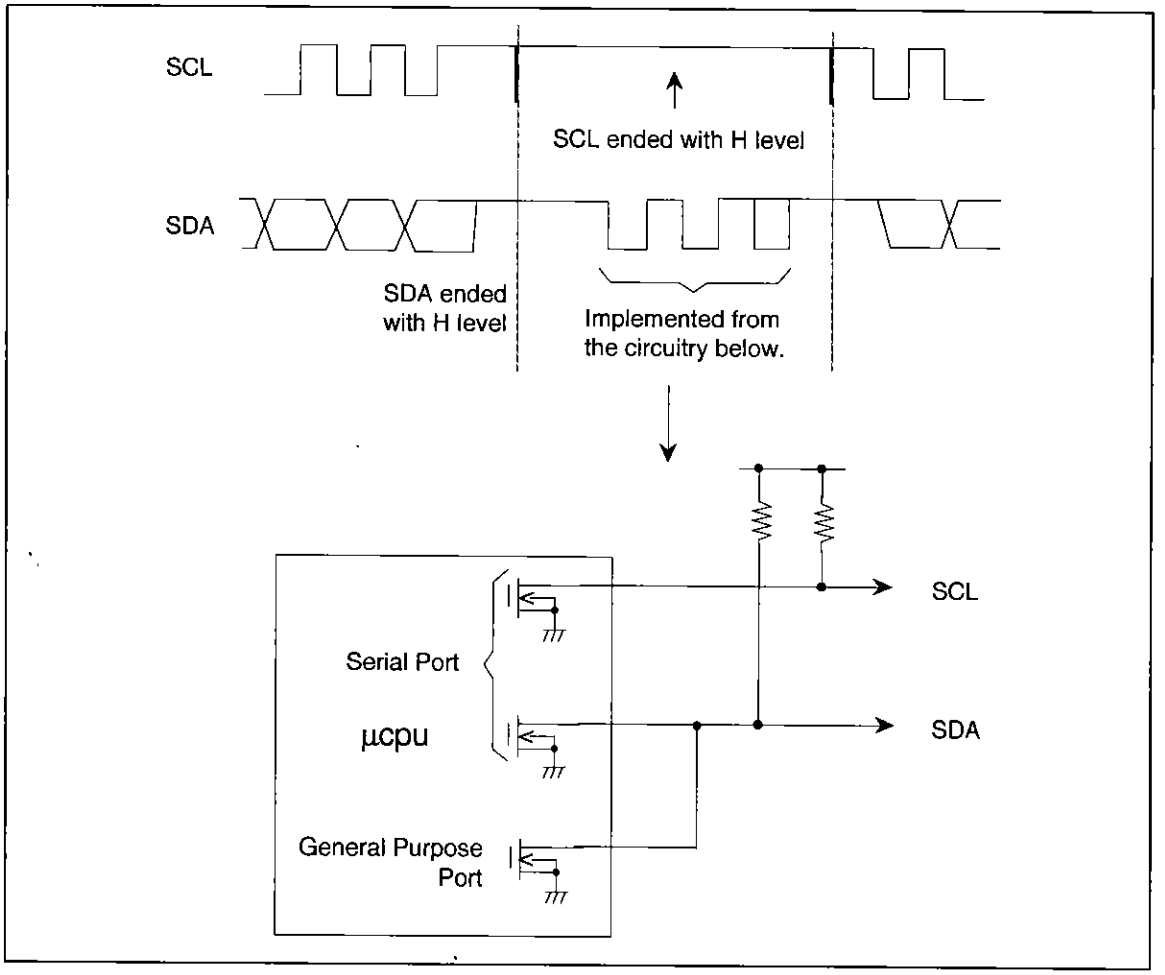


Figure 5 Method 2

1.4 Servo IC Internal Registers' Address Assignment

Bit	MSB														LSB	ADDRESS							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRUM ON	CAP ON	SEARCH SPEED (X1 to X63)								SW 12	SW 8	F/R	fH Corr.	PB/REC/ ASBL/ INST	SP / LP / EP	0	0	0	0	0	0	1	1
	VISS/VASS		VP M CUT	VP ON	VP DIR	VP SHIFT SEL.	VP SHIFT LENGTH		VP POSITION MSB							LSB	1	0	0	0	0	0	1	1
	MSB CTL DLY DATA															LSB	MODE OUT SEL.			WA/ WA	0	1	0	0	0	0	1	1
	VP POL	VP +6H	DPD FIX	CPD FIX	SW 13	NTSC PAL	SLOW A/B	FIELD DET	MSB REC SW POINT DATA							LSB					1	1	0	0	0	0	1	1

Figure 6

SSB Serial Table

DATA * MSB FIRST

MSB F E D C	B A 9 8	7 6 5 4	3 2 1 0 LSB	(ADDRESS = 00000011)		
			0 0	SP		
			0 1	LP		
			1 0	EP		
		0 0		REC		
		0 1		ASB		
		1 0		INST		
		1 1		PB		
		0 1 1		f_H CORRECTION	OFF	(DPD ON)
		1 1 1		f_H CORRECTION	ON	(DPD OFF)
		0 0 0		A. FF	OFF	
		0 0 1		A. FF	OFF	
		0 1 0		A. FF	OFF	
		1 0 0		A. FF	ON	
		1 0 1		A. FF	ON	
		1 1 0		A. FF	ON	
	0			FWD		
	1			REV		
	0			SW(8)	OFF	(FB SW of Pin 25 and 26)
	1			SW(8)	ON	
0				SW(12)	OFF	(FB SW of Pin 34 and 35)
1				SW(12)	ON	
* * * * * *				SEARCH SPEED		(NTSC/PAL.SP/LP/EP common)
0 0 0 0 0 0				SLOW		
0 0 0 0 0 1				X1		
0 0 0 0 1 0				X2		
|				|		
1 1 1 1 1 0				X62		
1 1 1 1 1 1				X63		
0				MOTOR	STOP	(CAP)
1					START	(CAP)
0				MOTOR	STOP	(DRUM)
1					START	(DRUM)

SSB Serial Table (cont)

* MSB FIRST

DATA MSB LSB F E D C B A 9 8 7 6 5 4 3 2 1 0	(ADDRESS =10000011)	
1	VISS REC FF RESET	
0	VISS REC FF RESET	
0 0	VASS Mode	Duty DET Mode
1 1 1	VASS Mode	WRITE Mode
1 1 0	VISS Mode	VISS REC Mode
0 1	VISS Mode	VISS DET Mode
1 0	VISS Mode	VISS DET FF RESET
* * * * *	V.P. POSITION DATA	
0 0 0	V.P. SHIFT	Length 0.0H
0 0 1	V.P. SHIFT	Length 0.5H
0 1 0	V.P. SHIFT	Length 1.0H
0 1 1	V.P. SHIFT	Length 1.5H
1 0 0	V.P. SHIFT	Length 2.0H
1 0 1	V.P. SHIFT	Length 2.5H
0 0	V.P. SHIFT SEL	CH1 FIXED / CH2 FIXED
0 1		FIXED / SHIFT
1 0		SHIFT / FIXED
1 1		SHIFT / SHIFT
0	V.P. SHIFT	Direction (+)
1	V.P. SHIFT	Direction (–)
0	V.P.	OFF
1	V.P.	ON
0	V.P.	MONITOR CUT OFF
1	V.P.	MONITOR CUT ON

SSB Serial Table (cont)

DATA * MSB FIRST

MSB												LSB	
F	E	D	C	B	A	9	8	7	6	5	4	3 2 1 0	**(ADDRESS = 01000011)**
												1	WIDE ASPECT (WA) MODE
												0	$\overline{\text{WA}}$ MODE

				MODE OUT					
				A	B	C	D	E	F
				Pin 1	Pin 2	Pin 3	Pin 56	Pin 55	Pin 54
			0					CTL C/D	CFG C/D
		0	1					0	CFG
		1	1					1	CFG
	0	0					NOISE DET		
	1	0					M-FF		
	0	1					0		
	1	1					1		
0						0			
1						1			
	0				0				
	1				1				
0				0					
1				1					

*	*	*	*	*	*	*	*	CTL DELAY DATA

SSB Serial Table (cont)

DATA * MSB FIRST

MSB															LSB	
F	**E**	**D**	**C**	**B**	**A**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**(ADDRESS =11000011)**
								*	*	*	*	*	*	*	*	REC SW POINT DATA
								0	0	0	0	0	0	0	0	ANALOG MM ON
								0	0	0	0	0	0	0	1	SW.P DATA/ANALOG MM OFF
										|				|		
								1	1	1	1	1	1	1	1	
							0									FIELD DET OFF
							1									FIELD DET ON
						0										SLOW A
						1										SLOW B
					0											SYSTEM SEL PAL
					1											SYSTEM SEL NTSC
				0												SW(13) OFF (SW of Pin 37)
				1												SW(13) ON
			0													P/D FIX OFF (CAP)
			1													P/D FIX ON (CAP)
		0														P/D FIX OFF (DRUM)
		1														P/D FIX ON (DRUM)
	0															V.P. SEL NOR
	1															V.P. SEL +6H
0																V.P. POLARITY H: PEDESTAL M: SYNC
1																V.P. POLARITY H: SYNC M: PEDESTAL

2. DRUM System Specification

2.1 DRUM Speed System's Constants

	DFG Frequency	S/H Frequency	Counter Clock	Counter Bit	FV-Gain	DRUM PD $\overline{ADJ}$
NTSC	359.61 Hz	359.61 Hz	fsc/3	12 bit	40.5 mV/%	312 Hz to 425 Hz
PAL	300.00 Hz	300.00 Hz	fsc/4	12 bit	45.1 mV/%	264 Hz to 348 Hz

2.2 DRUM Phase System's Constants

		S/H Frequency	Counter Clock	Counter Bit	PD Gain
NTSC	Phase detection	29.97 Hz	fsc/4	12 bit	1.092 V/ms
	fH correction	3.93 kHz	fsc/4	11 bit	2.184 V/ms
PAL	Phase detection	25.00 Hz	fsc/4	12 bit	1.353 V/ms
	fH correction	3.91 kHz	fsc/4	11 bit	2.706 V/ms

2.3 Drum P/D FIX System

1) P/D OUT FIX
P/D OUT signal is fixed at 1/2 Vcc when the DP/D FIX system is turned on by serial data.

2) SW1 On condition
Switch SW1 is on for the following conditions:
- In states other than fH correction and when the drum speed exceeds the range of Drum Speed System Constant DRUM PD $\overline{ADJ}$ in table 2-1.
- When COMP SYNC no-signal is detected or when noise is detected during fH correction.

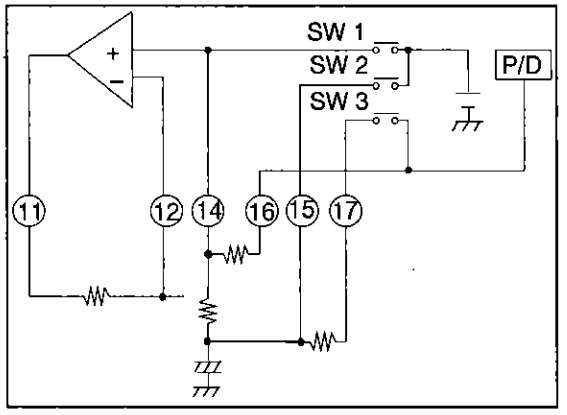


Figure 7 DRUM P/D FIX System

2.4 fH Correction System

1) fH correction accuracy
NTSC 63.5556 µs (discrepancy: 0)
PAL 63.9996 µs (discrepancy: −1/625 fsc sec)

2) fH correction
- The drum reference counter is forcibly synchronized with DRUM Head SW.
- Switch SW2 is off and switch SW3 is on.
- An H DISCRI error is output to the PD OUT pin.

3) fH correction cancellation
- Switch SW3 is off.
- Switch SW2 remains on until the time shown below after the fH correction is cancelled.
NTSC 67 to 100 ms
PAL 80 to 120 ms

3. CAPSTAN System Specification

3.1 CAPSTAN Speed System's Constants

			CFG Frequency	S / H Frequency	Counter Clock	Counter Bit	FV Gain
NTSC	NORMAL		SP	2157.8 Hz	fsc	11 bit	40.5 mV/%
			LP	1078.9 Hz	fsc/2		
			EP	719.3 Hz	fsc/3		
	SLOW	SLOW A	SP	1618.4 Hz	fsc	11 bit	54.0 mV/%
			LP	809.2 Hz	fsc/2		54.0 mV/%
			EP	539.5 Hz	fsc/3		54.0 mV/%
		SLOW B	SP	1163.3 Hz	fsc	11 bit	75.1 mV/%
			LP	809.2 Hz	fsc/2		54.0 mV/%
			EP	539.5 Hz	fsc/3		54.0 mV/%
PAL	NORMAL		SP	1513.4 Hz	fsc/2	11 bit	35.8 mV/%
			LP	756.7 Hz	fsc/4		
	SLOW	SLOW A	SP	1135.1 Hz	fsc/2	11 bit	47.7 mV/%
			LP	567.5 Hz	fsc/4		47.7 mV/%
		SLOW B	SP	756.7 Hz	fsc/2	11 bit	71.5 mV/%
			LP	567.5 Hz	fsc/4		47.7 mV/%

Note: F/V Center Correction (during search): The F/V center correction below is performed in fH correction mode. In search mode, FG is converted after FG pulse is decremented in the same ratio as for CTL pulse. The F/V-converted center frequency is corrected according to the speed as shown below.

fH Correction (Number of rotations)	NTSC SP	NTSC LP	NTSC EP
7.5%	From x9	From x18	From x28
3.3%	x3 to x8	x6 to x17	x10 to x27
0%	x2 to SLOW to x-2	x5 to SLOW to x-5	x9 to SLOW to x-9
–3.5%	x-3 to x-8	x-6 to x-17	x-10 to x-27
–7.1%	From x-9	From x-18	From x-28

fH Correction (Number of rotations)	PAL SP	PAL LP
8.7%	From x14	From x28
4.2%	x5 to x13	x10 to x27
0%	x4 to SLOW to x-4	x9 to SLOW to x-9
–4.5%	x-5 to x-13	x-10 to x-27
–8.1%	From x-14	From x-28

Home

3.2 CAPSTAN Phase System's Constant

		S/H Frequency	Counter Clock	Counter Bit	PD GAIN kP 1	PD GAIN kP 2
NTSC		29.97 Hz	fsc/8	11 bit	0.546 V/ms	1.639 V/ms
PAL	PB	25.00 Hz	fsc/8	11 bit	0.677 V/ms	2.030 V/ms
	REC	25.22 Hz				

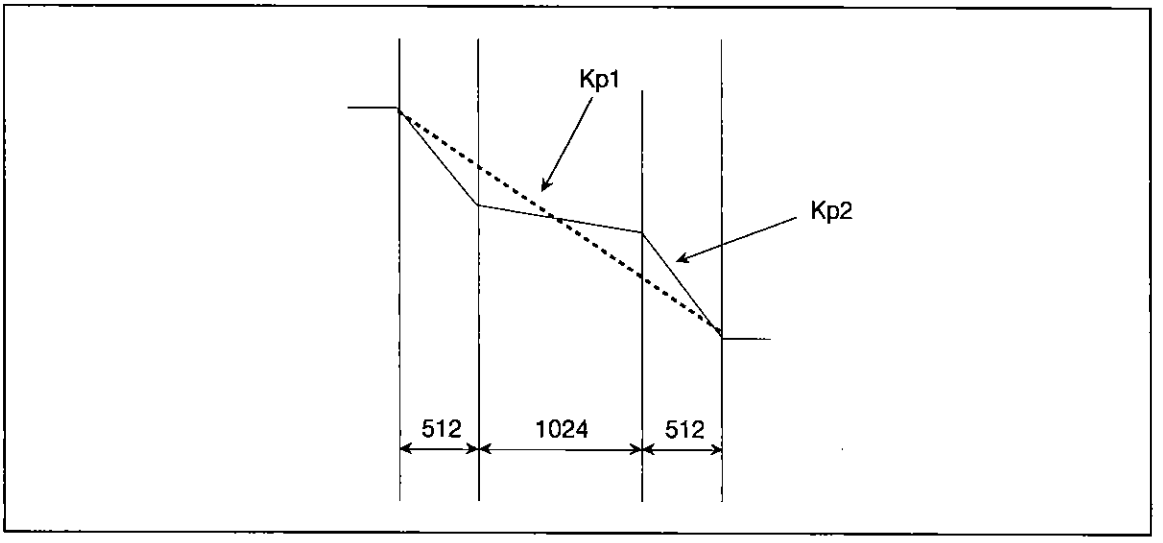


Figure 8 CAPSTAN Phase System's Constant

3.3 CAP P/D FIX System

1) For the conditions below, switch SW4 is on and the positive (+) input terminal of the mixing amplifier is fixed at 1/2 Vcc. But, the PD OUT terminal is not fixed. (PD error is output)
   - The capstan speed is shifted from the center by the ranges below.
     NTSC –7.17 to 8.35%
     PAL –8.05 to 9.56%
   - In PB mode, if CTL pulse is not detected until the following detection time.
     Detection time: NTSC 100 to 133 ms
     PAL 120 to 160 ms
   - The system is in SLOW speed mode.

2) The P/D OUT pulse is fixed at 1/2 Vcc when the CAP P/D FIX system is turned on by serial data.

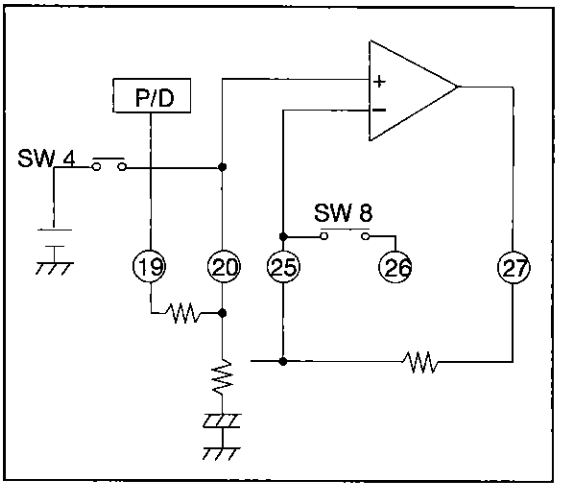


Figure 9

3.4 PB CTL Schmitt Level

• DC coupling of CTL amplifier and PB CTL Schmitt input must be performed to supply a bias to compensate the lack of an input bias.

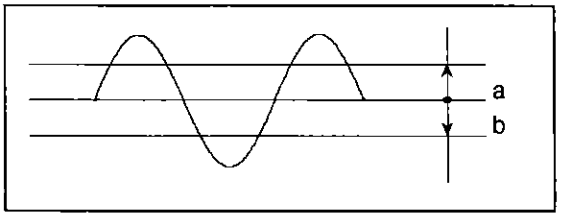


Figure 10

The VTHs below are available.

① +130 mV ±30 mV ② –130 mV ±30 mV
③ +260 mV ±60 mV ④ –260 mV ±60 mV
⑤ +500 mV ±80 mV ⑥ –500 mV ±80 mV

As shown in the table below, each VTH is set as a standard level according to the search speed.

VTH

		NTSC			PAL	
MODE	VTH a, b	SP	LP	EP	SP	LP
I	±130mV	SLOW	SLOW x 1	SLOW x 1	SLOW x 1	SLOW x 1
II	±260mV	x 1–x 2	x 2–x 5	x 2–x 9	x 1–x 4	x 2–x 9
III	±500mV	x 3–	x 6–	x 10–	x 5–	x 10–

VTH automatic selection: The VTH is set to the value with a higher sensitivity than the standard level by one step when a NO CTL pulse is detected. The VTH returns to the standard level when a Schmitt amplifier with a higher level than the standard value by one step is activated.

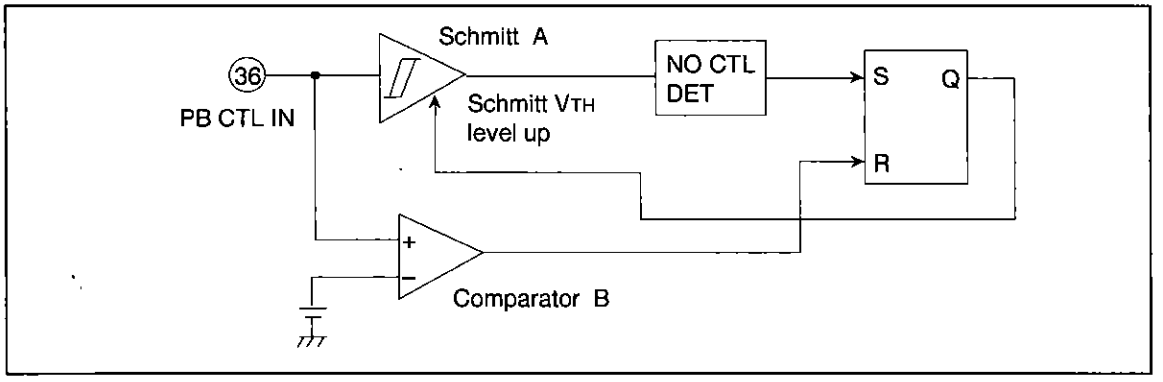


Figure 11

* In SLOW speed mode, the VTH is fixed to 130 mV.

MODE		I	II	III	
Comparator B		—	500 mV	1000 mV	Returns to the standard level
Schmitt A	Q = 0	130 mV	260 mV	500 mV	Standard level
	Q = 1	130 mV	130 mV	260 mV	After NO CTL pulse detection

3.5 Mixing Amplifier Gain Selection

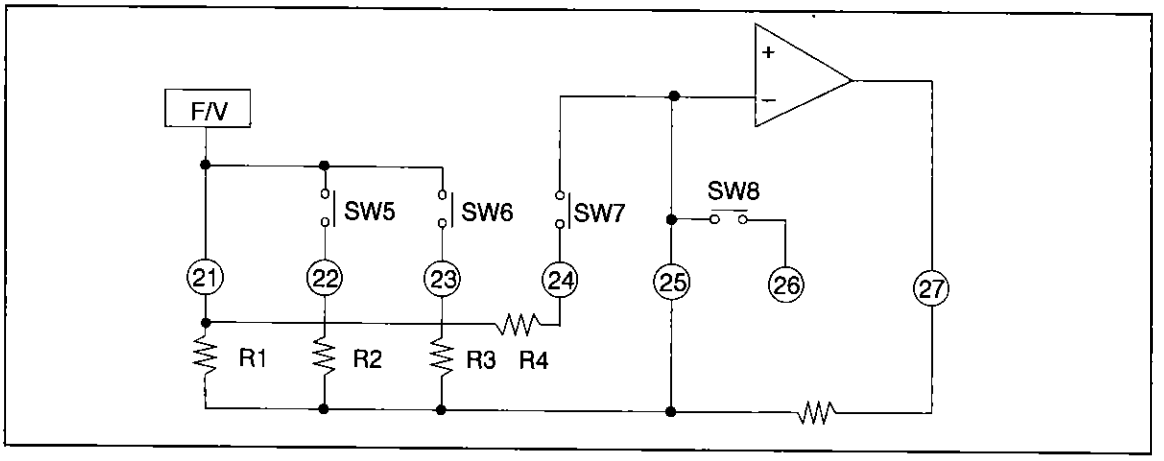


Figure 12

			NTSC			PAL	
SW5	**SW6**	**SW7**	**SP**	**LP**	**EP**	**SP**	**LP**
OFF	OFF	OFF	SLOW	SLOW	SLOW	SLOW	SLOW
OFF	OFF	OFF		x1	x1–x3		x1–x2
ON	OFF	OFF	x1–x2	x2–x5	x4–x9	x1–x4	x3–x9
ON	ON	OFF	x3–x8	x6–x17	x10–x27	x5–x13	x10–x27
ON	ON	ON	x9–	x18–	x28–	x14–	x28–

Switch SW8 is controlled by serial data. Each gain is selected in 10-dB steps. Therefore, R2 is R1/2, R3 is R1/6, and R4 is R1/18.

4. V Pulse

4.1 VP Output Conditions

- The V pulse is output when a PB*VP pulse is on.
- For the variable shift of t1, see the corresponding item.
- t3 is output only when VP +6H is specified. Without any specifications, it is set low.

4.2 VP Position

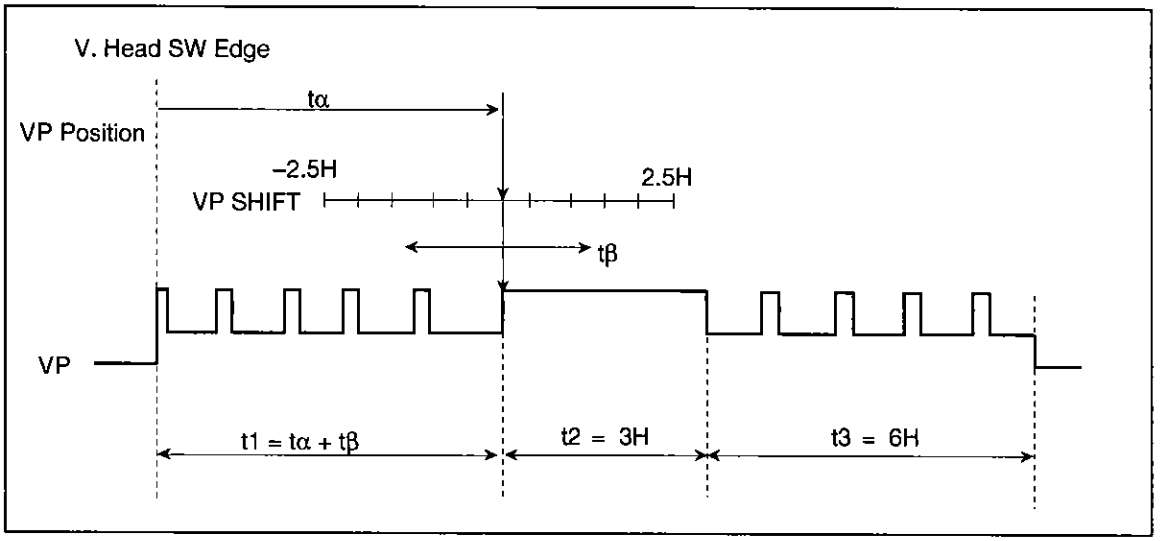


Figure 13

- **tα: VP Position**

In SLOW and two-times speed modes, the channels below can be changed. In other modes, both channels 1 and 2 are fixed.

Mode		CH-1	CH-2
2 Head		Fixed	Variable
DA - 4	SP	Fixed	Variable
	$\overline{SP}$	Variable	Fixed

Variable amount (depending on 5 bits (N) of serial data)

NTSC	64 (41.5−N) / fsc	≈ 3.0 H to 11.7 H
PAL	64 (43.75−N) / fsc	≈ 2.9 H to 9.9 H

Fixed amount approx. is 6.0H

4.3 VP Shift

- tβ: VP Shift

As described below, the VP shift amount, shift channel, and shift direction vary depending on the serial data.

VP shift amount

DATA									ADDRESS								
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	SHIFT Amount
	0	0	0	—	—	—	—	—	1	0	0	0	0	0	1	1	0.0 H
	0	0	1														0.5 H
	0	1	0														1.0 H
	0	1	1														1.5 H
	1	0	0														2.0 H
	1	0	1														2.5 H

VP shift channel and shift direction (⊕ is lagging direction)

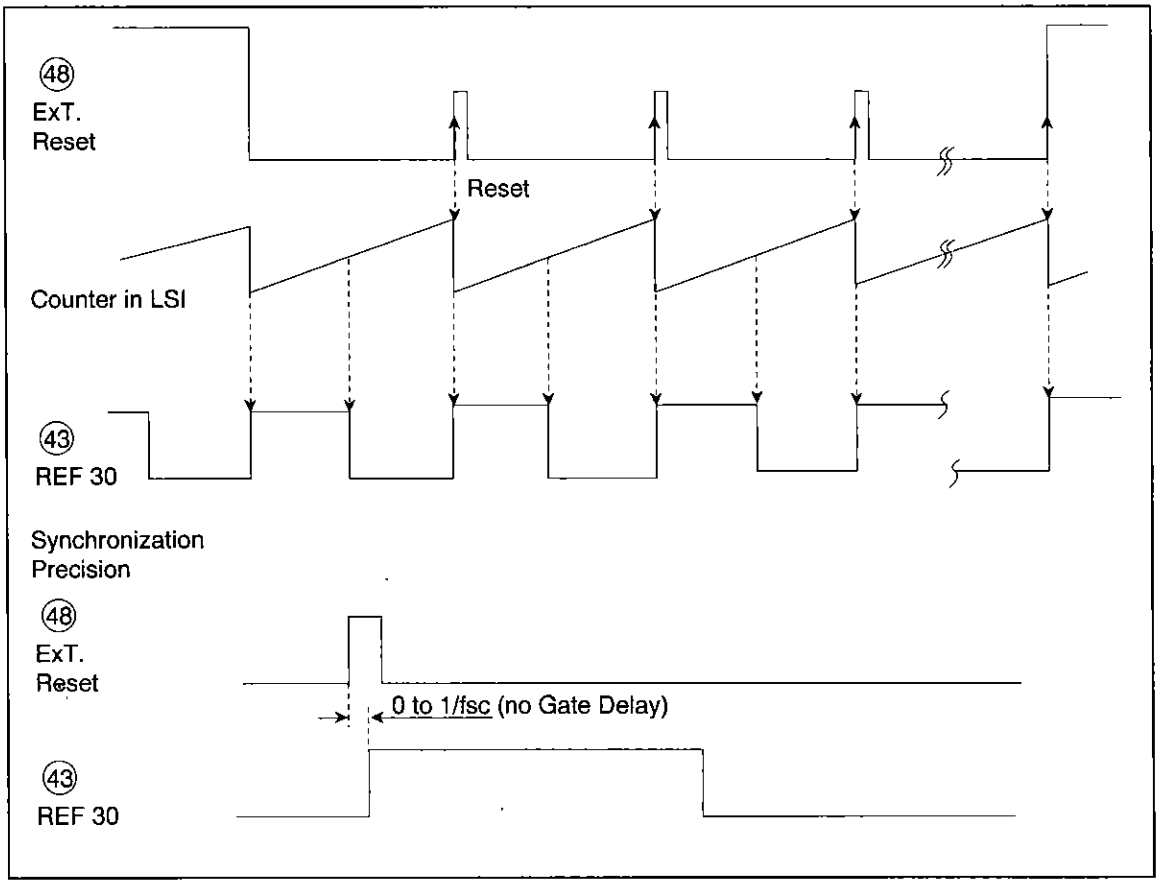
	DATA					ADDRESS								
Bit	A	9	8	7	6	7	6	5	4	3	2	1	0	CH-1	CH-2
	0	0	0	—	—	1	0	0	0	0	0	1	1	Fixed	Fixed
	1														
	0	0	1	—	—									Fixed	⊕ Shift
	1	0	1	—	—									Fixed	⊖ Shift
	0	1	0	—	—									⊕ Shift	Fixed
	1	1	0	—	—									⊖ Shift	Fixed
	0	1	1	—	—									⊖ Shift	⊕ Shift
	1	1	1	—	—									⊕ Shift	⊖ Shift

Note: To control the VP shift, the serial data is transmitted when no V pulse is output.

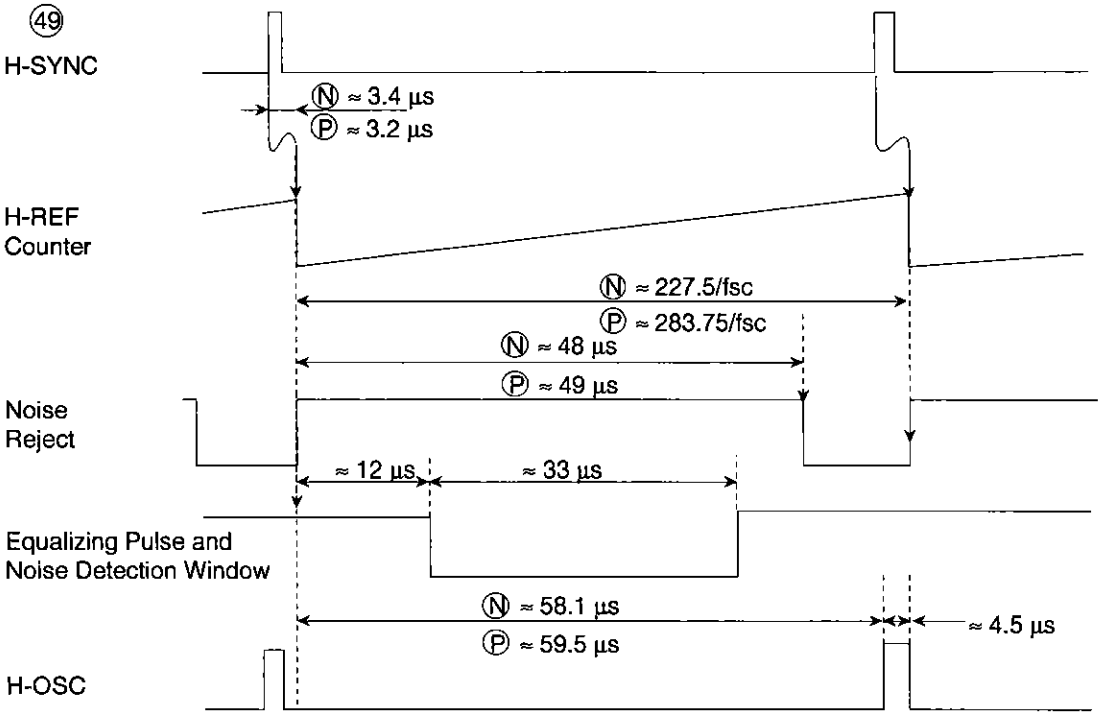
5. External Synchronization (EXT. RESET)

Pin			
(48)	H	In PB mode, synchronized with the internal reference period. In REC, ASBL, and INST modes, synchronized with the V-SYNC signal.	
	M	In all modes other than fH correction, this positive edge becomes a reference edge. It is not related to the V-SYNC signal or the internal reference period.	The negative edge is not related.
	L		

Timing Chart



6. H-OSC



Note: H-OSC is output with the additional V-pulse.
H-OSC contains a jitter of one clock for every fsc even if an external H-SYNC signal is stable.

7. Noise Det. & Field Det.

Noise in the COMP-SYNC signal is detected as follows:

1) Noise detection
   Detects whether the noise in an H-SYNC signal exceeds the specified amount.
2) H-SYNC detection
   Detects whether the loss of an H-SYNC signal exceeds the specified amount.

The operation below is performed when a noise detector is activated (noise is detected).

1) A high signal is output to the output pin (pin 56) of noise detector.
2) A synchronous reset pulse sent from V-SYNC to REF 30 is stopped.
3) In f_H correction mode, the f_H correction error output is adjusted.

8. REC CTL Duty Cycle and Duty I/O

In REC mode, the REC CTL duty cycle is determined by the modes and duty I/O below.

	WIDE ASPECT	VISS/ VASS	INDEX REC	DUTY I/O	CTL DUTY (%)	Remarks
①	NOT	VISS	NOT	H	62.5	
				L	70.0	Note 1
②	NOT	VISS	BUSY	H (OUT)	62.5	Note 2
				L (OUT)	30.0	
③	NOT	VASS	CAN NOT	H	62.5	Note 3
				L	30.0	
④	YES	VISS	NOT	H	57.5 or 62.5	Note 4
				L	70.0	Note 1
⑤	YES	VISS	BUSY	H (OUT)	57.5 or 62.5	Note 5
				L (OUT)	25.0 or 30.0	
⑥	YES	VASS	CAN NOT	H	57.5 or 62.5	
				L	25.0 or 30.0	

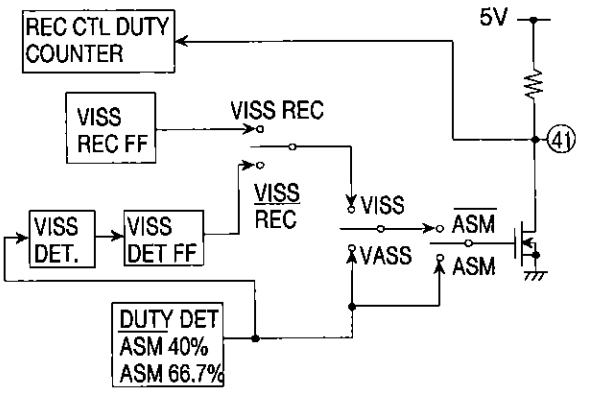
Notes: 1. ASM mark
2. Duty I/O enters the output mode.
3. In VASS mode, no ASM mark is used.
4. Recorded by an LLSS pattern.
5. Duty I/O enters the output mode. An LLSS pattern is continued even if the high and low levels of the duty I/O are selected.

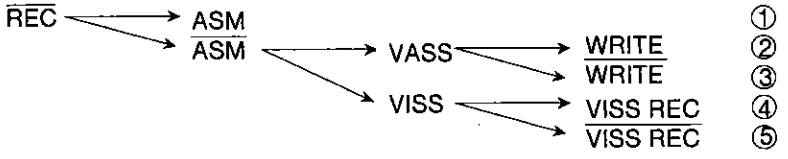
* In back-space editing mode, the LLSS pattern is not continued.

9. Duty I/O

Output Format : Pull-up of approximately 10 kΩ

Operation : Five modes are used in this case. The operation for each mode is explained below. For the REC mode, see section 8.





Home

① ASM mode
An ASM mark is detected and output. The duty I/O is set low during ASM mark detection.
The threshold level is 66.7%.
* The VISS/VASS function is not activated.

② $\overline{\text{ASM}}$*VASS*WRITE mode
Duty rewrite mode. This mode is determined by the rewrite of DUTY I/O level.
L: DUTY, $\overline{\text{WA}}$: 30%, WA: (S)25 or (L)30%
H: DUTY, $\overline{\text{WA}}$: 62.5%, WA: (S)57.5 or (L)62.5%
* Pin 41 is set high.
* The I/D LLSS pattern in a wide aspect ratio is not continued before and after the rewrite point when a duty cycle is rewritten. The LLSS pattern is only continued during continuous rewrite.

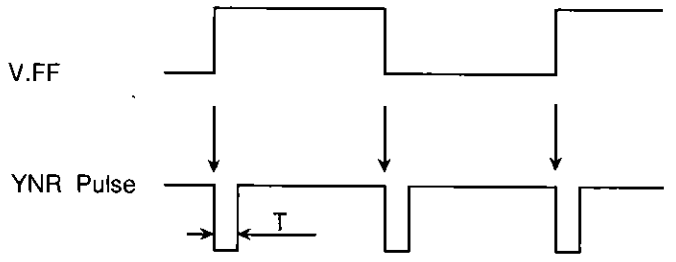
③ $\overline{\text{ASM}}$*VASS*$\overline{\text{WRITE}}$ mode
A duty cycle is detected and output. The duty I/O is set low when the duty cycle is less than 40%.

④ $\overline{\text{ASM}}$*VISS*VISS REC mode
Duty rewrite mode. In this mode, VISS is written. An IC automatically determines the write duty cycle by controlling the low and high signals at pin 41. An LLSS pattern is continued even if the low and high levels of the duty I/O change. However, it is not continued before and after the write point.

⑤ $\overline{\text{ASM}}$*VISS*$\overline{\text{VISS REC}}$ mode
Index detection mode. The duty I/O is latched low when VISS is detected.
Presetting this mode requires the serial operation.

Note: The result of a duty cycle immediately after a mode is selected is undefined. To define the duty cycle, a minimum of one cycle and a maximum of two cycles are required.

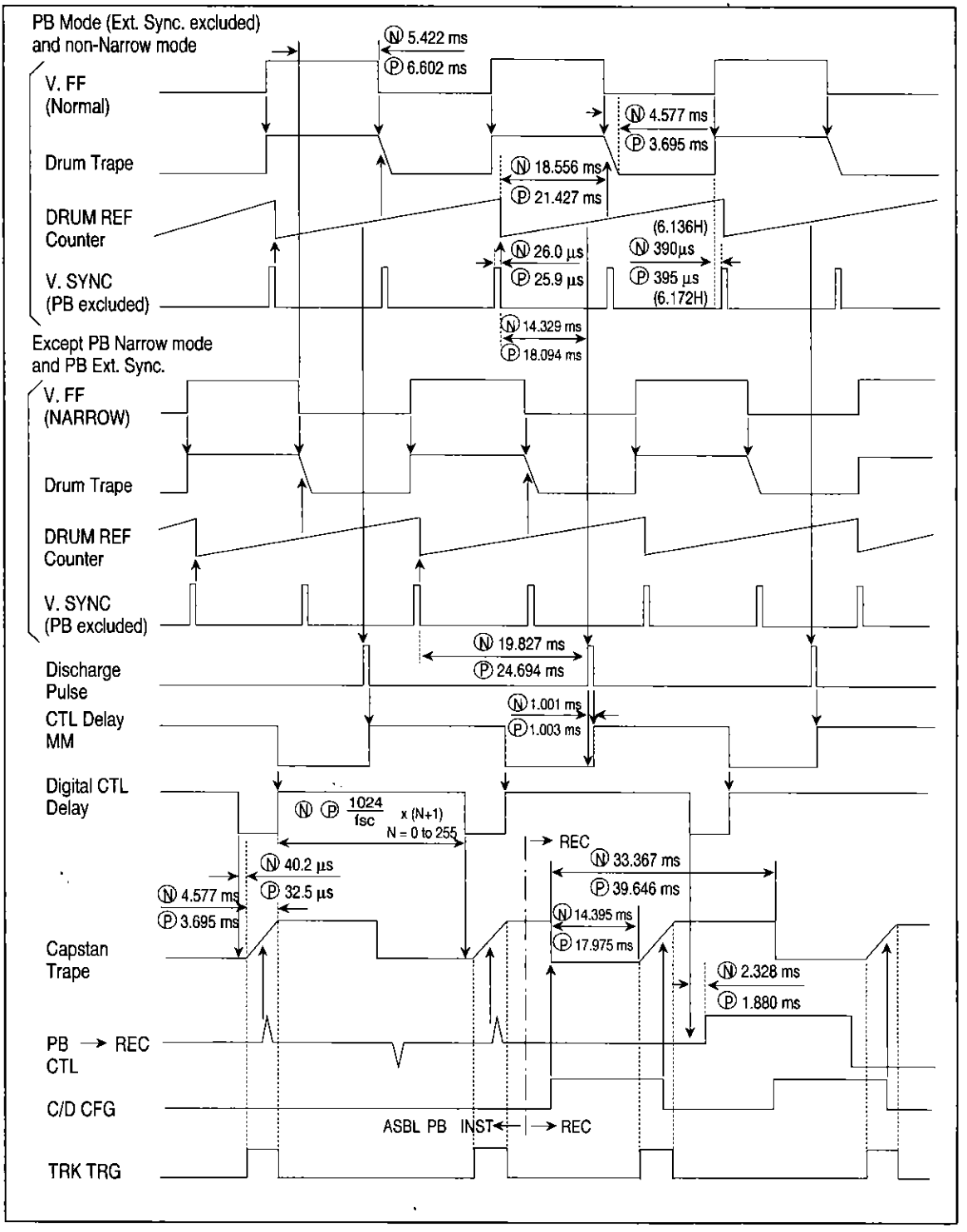
10. YNR Pulse



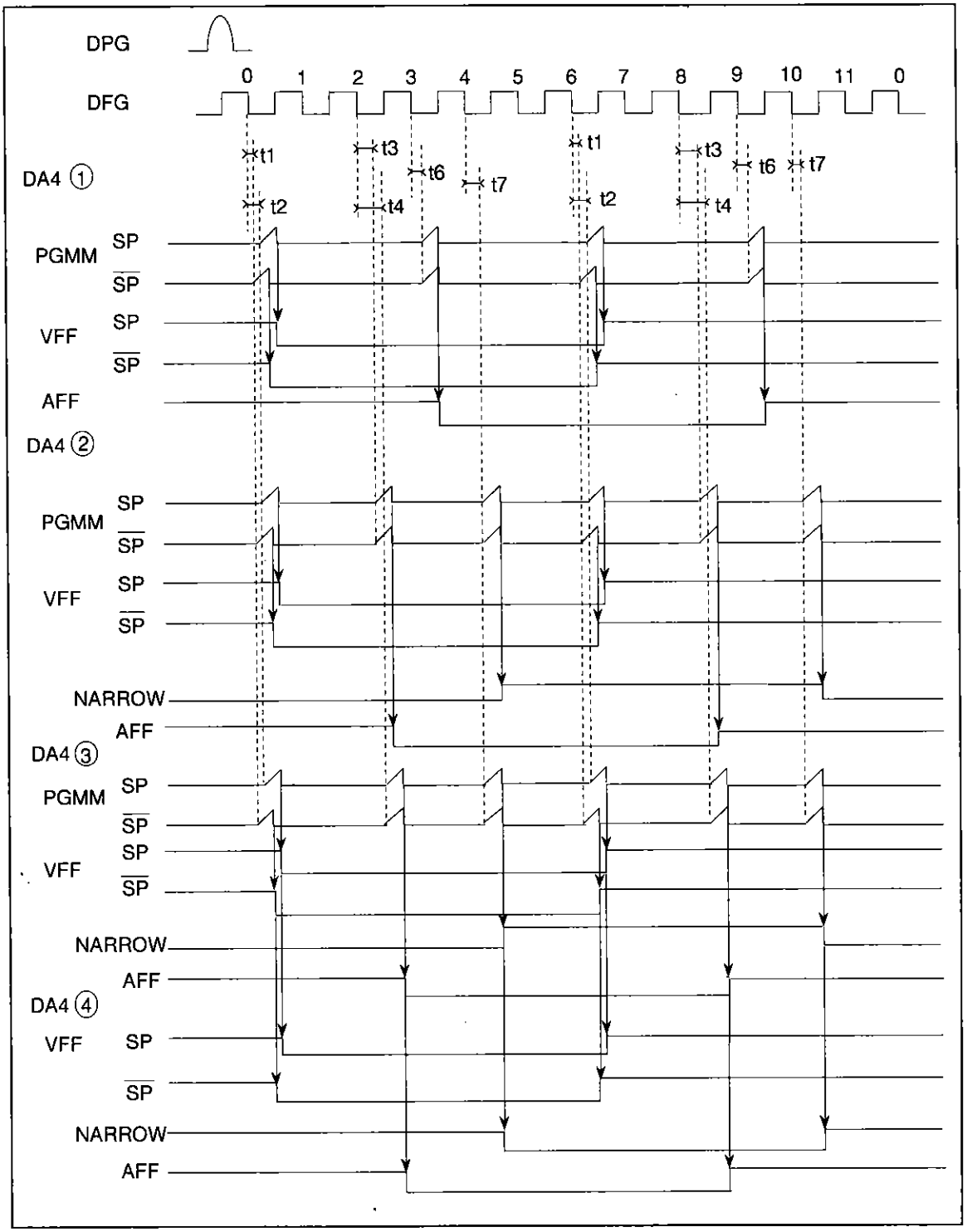
T: NTSC approximately 1.600 ms
PAL approximately 1.616 ms

CMOS output at ±2 mA H: min 3.8 V
L: max 1.2 V

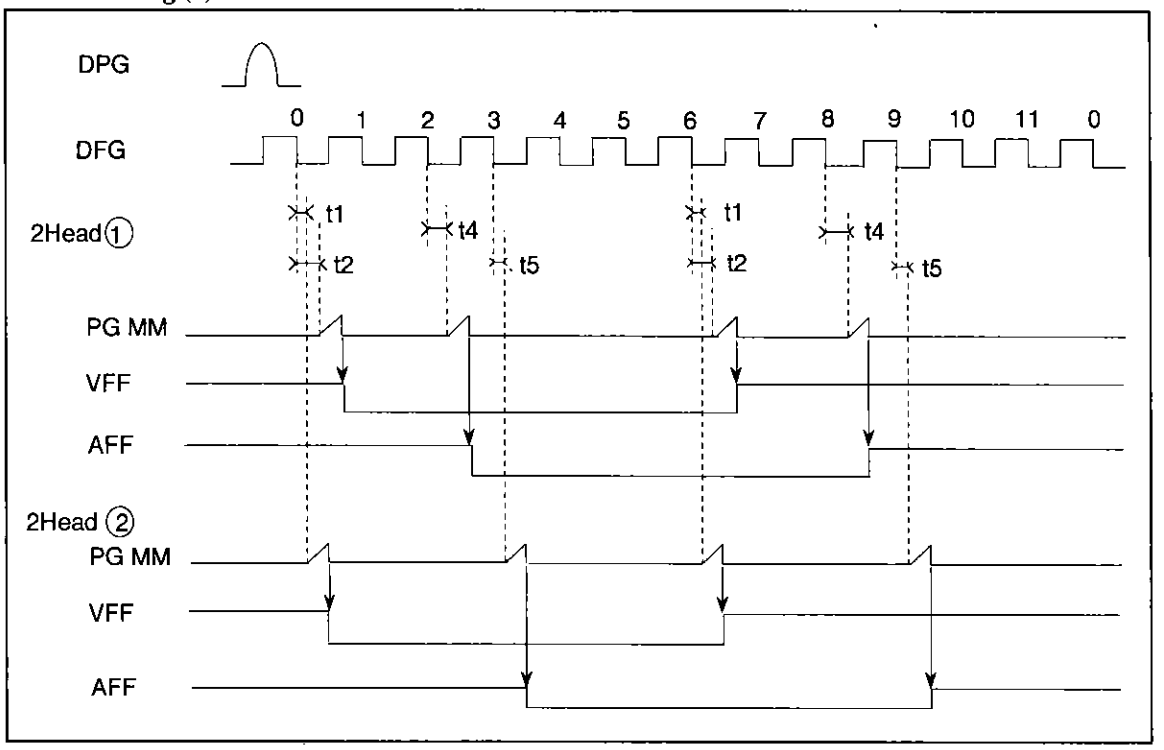
Timing Chart



HSW Timing (1)



HSW Timing (2)



(Unit: µs)

Mode	PGMM	t1	t2	t3	t4	t5	t6	t7
NTSC	CR	10.9	136.1	73.5	136.1	10.9	73.5	73.5
	Digital	234.4	360.0	297.0	360.0	234.4	297.0	297.0
PAL	CR	8.8	138.7	73.8	138.7	8.8	73.8	73.8
	Digital	737.8	867.7	802.7	867.7	737.8	802.7	802.7

Delay (T) of Digital PGMM is calculated from formula below.

$T = (36 + 32 \times N) / fsc$
N: 1 to 255 (serial data)

Drum Select

Pin 10 \ Pin 9	H	M	L
H	2Head ①	2Head ②	DA4 ④
M	DA4 ①	DA4 ②	DA4 ③
L	DA4 ① TEST	DA4 ② TEST	DA4 ③ TEST

Test: CFG is count-downed by 1/2

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Maximum supply voltage	Vcc Max	7.0	V
Operating supply voltage	Vopr	4.5 to 6.0	V
Storage temperature	Tstg	–40 to +125	°C
Operating temperature	Topr	–10 to +70	°C
Power dissipation	P_T	500	mW
Pin max. applied voltage		0 to Vcc	V

Electrical Characteristics (Ta = 25°C, VCC = 5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Application Terminal	Test Circuit
Supply current	ICC	8.0	20.0	32.0	mA	No Load Pin 28 & 39 Total	28, 39	
Binary output voltage	VOL	—	0.0	0.05	V	No Load	1 to 3, 43 to 46, 53 to 56	
		—	0.3	0.8	V	Load Current = 2 mA		
	VOH	4.9	5.0	—	V	No Load		
		4.2	4.7	—	V	Load Current = –2 mA		
Pull-up output voltage	VOL	0.0	0.1	0.3	V	No Load	40, 41	
		—	0.4	0.8	V	Load Current = 2mA		
	VOH	4.9	5.0	—	V	No Load		
Pull-up resistance	RH	4.5	9.0	13.5	kΩ			
Ternary output voltage	VOL	0.0	0.1	0.3	V	No Load	47	
		—	0.4	1.0	V	Load Current = 2mA		
	VOH	4.7	4.9	5.0	V	No Load		
		4.0	4.6	—	V	Load Current = –2mA		
	VOM	2.4	2.5	2.6	V	No Load		
Ternary output Output impedance	RM	4.5	9.0	13.5	kΩ			
REC CTL output Pin-to-pin voltage	VCTL	4.3	4.6	4.9	V	No Load voltage between Pin 29 & 30	29, 30	
REC CTL Output impedance	RCTL	300	450	750	Ω	I ≤ 3mA Pin 29 & 30 Total		
Binary inputVTH	VTH	1.5	2.5	3.5	V		18, 41, 51, 52	
Binary input Pull-up resistance1	RH1	4.5	9.0	13.5	kΩ		41, 51, 52	
Binary input Pull-up resistance2	RH2	14.0	28.0	42.0	kΩ		18	

Electrical Characteristics (Ta = 25°C, V_{CC} = 5 V) (cont)

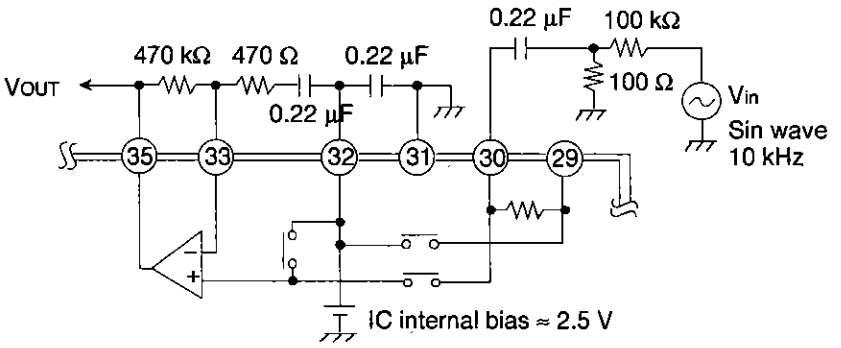
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Application Terminal	Test Circuit
Ternary input V_{TH}	V_{TH1}	1.0	1.4	1.9	V	L/M V_{TH}	9, 10, 48	
	V_{TH2}	3.1	3.5	4.0	V	M/H V_{TH}		
Ternary input Pin voltage	V_M	2.1	2.5	2.9	V			
Ternary input Input impedance	R_{M1}	17.3	34.5	51.8	kΩ			
fsc input Sensitivity	V_{ISC}	—	—	150	mVpp		42	
CTLP schmitt Input V_{TH}	V_{+TH1}	100	130	160	mVp	Normal speed	36	
	V_{-TH1}	−160	−130	−100	mVp			
	V_{+TH2}	200	260	320	mVp	Medium-speed search		
	V_{-TH2}	−320	−260	−200	mVp			
	V_{+TH3}	420	500	580	mVp	High-speed search		
	V_{-TH3}	−580	−500	−420	mVp			
Schmitt input Pin voltage 1	V_{IS1}	2.2	2.6	3.0	V		8	
DFG schmitt Input V_{TH}	V_{+TH}	120	190	250	mVp			
	V_{-TH}	−30	0	30	mVp			
DFG schmitt Input impedance	R_{M2}	18.5	37.0	55.5	kΩ			
DPG schmitt Pin voltage 2	V_{IS2}	1.7	2.1	2.5	V		6	
DPG schmitt Input V_{TH}	V_{+TH}	0.4	0.5	0.6	V			
	V_{-TH}	0.1	0.2	0.3	V			
DPG schmitt Input impedance	R_{M3}	20.5	41.0	61.5	kΩ			
CFG schmitt Pin voltage 3	V_{IS3}	2.3	2.5	2.7	V		38	
CFG schmitt Input V_{TH}	V_{+TH}	60	80	100	mVp			
	V_{-TH}	−10	0	10	mVp			
CFG schmitt Input impedance	R_{M4}	15.0	30.0	45.0	kΩ			
Analog SW On resistance	R_{ASW}	150	300	500	Ω		16 to 17, 21 to 23, 24 to 26, 34 to 35	

Electrical Characteristics (Ta = 25°C, V_{CC} = 5 V) (cont)

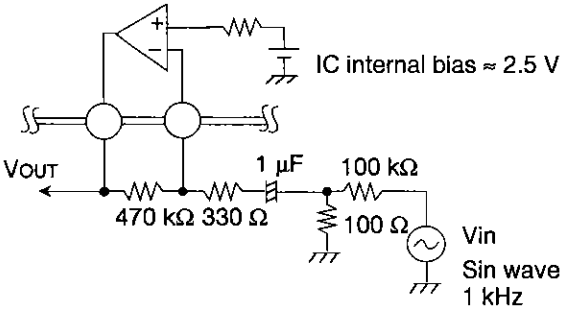
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Application Terminal	Test Circuit
Power on reset Input V_{TH}	V_{50TH}	1.0	1.5	2.0	V		50	
Power on reset Pull-up resistance	R_{50}	21.8	43.5	65.3	kΩ			
SYNC input V_{TH}	V_{49TH}	1.2	1.8	2.4	V	DC input	49	
SYNC input Pin voltage	V_{49}	0.8	1.3	1.8	V			
SYNC input Input sensitivity	V_{SYNC}	300	500	700	mVp	Capacitive coupling Pin peak voltage		
SYNC input Input impedance	R_{49}	15.3	30.5	45.8	kΩ			
Mono-multi V_{TH}		—	2.5	—	V	V_{TH} of each Mono-multi	4, 5	
CTLP AMP gain	A_{CTL}	56	60	62	dB	f = 10 kHz		1
	A_{CTLO}	—	85	—	dB	Open loop gain		
DRUM AMP gain	A_D	57	60	62	dB	f = 1 kHz		2
	A_{DO}	—	85	—	dB	Open loop gain		
CAPSTAN AMP gain	A_C	57	60	62	dB	f = 1 kHz		2
	A_{CO}	—	85	—	dB	Open loop gain		

Test Circuit

1.



2.



$$\text{Gain} = 20 \log \frac{Vout}{Vin} + 60 \text{ dB}$$

fsc input circuitry