Ordering number : 1171A

SANYO Semiconductors

DATA SHEET

LC7131/7135 LC7136/7137

C MOS LSI

PLL Frequency Synthsizer LSI for 27MHz CB Transceivers

Use

PLL frequency synthesizer LSI for 27MHz CB transceivers (U.S. standard, 40ch: LC7131), (European standard, 22ch: LC7135), (U.K. standard, 40ch: LC7136, 37)

Functions, features

1. Built-in high speed programmable divider for direct PLL system.
2. PLL out-of-lock output available to inhibit transmittion.
3. Instantaneous call capability of channel 9 and 19.
4. Built-in detecting circuit of mis-program.
5. Built-in amplifier for crystal oscillator.
6. Built-in amplifier for active low-pass filter.
7. BCD code channel selection. (Pull-down resistors included)

Description of functions

Digital Out-of-Lock Output

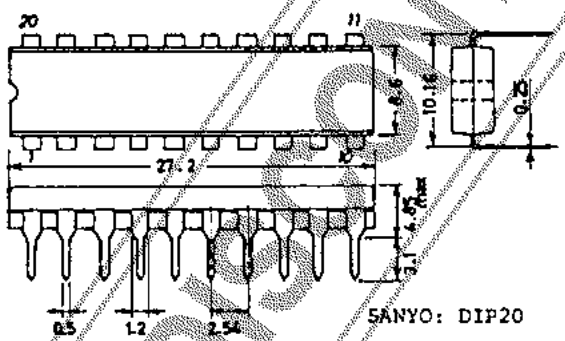
In direct PLL system, phase difference signal's pulse width at channel change is too narrow, so it is difficult to get out-of-lock signal from phase detector in the way of using C, R components externally.

LC7131, 7135, 7136 and 7137 make it possible to output the out-of-lock signal to have digital discriminate-expander of the pulse from phase detector internally (Detects the phase difference signal over 1.6μs pulse width, and makes it expand to 6ms output pulse).

And also LC7131, 7135, 7136 and 7137 output the out-of-lock signal when the phase difference signal is within 1.6μs to have the detector of channel change input.

Case Outline 3021B-D20SIC
(unit:mm)

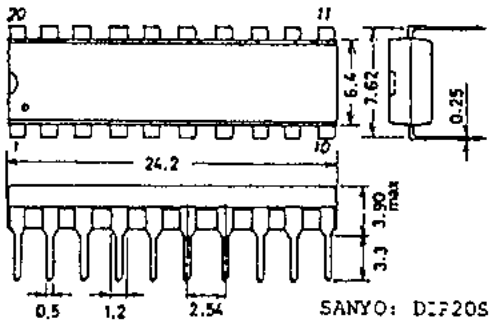
[LC7131/35/36]



SANYO: DIP20

Case Outline 3008A-D20IC
(unit:mm)

[LC7137]



SANYO: DIP20S

These specifications are subject to change without notice.

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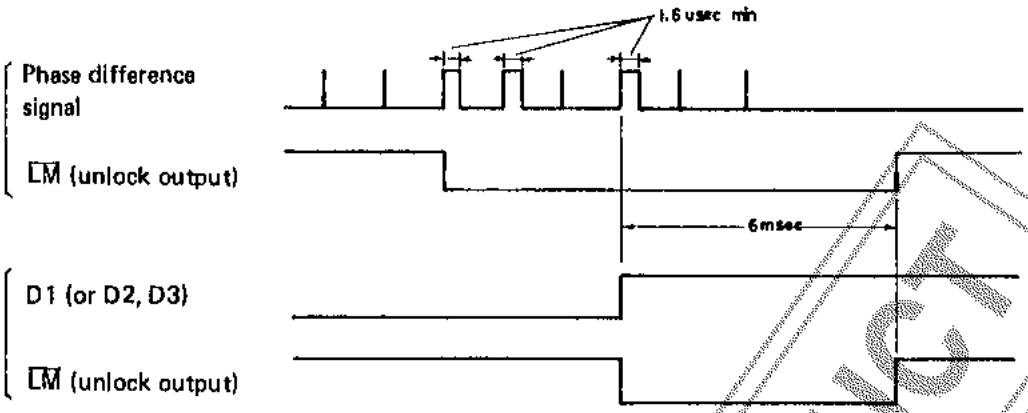


Instantaneous call of channel 9, 19 and recourse against miscode.

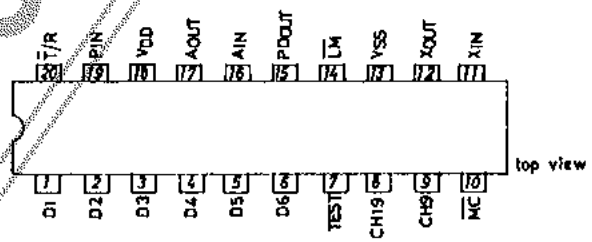
- Setting CH9 at "H" level causes channel 9 and setting CH19 at "H" level causes channel 19 to be selected.
- Inputting miscode to D1 to D6 causes channel 9 to occur, and $\overline{MC}$ output to be "L" level.
- The following table shows the transmitting/receiving channel corresponding to the combination of D1 to D6 and CH9 , 19.

Input			Output	
Data of D1 to D6	CH19	CH9	Channel	$\overline{MC}$
BCD code 0 to 39 (LC7131/36/37) 1 to 22 (LC7135)	0	0	Channel depending on D1 to D6	1
	0	1	Channel 9	1
	1	0	Channel 19	1
	1	1	Channel 19	1
Error program	0	0	Channel 9	0
	0	1	Channel 9	1
	1	0	Channel 19	1
	1	1	Channel 19	1

1: "H" level
0: "L" level

- Built-in amplifier for active low-pass filter
  In direct PLL system, active low-pass filter is more available, as lock-up-time of PLL using active low-pass filter is shorter than the one using passive low-pass filter. The LC7131, 7135, 7136 and 7137 contains an N channel open drain amplifier for active filter in order to make lockup time shorter.
- Channel Programming by BCD code.
  Scan type transciever can be composed using LC7181/7191. (LC7131/36/37)

Pin Assignment



Absolute Maximum Ratings/ T_a=25°C

					unit
Maximum Supply Voltage	$V_{DD}max$			−0.3~+8.0	V
Maximum Input Voltage	$V_{IN}max$			−0.3~V_{DD}+0.3	V
Maximum Output Voltage	$V_{OUT}(1)$	$\overline{MC}$, $\overline{LM}$, A_{OUT},	output off	−0.3~+10.0	V
	$V_{OUT}(2)$	PD_{OUT},	〃	−0.3~V_{DD}+0.3	V

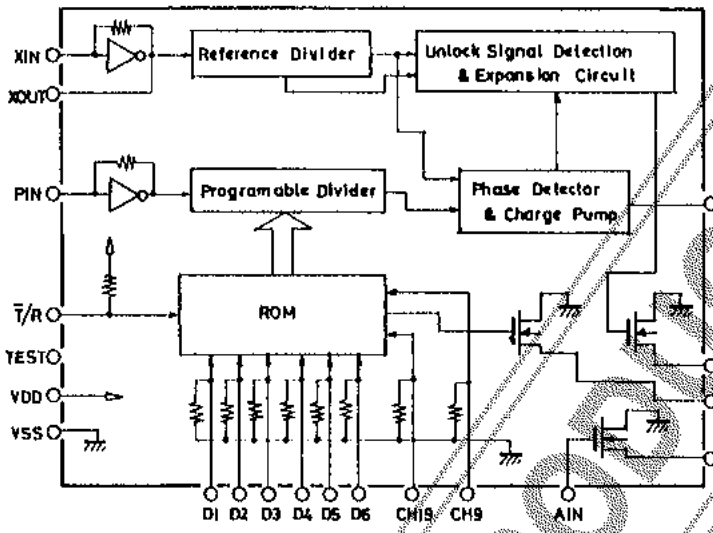
Maximum Output Current	$I_{OUT}(1)$	$\overline{MC}$, $\overline{LM}$	0～15	mA	
	$I_{OUT}(2)$	AOUT	0～2.5	mA	
Allowable Power Dissipation	Pdmax	T_a=70°C	300	mW	
Operating Temperature	Topg		−30～+70	°C	
Storage Temperature	Tstg		−40～+125	°C	

Allowable Operating Ranges/T_a=25°C			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=−30～+70 °C	5.0	6.0	7.0	V
Output Voltage	V_{OUT}	$\overline{MC}$, $\overline{LM}$, AOUT, output off	0		9.0	V
Input Amplitude	$V_{IN}(1)$	XIN, ✻, $f_{IN}(1)$=10.25MHz	1.0		0.9V_{DD}	V_{p-p}
	$V_{IN}(2)$	PIN, ✻, $f_{IN}(2)$=20MHz	1.0		0.9V_{DD}	V_{p-p}
Input Frequency	$f_{IN}(1)$	XIN, ✻, $V_{IN}(1)$=1.0V_{p-p}	1.0		10.25	MHz
	$f_{IN}(2)$	PIN, ✻, $V_{IN}(2)$=1.0V_{p-p}	1.0		20	MHz
Input "H" Level Voltage	V_{IH}	D1～D6, $\overline{T}/R$, CH9, CH19	V_{DD}−0.8			V
Input "L" Level Voltage	V_{IL}	〃 〃			0.8	V

Note*: Sinusoidal wave, capacitive coupling, T_a=−30 to +70°C

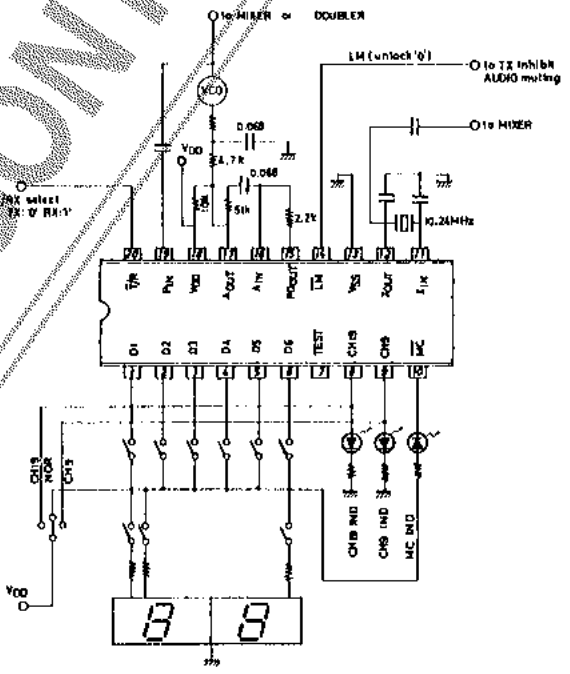
Electrical Characteristics/T_a=25°C, V_{DD}=5 to 7V.				min	typ	max	unit
Input "H" Level Current	$I_{IH}(1)$	XIN, PIN	V_{IN}=V_{DD}			8.0	μA
Input "L" Level Current	$I_{IL}(1)$	〃	V_{IN}=V_{SS}			8.0	μA
Feedback Resistance	RF	〃			3.0		MΩ
Input Threshold Voltage	Vth	〃			½V_{DD}		V
Input "H" Level Current	$I_{IH}(2)$	D1～D6, CH9, CH19	V_{IN}=V_{DD}	60	180	500	μA
Input Floating Voltage	$V_{IF}(1)$	D1～D6, CH9, CH19	Input pins open			0.2	V
Input "L" Level Current	$I_{IL}(2)$	$\overline{T}/R$	V_{IN}=V_{SS}	40	140	400	μA
Input Floating Voltage	$V_{IF}(2)$	〃	Input pin open	V_{DD}−0.2			V
Input "H" Level Current	$I_{IH}(3)$	AIN	V_{IN}=V_{DD}		0.01		nA
Input "L" Level Current	$I_{IL}(3)$	〃	V_{IN}=V_{SS}		0.01		nA
"H" Level 3-state Leak Current	I_{OFFH}	PD_{OUT}	V_{OUT}=V_{DD}		0.01		nA
"L" Level 3-state Leak Current	I_{OFFL}	〃	V_{OUT}=V_{SS}		0.01		nA
Output "H" Level Current	$V_{OH}(1)$	〃	I_{OUT}=0.3mA	V_{DD}−1.0			V
Output "L" Level Voltage	$V_{OL}(1)$	〃	〃			1.0	V
Output "H" Level Voltage	$V_{OH}(2)$	XOUT	I_{OUT}=0.5mA	V_{DD}−0.35			V
Output "L" Level Voltage	$V_{OL}(2)$	〃	〃		0.35		V
Output "L" Level Voltage	$V_{OL}(3)$	AOUT	〃			0.3	V
Output Off Leak Current	$I_{OFF}(1)$	〃	V_{OUT}=9V			3.0	μA
Output "L" Level Voltage	$V_{OL}(4)$	$\overline{MC}$, $\overline{LM}$	I_{OUT}=15mA			1.1	V
Output Off Leak Current	$I_{OFF}(2)$	〃	V_{OUT}=9V			5.0	μA
Current Dissipation	I_{DD}		$f_{IN}(1)$=10.25MHz, $f_{IN}(2)$=20MHz, $V_{IN}(1)$=$V_{IN}(2)$=1.0V_{p-p}, AIN=V_{SS}, D1=V_{DD}, Other pins open, Number of frequency		10	20	mA

Equivalent Circuit and Block Diagram



D1 to D6: Program input (BCD) D1.....LSB, D6.....MSB
X_{IN}, X_{OUT}: Amplifier for crystal oscillator
V_{DD}, V_{SS}: Power Supply
$\overline{MC}$: Miscode Indication Output
$\overline{LM}$: Lock Monitor output Lock.....open "1", unlock....."0"
PD_{OUT}: Charge pump output
A_{IN}, A_{OUT}: Amplifier for low-pass filter
P_{IN}: Programmable divider input
$\overline{T}/R$: Transmission/reception changeover input
$\overline{T}/R$="0".....Transmission $\overline{T}/R$="1"
$\overline{T}/R$="1" (or open).....reception
CH19: Channel 19 select input
CH9: Channel 9 select input
TEST: LSI test pin (TEST pin: Connected to V_{SS} or open)

■ **Application Circuit**



LC7131 Program Data and Frequency Division

Channel No.	PROGRAM CODE						RX($\overline{T}$/R='1')		TX($\overline{T}$/R='0')	
	D1	D2	D3	D4	D5	D6	N	Fvco (MHz)	N	Fvco (MHz)
1	1	0	0	0	0	0	3254	16.27	3345	16.725
2	0	1	0	0	0	0	3256	16.28	3347	16.735
3	1	1	0	0	0	0	3258	16.29	3349	16.745
4	0	0	1	0	0	0	3262	16.31	3353	16.765
5	1	0	1	0	0	0	3264	16.32	3355	16.775
6	0	1	1	0	0	0	3266	16.33	3357	16.785
7	1	1	1	0	0	0	3268	16.34	3359	16.795
8	0	0	0	1	0	0	3272	16.36	3363	16.815
9	1	0	0	1	0	0	3274	16.37	3365	16.825
10	0	0	0	0	1	0	3276	16.38	3367	16.835
11	1	0	0	0	1	0	3278	16.39	3369	16.845
12	0	1	0	0	1	0	3282	16.41	3373	16.865
13	1	1	0	0	1	0	3284	16.42	3375	16.875
14	0	0	1	0	1	0	3286	16.43	3377	16.885
15	1	0	1	0	1	0	3288	16.44	3379	16.895
16	0	1	1	0	1	0	3292	16.46	3383	16.915
17	1	1	1	0	1	0	3294	16.47	3385	16.925
18	0	0	0	1	1	0	3296	16.48	3387	16.935
19	1	0	0	1	1	0	3298	16.49	3389	16.945
20	0	0	0	0	0	1	3302	16.51	3393	16.965
21	1	0	0	0	0	1	3304	16.52	3395	16.975
22	0	1	0	0	0	1	3306	16.53	3397	16.985
23	1	1	0	0	0	1	3312	16.56	3403	17.015
24	0	0	1	0	0	1	3308	16.54	3399	16.995
25	1	0	1	0	0	1	3310	16.55	3401	17.005
26	0	1	1	0	0	1	3314	16.57	3405	17.025
27	1	1	1	0	0	1	3316	16.58	3407	17.035
28	0	0	0	1	0	1	3318	16.59	3409	17.045
29	1	0	0	1	0	1	3320	16.60	3411	17.055
30	0	0	0	0	1	1	3322	16.61	3413	17.065
31	1	0	0	0	1	1	3324	16.62	3415	17.075
32	0	1	0	0	1	1	3326	16.63	3417	.7.085
33	1	1	0	0	1	1	3328	16.64	3419	17.095
34	0	0	1	0	1	1	3330	16.65	3421	17.105
35	1	0	1	0	1	1	3332	16.66	3423	17.115
36	0	1	1	0	1	1	3334	16.67	3425	17.125
37	1	1	1	0	1	1	3336	16.68	3427	17.135
38	0	0	0	1	1	1	3338	16.69	3429	17.145
39	1	0	0	1	1	1	3340	16.70	3431	17.155
40	0	0	0	0	0	0	3342	16.71	3433	17.165

LC7135 Program Data and Frequency Division

1	1	0	0	0	0	0	3254	16.27	3345	16.725
2	0	1	0	0	0	0	3256	16.28	3347	16.735
3	1	1	0	0	0	0	3258	16.29	3349	16.745
4	0	0	1	0	0	0	3262	16.31	3353	16.765
5	1	0	1	0	0	0	3264	16.32	3355	16.775
6	0	1	1	0	0	0	3266	16.33	3357	16.785
7	1	1	1	0	0	0	3268	16.34	3359	16.795
8	0	0	0	1	0	0	3272	16.36	3363	16.815
9	1	0	0	1	0	0	3274	16.37	3365	16.825
10	0	0	0	0	1	0	3276	16.38	3367	16.835
11	1	0	0	0	1	0	3278	16.39	3369	16.845
12	0	1	0	0	1	0	3282	16.41	3373	16.865
13	1	1	0	0	1	0	3284	16.42	3375	16.875
14	0	0	1	0	1	0	3286	16.43	3377	16.885
15	1	0	1	0	1	0	3288	16.44	3379	16.895
16	0	1	1	0	1	0	3292	16.46	3383	16.915
17	1	1	1	0	1	0	3294	16.47	3385	16.925
18	0	0	0	1	1	0	3296	16.48	3387	16.935
19	1	0	0	1	1	0	3298	16.49	3389	16.945
20	0	0	0	0	0	1	3302	16.51	3393	16.965
21	1	0	0	0	0	1	3304	16.52	3395	16.975
22	0	1	0	0	0	1	3306	16.53	3397	16.985

'1': logical high level
'0': logical low level

LC7136/37 Program Data and Frequency Division

Channel No.	PROGRAM CODE D1	D2	D3	D4	D5	D6	RX(T/R="1") N	TX(T/R="0") N
1	1	0	0	0	0	0	3381	2760
2	0	1	0	0	0	0	3383	2761
3	1	1	0	0	0	0	3385	2762
4	0	0	1	0	0	0	3387	2763
5	1	0	1	0	0	0	3389	2764
6	0	1	1	0	0	0	3391	2765
7	1	1	1	0	0	0	3393	2766
8	0	0	0	1	0	0	3395	2767
9	1	0	0	1	0	0	3397	2768
10	0	0	0	0	1	0	3399	2769
11	1	0	0	0	1	0	3401	2770
12	0	1	0	0	1	0	3403	2771
13	1	1	0	0	1	0	3405	2772
14	0	0	1	0	1	0	3407	2773
15	1	0	1	0	1	0	3409	2774
16	0	1	1	0	1	0	3411	2775
17	1	1	1	0	1	0	3413	2776
18	0	0	0	1	1	0	3415	2777
19	1	0	0	1	1	0	3417	2778
20	0	0	0	0	0	1	3419	2779
21	1	0	0	0	0	1	3421	2780
22	0	1	0	0	0	1	3423	2781
23	1	1	0	0	0	1	3425	2782
24	0	0	1	0	0	1	3427	2783
25	1	0	1	0	0	1	3429	2784
26	0	1	1	0	0	1	3431	2785
27	1	1	1	0	0	1	3433	2786
28	0	0	0	1	0	1	3435	2787
29	1	0	0	1	0	1	3437	2788
30	0	0	0	0	1	1	3439	2789
31	1	0	0	0	1	1	3441	2790
32	0	1	0	0	1	1	3443	2791
33	1	1	0	0	1	1	3445	2792
34	0	0	1	0	1	1	3447	2793
35	1	0	1	0	1	1	3449	2794
36	0	1	1	0	1	1	3451	2795
37	1	1	1	0	1	1	3453	2796
38	0	0	0	1	1	1	3455	2797
39	1	0	0	1	1	1	3457	2798
40	0	0	0	0	0	0	3459	2799

"1" : logical high level
"0" : logical low level