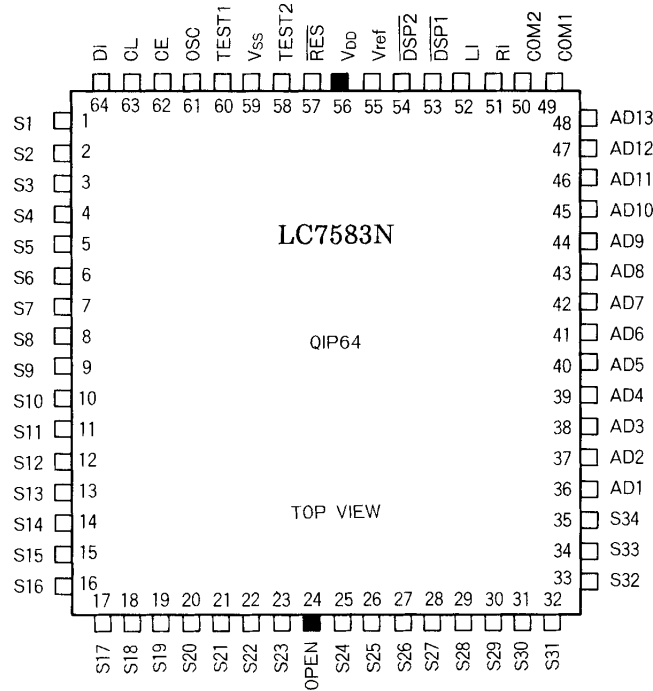




# LC7583N

## Pin Assignment



## Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ ,  $V_{SS}=0\text{V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$V_{DD}$	-0.3 to +7.0	V
Input voltage	$V_{IN1}$	CE, CL, DI, RES, DSP1, DSP2	-0.3 to +7.0	V
	$V_{IN2}$	RI, LI	$V_{DD}+0.3$	V
	$V_{IN3}$	Vref	-0.3 to $V_{DD}+0.3$	V
	$V_{IN4}$	OSC output OFF	-0.3 to $V_{DD}+0.3$	V
Output voltage	$V_{OUT}$	OSC output OFF	-0.3 to $V_{DD}+0.3$	V
Output current	$I_{OUT1}$	S1 to S34, AD1 to AD13	500	$\mu\text{A}$
	$I_{OUT2}$	COM1, 2	1	mA
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 85^\circ\text{C}$	100	mW
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-45 to +125	$^\circ\text{C}$

**Allowable Operating Conditions** at  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{SS}=0\text{V}$

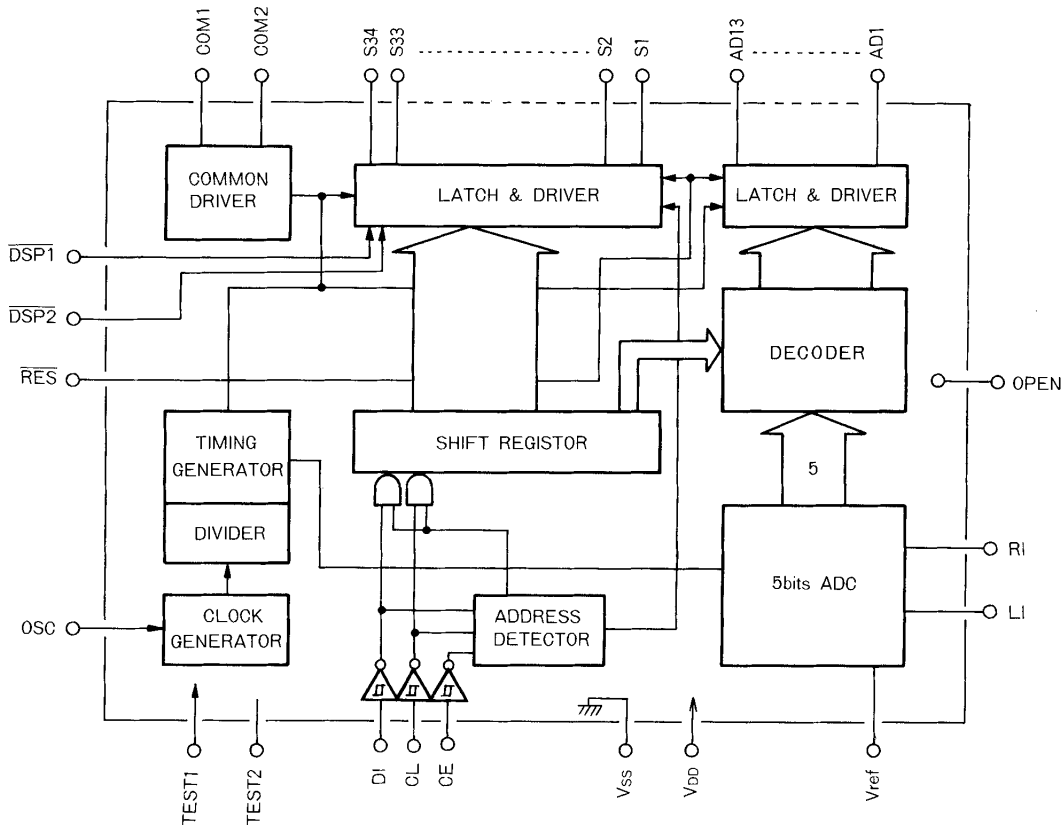
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		4.5		6.5	V
Reference voltage	Vref	$V_{ref} \leq V_{DD}$	4.5		$V_{DD}$	V
Input high-level voltage	$V_{IH1}$	CE, CL, DI, RES, DSP1, DSP2	$0.7V_{DD}$		6.5	V
Input low-level voltage	$V_{IL1}$	CE, CL, DI, RES, DSP1, DSP2	0		$0.3V_{DD}$	V
Input hysteresis width	$V_H$	CE, CL, DI	$0.05V_{DD}$	$0.10V_{DD}$		V
Recommended external resistance	R	OSC		47		$\text{k}\Omega$
Recommended external capacitance	C	OSC		1000		pF
OSC guaranteed range	$f_{OSC}$	OSC	10	32	50	kHz
Low-level clock pulse width	$t_{\phi L}$	CL, DI	0.5			$\mu\text{s}$
High-level clock pulse width	$t_{\phi H}$	CL, DI	0.5			$\mu\text{s}$
Setup time	$t_{sup}$	CL, DI	0.5			$\mu\text{s}$
Serial data pulse width	$t_1$	CL, CE see fig. A.	2			$\mu\text{s}$
	$t_2$	See fig. A.			3	$\mu\text{s}$
Data hold time	$t_{dh}$	CL, DI	0.5			$\mu\text{s}$
AD conversion time	$t_{CONV}$	RI, LI, per channel	200			$\mu\text{s}$
Input voltage	$V_{IN}$	RI, LI/ $V_{IN} \leq V_{ref}$	0		$V_{DD}$	V

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## Electrical Characteristics at Ta = 25°C, under Allowable Operating Conditions


Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH1}$	CE, CL, DI, RI, LI, $\overline{RES}$ , $\overline{DSP1}$ , $\overline{DSP2}$ , $V_I=6.5V$			5	$\mu A$
Input low-level current	$I_{IL1}$	CE, CL, DI, RI, LI, $\overline{RES}$ , $\overline{DSP1}$ , $\overline{DSP2}$ , $V_I=0V$			5	$\mu A$
Output high-level voltage	$V_{OH1}$	S1 to S34, $I_O=-10\mu A$	$V_{DD}-1.0$			V
Output low-level voltage	$V_{OL1}$	AD1 to AD13, $I_O=10\mu A$			1.0	V
Output high-level voltage	$V_{OH2}$	COM1, COM2, $I_O=-100\mu A$	$V_{DD}-0.6$			V
Output low-level voltage	$V_{OL2}$	COM1, COM2, $I_O=100\mu A$			0.6	V
M-level voltage	$V_{MID}$	COM1, COM2, $V_{DD}=6.5V$ , $I_O=\pm 100\mu A$	2.65	3.25	3.85	V
M-level voltage	$V_{MID}$	COM1, COM2, $V_{DD}=3.0V$ , $I_O=\pm 100\mu A$	0.9	1.5	2.1	V
OSC frequency	$f_{OSC}$	OSC, R=47k $\Omega$ , C=1000pF		32		kHz
AD conversion linearity error	Err	$V_{ref}=4.5$ to $6.5V \leq V_{DD}$	-1/2		+1/2	LSB
Supply current	$I_{DD}$	$f_{OSC}=32kHz$ , input= $V_{OD}$ , output=open		2	4	mA
Reference supply current	$I_{ref}$	$V_{ref}$		0.3	1	mA

## Block Diagram

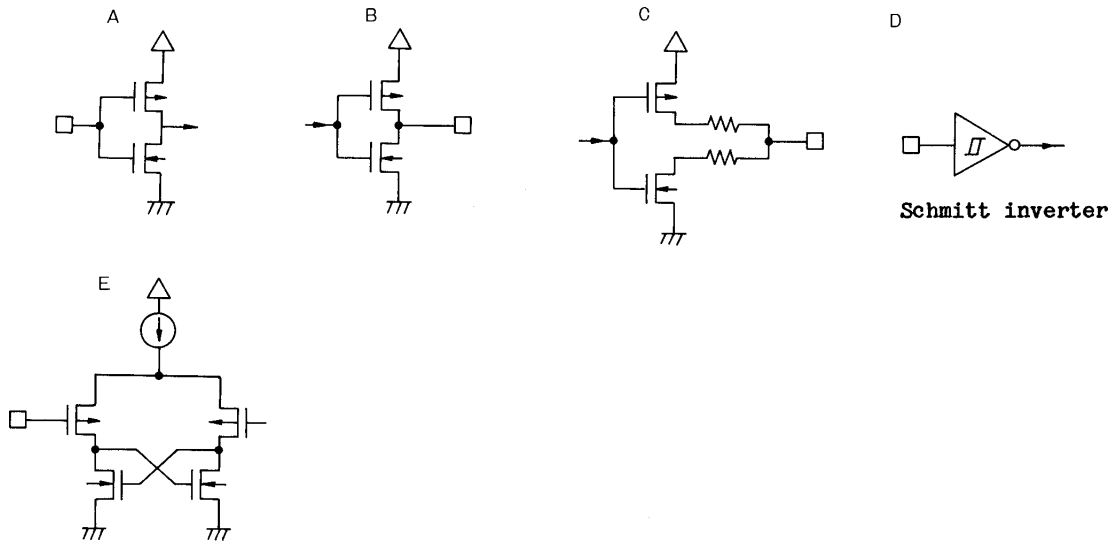


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## Pin Function

Pin Name	Pin No.	Description	Active	I/O	I/O Configuration
S1 to S33	1 to 34	Segment output pins used to display the data transferred from the serial data input pin.	-	O	B
S34	35	Segment output pin used to display the external input (DSP1, DSP2) data	-	O	
AD1 to AD13	36 to 48	Segment output pins used to display the ADC input (R1, L1) data. Control bits "A1", "A2" are used to provide 3 types of pattern. AD1 : Lowest lighting level, AD13 : Highest lighting level	-	O	
COM1 COM2	49 50	Common driver output pins. Frame frequency : $f_{OSC}/512\text{Hz}$	-	O	C
RI LI	51 52	AD converter input pins.	Analog	I	E
DSP1 DSP2	53 54	Direct (external input) display pins whose segment output is delivered at S34.	L	I	A
Vref	55	Pin used to supply the AD converter reference voltage.	-	-	-
V <sub>DD</sub> V <sub>SS</sub>	56 59	Power supply pin.	-	-	-
RES	57	Pin used to force the display to be unlighted at the initial mode.	L	I	A
TEST2	58	Open	-	O	-
TEST1	60	Open or connected to V <sub>SS</sub> .	-	I	A
CE	62	Serial data transfer pin. Connected to a controller (microcomputer). CE : Chip enable CL : Sync clock DI : Transfer data	H	I	D
CL	63				
DI	64		-		
OPEN	24	No connection.	-	-	-

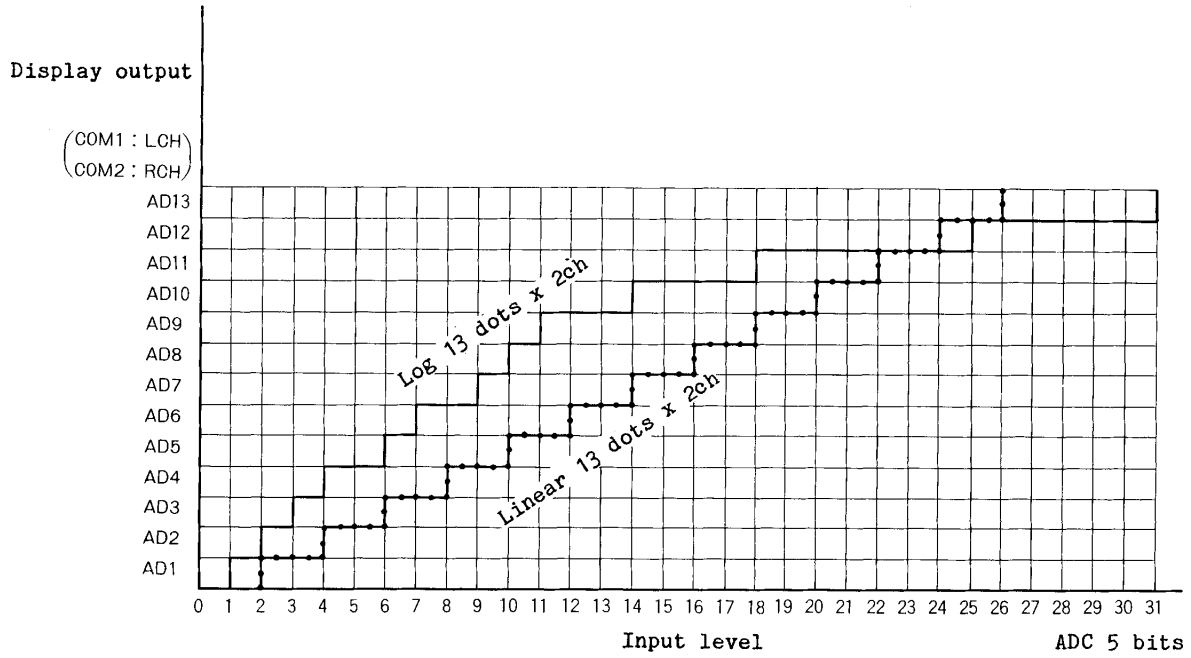
## Equivalent Input/Output Configuration



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## ADC Display Mode

2ch (stereo) Display (shown for one channel only)

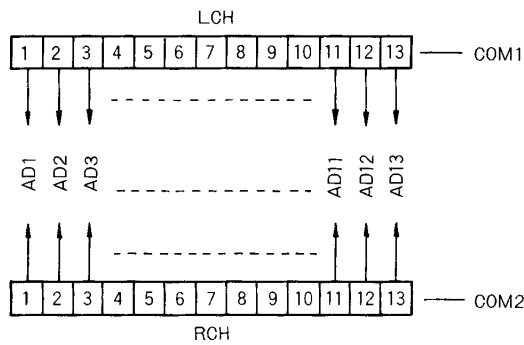


## Lighting Level for Log Display

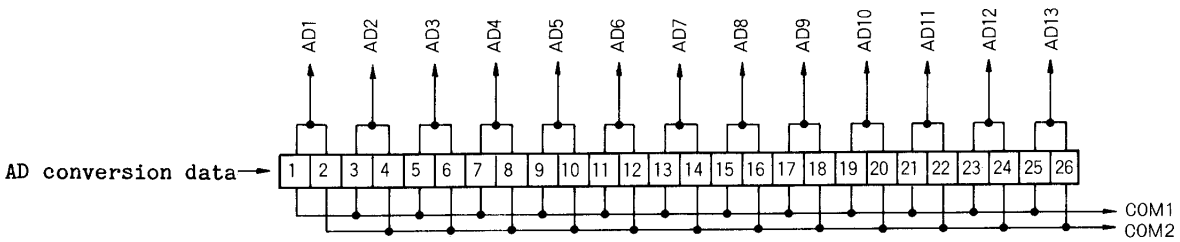
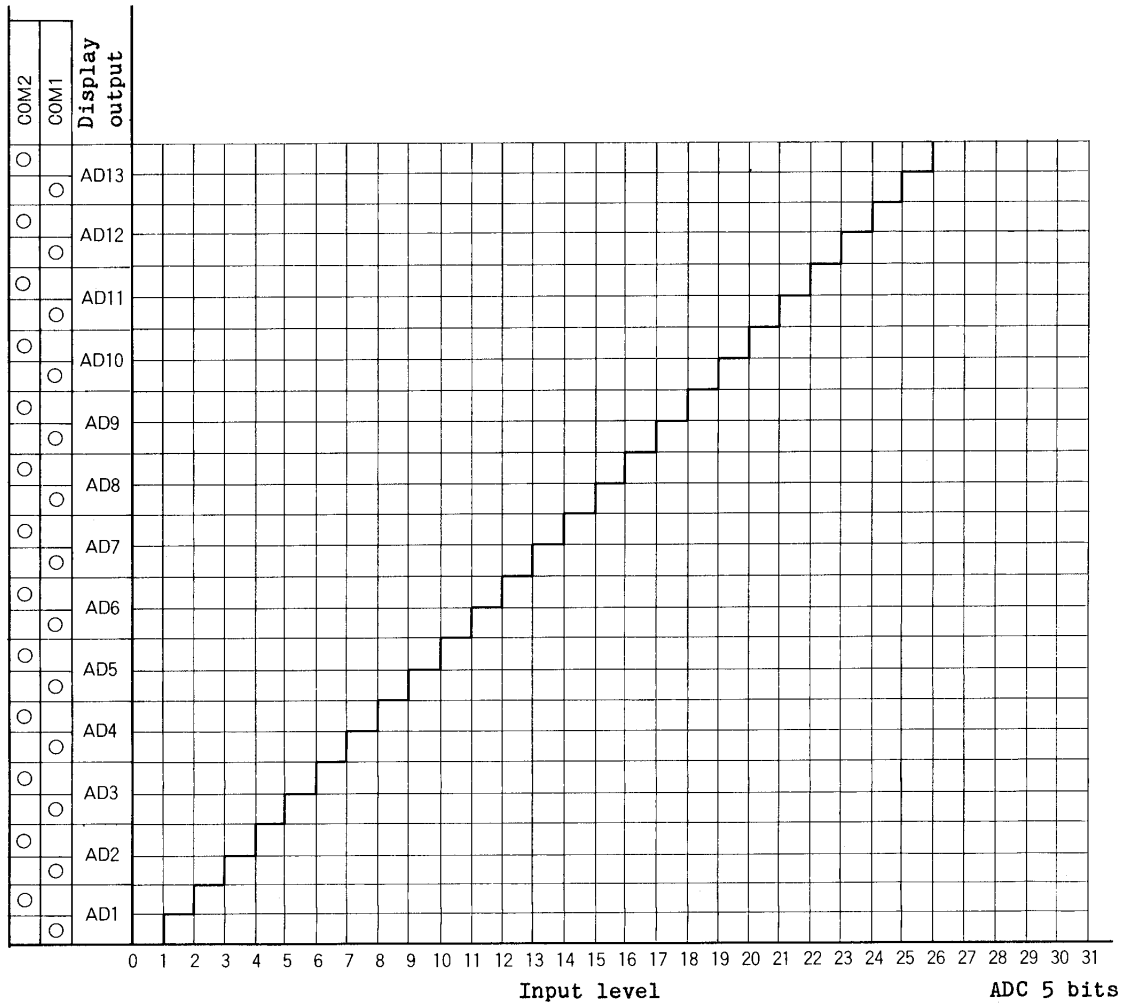
Display Output	dB Display (dB)	Display Output	dB Display (dB)
AD1	-20.0	AD8	0.0
AD2	-14.0	AD9	1.0
AD3	-10.5	AD10	3.0
AD4	-8.0	AD11	5.0
AD5	-4.5	AD12	8.0
AD6	-3.0	AD13	10.0
AD7	-1.0		

Note) The conversion error of the AD converter is  $\pm 1/2\text{LSB}$ .  
When 0dB is taken as 1V (at  $V_{\text{ref}}=4.95\text{V}$ ), a conversion error of approximately  $\pm 3.5\text{dB}$  occurs at -20dB.

## COMMON Connection



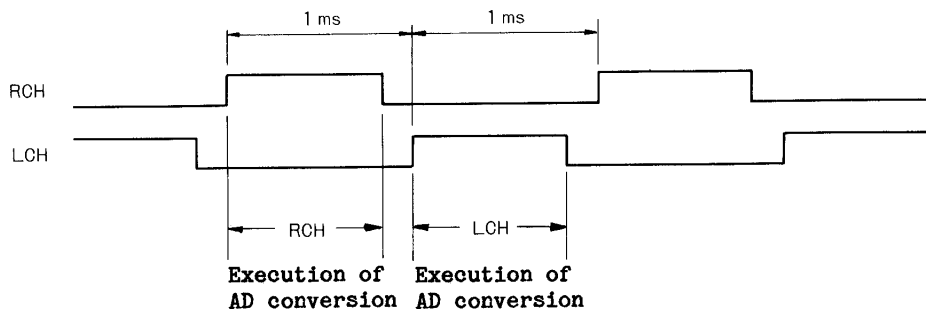
1ch (monaural) Display



Connect the RI pin and LI pin at the monaural mode.

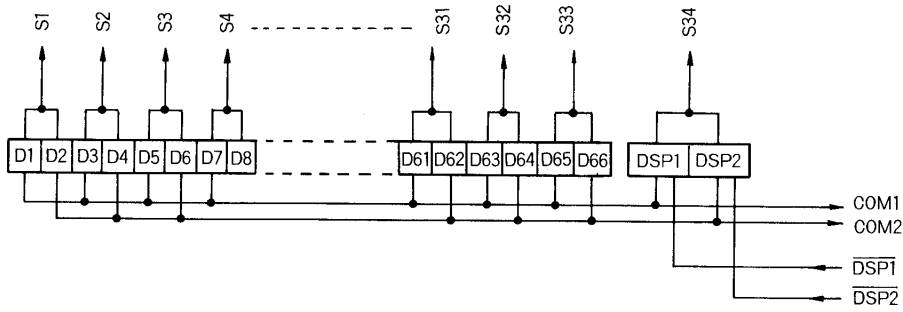
ADC Conversion Time

When the oscillation frequency is 32kHz, individual input signals at the RI pin, LI pin are sampling-processed alternately once every 1ms.



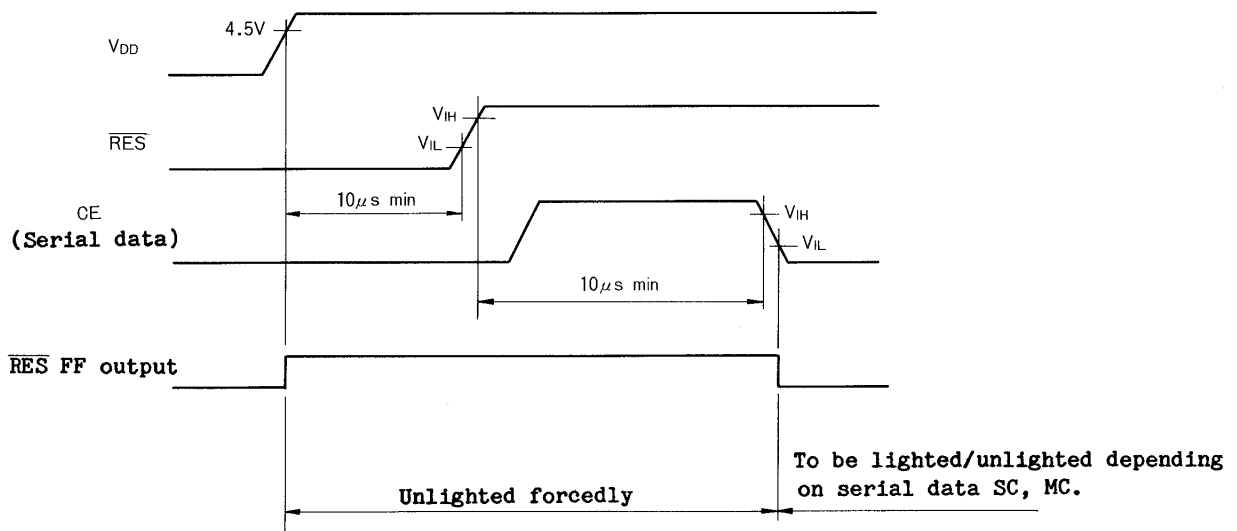
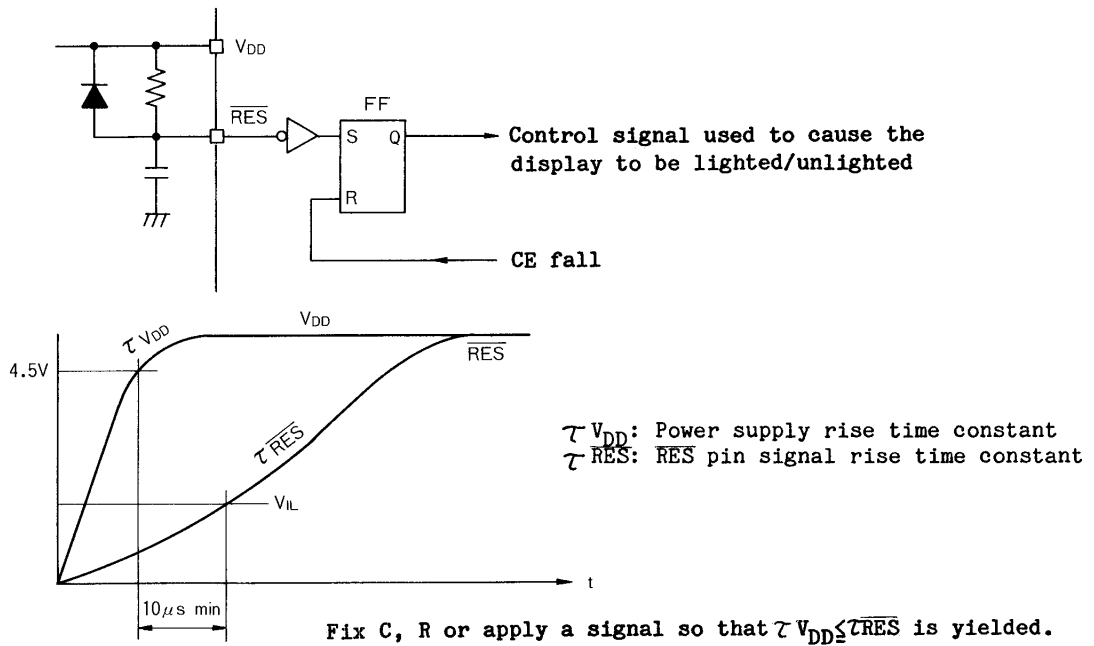
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## Connection of Serial Data, DSP Input Data



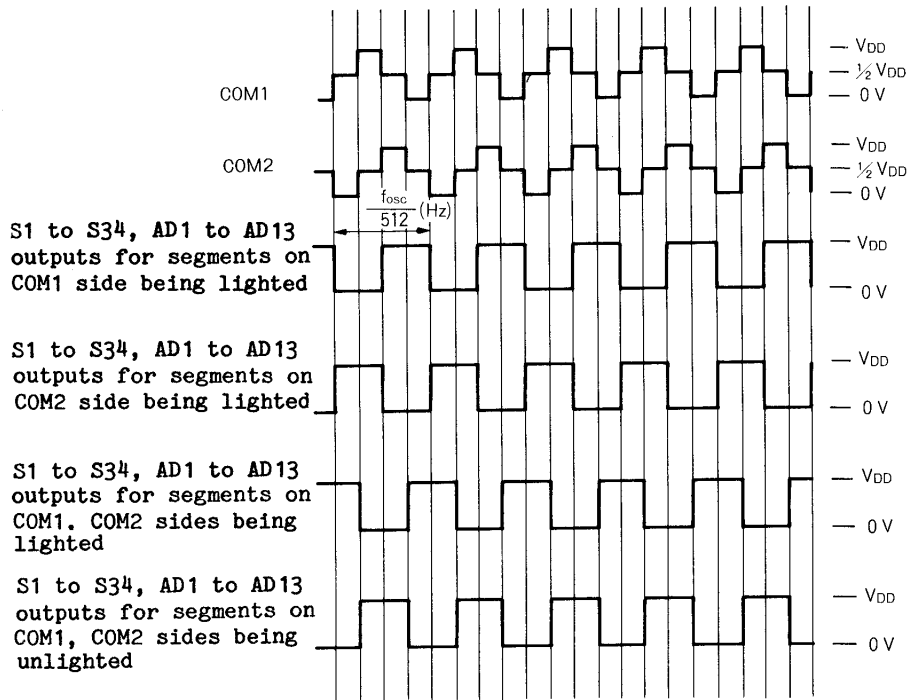
## RES Pin and Display Control

The internal circuit of the RES pin is shown below.

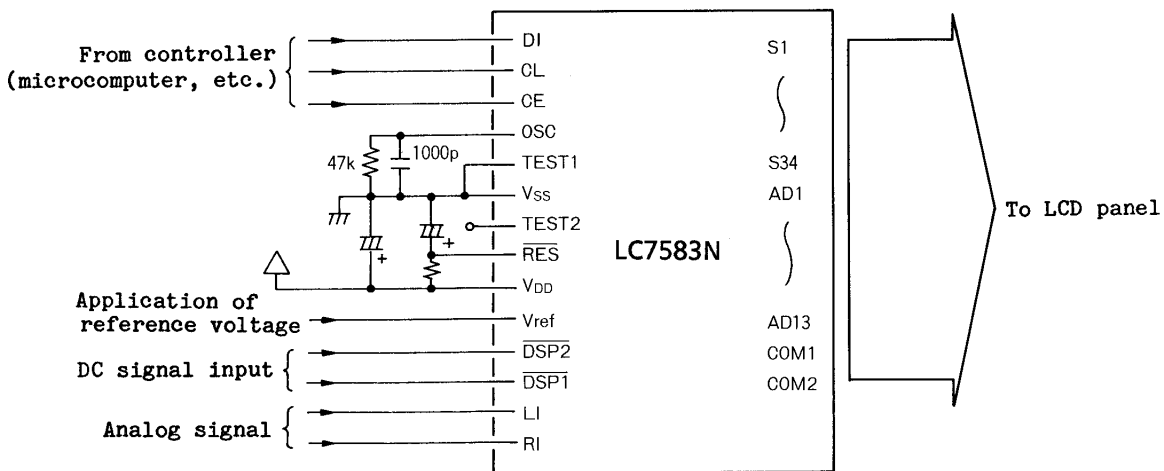


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## Output Waveforms (S1 to S34, AD1 to AD13)



## Sample Application Circuit



Unit (resistance:  $\Omega$ , capacitance: F)

[Fig. A] : Data Transfer Mode (Transferred from a controller as shown below)

