MOS IC



LC89970, 89970M

PAL CCD Delay Line

Overview

The LC89970 and LC89970M are CCD delay lines for PAL television systems. It incorporates a comb filter for chrominance signal and a 1 H delay line for luminance signal.

Structure

• NMOS + CCD

Functions

- Two CCD shift registers (for chrominance and luminance signals)
- CCD drive circuits
- CCD stage count switching circuit
- CCD signal adder
- Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- Sample-and-hold circuit
- PLL $3 \times$ frequency multiplier
- fsc clock output circuit
- RD voltage generator

Features

- 5 V single-voltage power supply
- Built-in PLL 3 × frequency multiplier circuit allows 3 fsc operation from an fsc (4.43 MHz) input.
- Control pin switchable to handle PAL/GBI and 4.43 MHz NTSC systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max		-0.3 to +6.0	V
Allowable power dissipation	Pd max	LC89970	1200	mW
	Pumax	LC89970M	600	mW
Operating temperature	Topr		-10 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

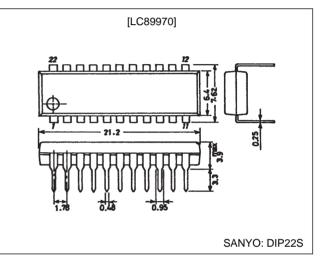
SANYO Electric Co., Ltd. Semiconductor Bussiness Headquarters TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

63095 TH (OT) No. 5111-1/9

Package Dimensions

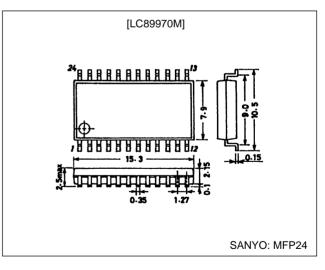
unit: mm

3059-DIP22S (375 mil)



unit: mm

3045B-MFP24



Allowable Operating Ranges at $Ta=25^{\circ}C$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V _{DD}		4.75	5.00	5.25	V
Clock input amplitude	V _{CLK}		300	500	1000	mVp-p
Clock frequency	F _{CLK}	Sine wave	_	4.43361875	_	MHz
Clock signal input amplitude	V _{IN-C}		_	350	500	mVp-p
Luminance signal input amplitude	V _{IN-Y}		_	400	572	mVp-p

Electrical Characteristics at V_{DD} = 5.0 V, Ta = 25°C, F_{CLK} = 4.43361875 MHz, V_{CLK} = 500 mVp-p

Parameter	Symbol	5	Switch state	s	Conditions	min	typ	max	Unit
	Symbol	SW1	SW2	SW3	Conditions				
Supply current	I _{DD-1}	а	а	b	1	40	50	60	mA
Supply current	I _{DD-2}	b	а	b	I	40	50	00	IIIA
Chrominance System Characteri	stics (with no Y	IN input)			-				
Pin voltage (input)	V _{INC-1}	а	а	b		2.0	2.4	2.8	v
T in voltage (input)	V _{INC-2}	b	а	b	2	2.0	2.4	2.0	v
Pin voltage (output)	V _{OUYC-1}	а	а	b	2	1.2	1.6	2.0	v
T in voltage (output)	V _{OUTC-2}	b	а	b		1.2	1.0	2.0	v
Voltage gain	G _{VC-1}	а	а	b	3	-2	0	+2	dB
	G _{VC-2}	b	а	b	3	-2			
Comb depth	C _{D-1}	а	а	b	4	_	-40	-35	dB
	C _{D-2}	b	а	b					
Linearity	L _{NC-1}	а	а	b	5	-0.3	0.0	+0.3	dB
Lincarty	L _{NC-2}	b	а	b					
Clock leakage (3 fsc)	L _{CK3C-1}	а	а	b		_	10	50	mVrms
Clock leakage (3 13c)	L _{CK3C-2}	b	а	b	6				
Clock leakage (fsc)	L _{CK1C-1}	а	а	b			0.8	1.5	mVrms
Clock leakage (13c)	L _{CK1C-2}	b	а	b					
Noise	N _{C-1}	а	а	b	7	_	0.5	2.0	mVrms
Noise	N _{C-2}	b	а	b	1			2.0	mvims
Output impedance	Z _{OC-1}	а	а	a, b	8	200	350	500	Ω
	Z _{OC-2}	b	а	a, b	0			500	52
0 H delay time	T _{DC-1}	а	а	b	9	_	245		ns
	T _{DC-2}	b	а	b					115

Continued from preceding page.

Parameter	Cumb al	5	Switch state	S	Conditions	min	typ	max	Unit
	Symbol	SW1	SW2	SW3	Conditions				
Luminance System Characteris	tics (with no C-IN	1 or C-IN2	input)						
Din voltogo (innut)	V _{INY-1}	а	а	b		1.7	2.1	2.5	V
Pin voltage (input)	V _{INY-2}	b	а	b	10	1.7	2.1	2.5	
Pin voltage (output)	V _{OUTY-1}	а	а	b	10	0.8	1.2	1.6	V
Fill Voltage (Output)	V _{OUTY-2}	b	а	b		0.0	1.2	1.0	v
Voltage gain	G _{VY-1}	а	а	b	11	-2	0	+2	dB
voltage gain	G _{VY-2}	b	а	b		-2	0	τz	uБ
Frequency responce	G _{FY-1}	а	b	b	12	-2	0	+2	dB
	G _{FY-2}	b	b	b	12	-2			
Differential gain	D _{GY-1}	а	а	b	13	0	5	7	%
	D _{GY-2}	b	а	b					70
Differential phase	D _{PY-1}	а	а	b		0	5	7	deg
Differential priase	D _{PY-2}	b	а	b		Ŭ	5	· ·	
Linearity	L _{SY-1}	а	а	b	- 14	37	40	43	%
Lineanty	L _{SY-2}	b	а	b					
Clock leakage (3 fsc)	L _{CK3Y-1}	а	а	b		_	10	50	mVrms
Clock leakage (5 130)	L _{CK3Y-2}	b	а	b	15				
Clock leakage (fsc)	L _{CK1Y-1}	а	а	b	15	_	0.8	1.5	mVrms
Clock leakage (ISC)	L _{CK1Y-2}	b	а	b					
Noise	N _{Y-1}	а	а	b	16		0.5	2.0	mVrms
NOISE	N _{Y-2}	b	а	b	10		0.5	2.0	mvrms
Output impedance	Z _{OY-1}	а	а	c, b	17	250	400	550	Ω
	Z _{OY-2}	b	а	c, b		250	400	550	52
Delay time	T _{DY-1}	а	а	b	18	—	63.92	—	116
	T _{DY-2}	b	а	b	10	—	63.47	—	μs

Test Conditions

- 1. Supply current with no signal input.
- 2. C-OUT voltage (center bias voltage) with no signal input.
- 3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

$$GVC = 20 \log \frac{C\text{-}OUT \text{ output } [mVp\text{-}p]}{350 \ [mVp\text{-}p]} \ [dB]$$

Test frequencies

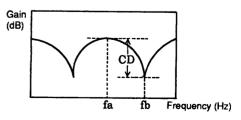
GVC-1	4.429662 MHz (PAL/GBI)
GVC-2	4.425694 MHz (4.43 NTSC)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.

 $CD = 20 \log \frac{C\text{-}OUT \text{ output with fb input } [mVp-p]}{C\text{-}OUT \text{ output with fa input } [mVp-p]} \text{ [dB]}$

Test frequencies

	fa	fb
CD-1	4.429662 MHz	4.425756 MHz (PAL/GBI)
CD-2	4.425694 MHz	4.417819 MHz (4.43 NTSC)



5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

 $LNC = 20 \log \left(\frac{Output \text{ for a } 500 \text{ mVp-p input } [mVp-p]}{500 \text{ [mVp-p]}} / \frac{Output \text{ for a } 200 \text{ mVp-p input } [mVp-p]}{200 \text{ [mVp-p]}} \right) \text{ [dB]}$

Test frequencies

LNC-1 4.429662 MHz (PAL/GBI) LNC-2 4.425694 MHz (4.43 NTSC)

- 6. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input.
- Measure the noise in the C-OUT output with no input. Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.
- 8. Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$ZOC = \frac{V2 [mVp-p] - V1 [mVp-p]}{V1 [mVp-p]} \times 500 [\Omega]$$

Test frequencies

ZOC-1 4.429662 MHz (PAL/GBI) ZOC-2 4.425694 MHz (4.43 NTSC)

- 9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)
- 10. Y-OUT voltage (clamp voltage) with no signal input.
- 11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

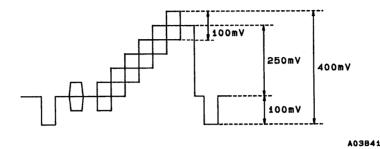
 $GVY = 20 \log \frac{Y-OUT \text{ output } [mVp-p]}{400 \ [mVp-p]} \ [dB]$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

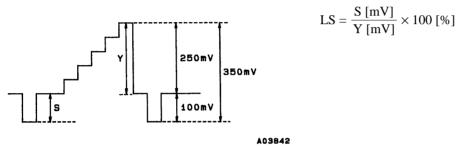
 $GFY = 20 \log \frac{\text{Y-OUT output with a 3.3 MHz input [mVp-p]}}{\text{Y-OUT output with a 200 kHz input [mVp-p]}} \text{ [dB]}$

Note that V_{bias} should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



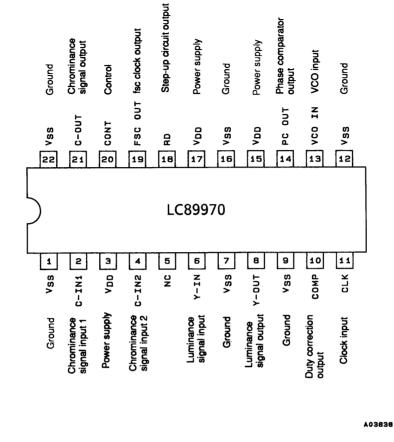
14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



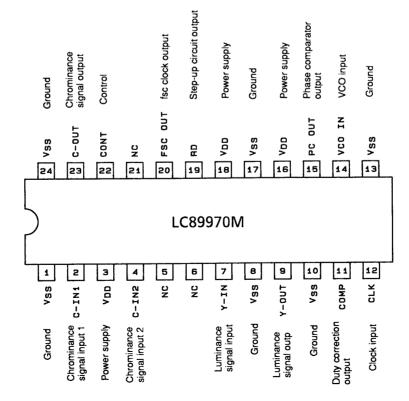
- 15. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input.
- 16. Measure the noise in the Y-OUT output with no input. Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 5 MHz low-pass filter, and a 4.43 MHz trap filter.
- 17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW3 set to c, and let V2 be the C-OUT output with SW3 set to b.

$$ZOY = \frac{V2 [mVp-p] - V1 [mVp-p]}{V1 [mVp-p]} \times 500 [\Omega]$$

18. The Y-OUT delay time with respect to Y-IN



Pin Assignment [LC89970M]



A03858

Top view

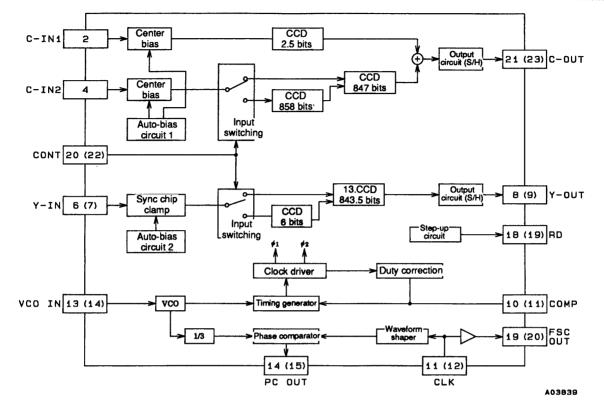
Top view

LC89970, 89970M

Pin Assignment [LC89970]

Block Diagram

Note * Pin numbers in parentheses are for the LC89970M.



Control Pin Function

CONT	Mode (representative example)	Chrominance signal delay (CCD bits)	Luminance signal delay (CCD bits)
Low	PAL/GBI	2 H (1705) + 0 H (2.5)	1 H (849.5)
High	4.43 NTSC	1 H (847) + 0 H (2.5)	1 H (843.5)

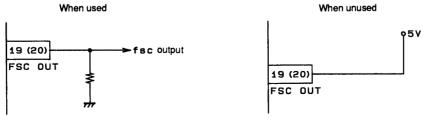
Switching Voltage Levels

Low/high	Symbol	min	typ	max	Unit
Low	VL	-0.3	0.0	0.5	V
High	V _H	2.0	5.0	6.0	V

Note: Since the control pin has a built-in pull-down resistor, the pin will be set to the low state if left open.

FSC OUT Pin Function

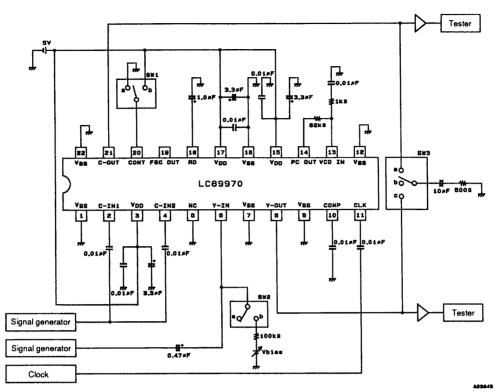
This pin provides a buffer output for the clock signal input to the CLK pin.



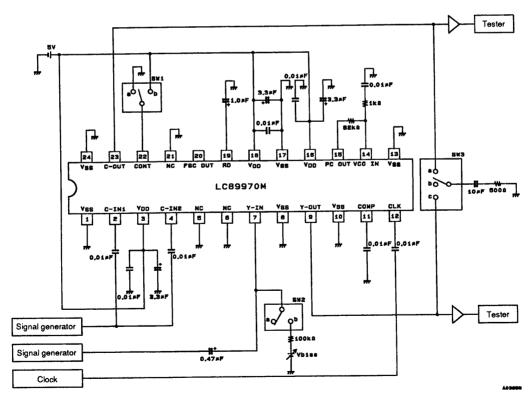
A03840

Note: Since this pin has a built-in pull-up resistor, the pin voltage will go to the supply voltage and output will cease if left open.

Test Circuit [LC89970]



Test Circuit [LC89970M]



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