LM148/LM248/LM348 Quad 741 Op Amps

Check for Samples: LM148-N, LM248-N, LM348-N

FEATURES

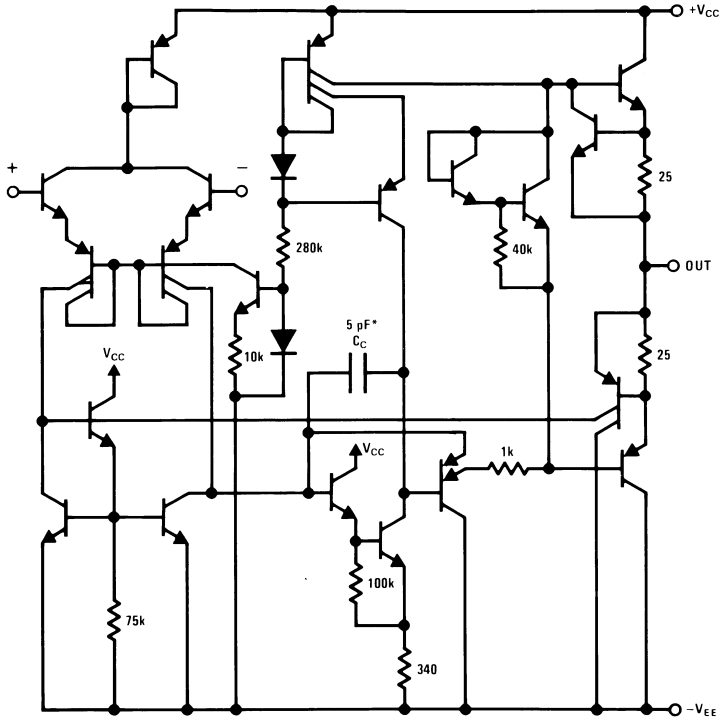
- **741 Op Amp Operating Characteristics**
- **Class AB Output Stage—No Crossover Distortion**
- **Pin Compatible With the LM124**
- **Overload Protection for Inputs and Outputs**
- **Low Supply Current Drain: 0.6 mA/Amplifier**
- **Low Input Offset Voltage: 1 mV**
- **Low Input Offset Current: 4 nA**
- **Low Input Bias Current 30 nA**
- **High Degree of Isolation Between Amplifiers: 120 dB**
- **Gain Bandwidth Product**
  - **LM148 (Unity Gain): 1.0 MHz**

DESCRIPTION

The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required. For lower power refer to LF444.

Schematic Diagram



* 1 pF in the LM149

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

		LM148	LM248	LM348
Supply Voltage		±22V	±18V	±18V
Differential Input Voltage		±44V	±36V	±36V
Output Short Circuit Duration(3)		Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA})(4)				
PDIP (NFF) P_d		—	—	750 mW
θ_{JA}		—	—	100°C/W
CDIP (J) P_d		1100 mW	800 mW	700 mW
θ_{JA}		110°C/W	110°C/W	110°C/W
Maximum Junction Temperature (T_{jMAX})		150°C	110°C	100°C
Operating Temperature Range		$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$
Storage Temperature Range		−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.) Ceramic		300°C	300°C	300°C
Lead Temperature (Soldering, 10 sec.) Plastic				260°C
Soldering Information				
Dual-In-Line Package	Soldering (10 seconds)	260°C	260°C	260°C
Small Outline Package	Vapor Phase (60 seconds)	215°C	215°C	215°C
	Infrared (15 seconds)	220°C	220°C	220°C
ESD tolerance(5)		500V	500V	500V

(1) Refer to RETS 148X for LM148 military specifications.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(4) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the 25°C P_{DMAX}, whichever is less.
(5) Human body model, 1.5 kΩ in series with 100 pF.

Electrical Characteristics

These specifications apply for V_S = ±15V and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise noted.

Parameter	Conditions	LM148			LM248			LM348			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, $R_S \le 10$ kΩ		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	T_A = 25°C		4	25		4	50		4	50	nA
Input Bias Current	T_A = 25°C		30	100		30	200		30	200	nA
Input Resistance	T_A = 25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	T_A = 25°C, V_S = ±15V		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \ge 2$ kΩ	50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		−120			−120			−120		dB
Small Signal Bandwidth	T_A = 25°C, LM148 Series		1.0			1.0			1.0		MHz
Phase Margin	T_A = 25°C, LM148 Series (A_V = 1)		60			60			60		degrees

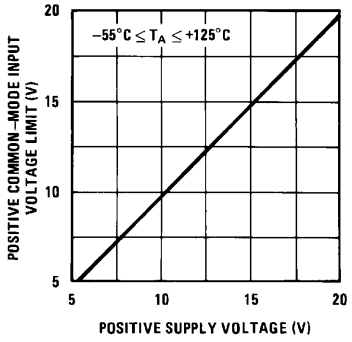
Electrical Characteristics (continued)

These specifications apply for V_S = ±15V and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise noted.

Parameter	Conditions	LM148			LM248			LM348			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	T_A = 25°C, LM148 Series (A_V = 1)		0.5			0.5			0.5		V/µs
Output Short Circuit Current	T_A = 25°C		25			25			25		mA
Input Offset Voltage	$R_S \le 10$ kΩ			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L > 2$ kΩ	25			15			15			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		±12	±13		±12	±13		V
	R_L = 2 kΩ	±10	±12		±10	±12		±10	±12		V
Input Voltage Range	V_S = ±15V	±12			±12			±12			V
Common-Mode Rejection Ratio	$R_S \le 10$ kΩ	70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \le 10$ kΩ, ±5V ≤ V_S ≤ ±15V	77	96		77	96		77	96		dB

CROSS TALK TEST CIRCUIT

V_S = ±15V



Typical Performance Characteristics

Supply Current

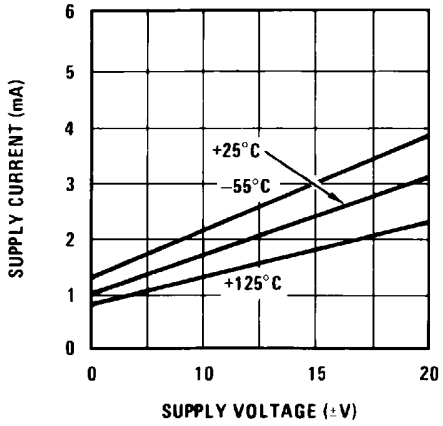


Figure 1.

Input Bias Current

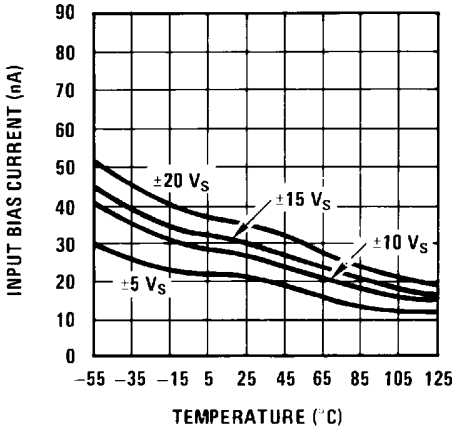


Figure 2.

Voltage Swing

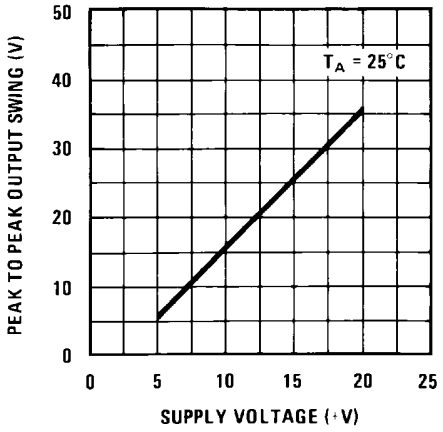


Figure 3.

Positive Current Limit

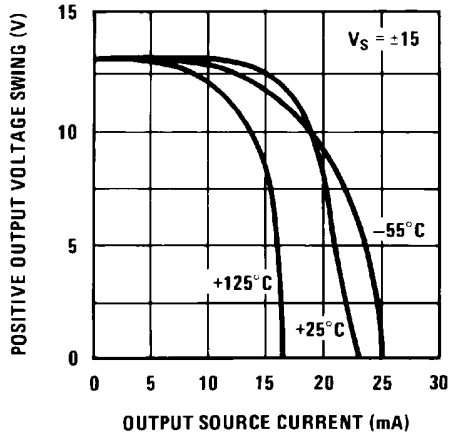


Figure 4.

Negative Current Limit

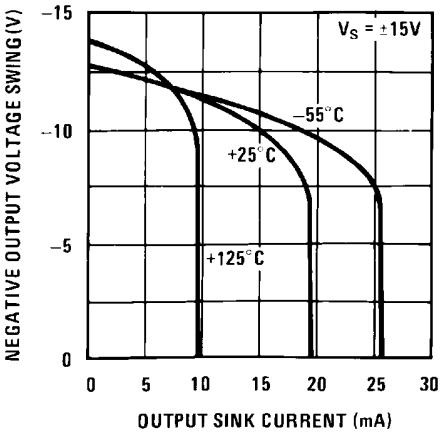


Figure 5.

Output Impedance

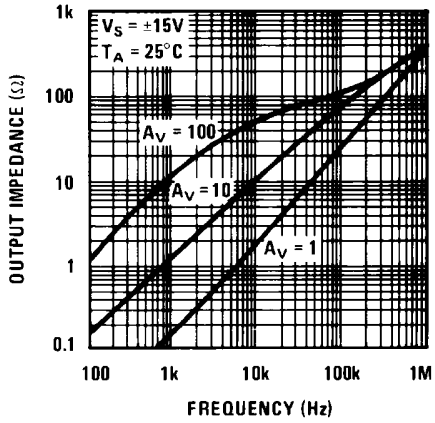


Figure 6.

Typical Performance Characteristics (continued)

Common-Mode Rejection Ratio

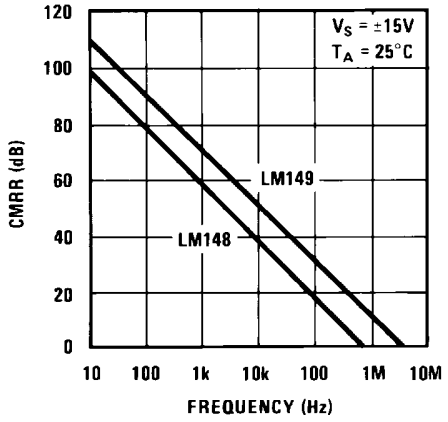


Figure 7.

Open Loop Frequency Response

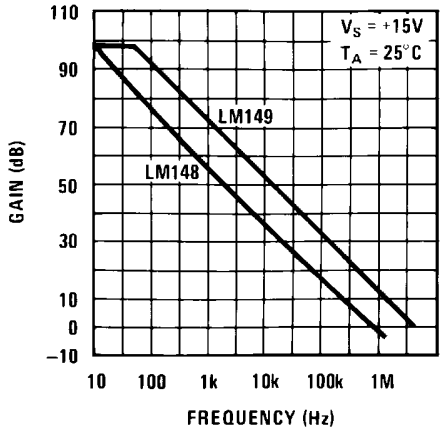


Figure 8.

Bode Plot LM148

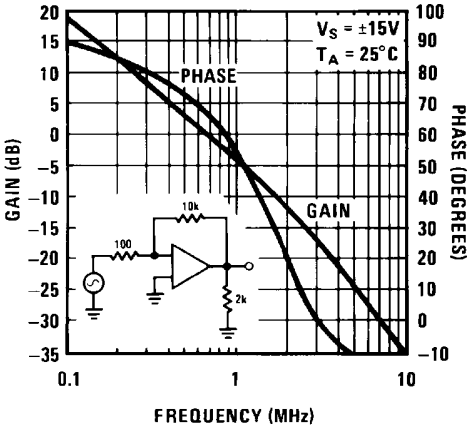


Figure 9.

Large Signal Pulse Response (LM148)

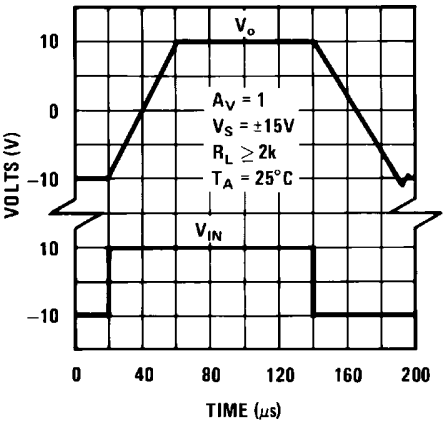


Figure 10.

Small Signal Pulse Response (LM148)

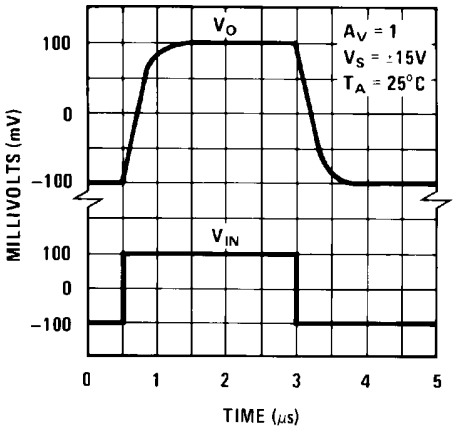


Figure 11.

Undistorted Output Voltage Swing

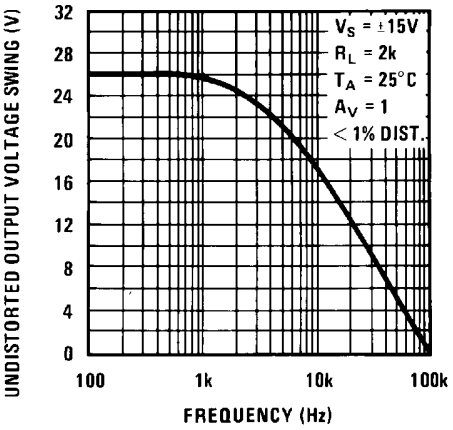


Figure 12.

Typical Performance Characteristics (continued)

Gain Bandwidth

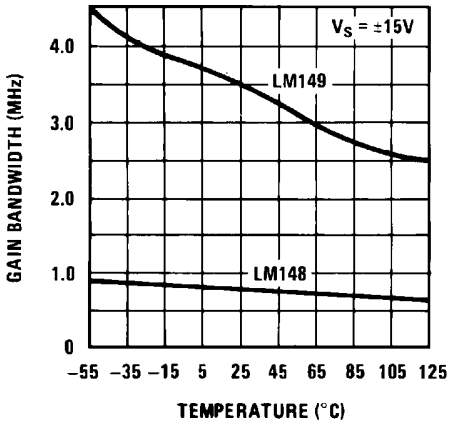


Figure 13.

Slew Rate

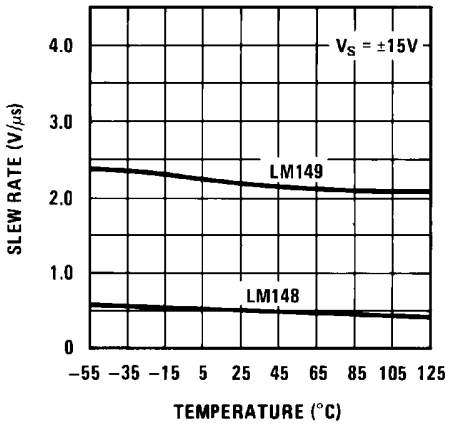


Figure 14.

Inverting Large Signal Pulse Response (LM148)

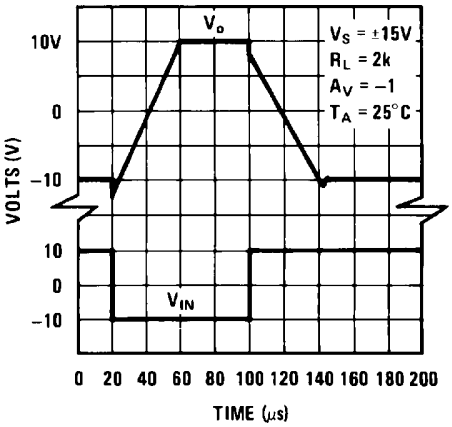


Figure 15.

Input Noise Voltage and Noise Current

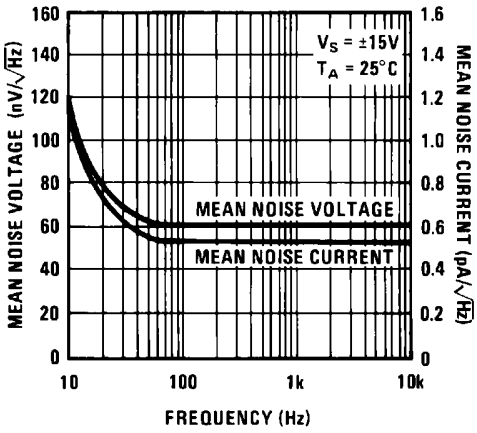


Figure 16.

Positive Common-Mode Input Voltage Limit

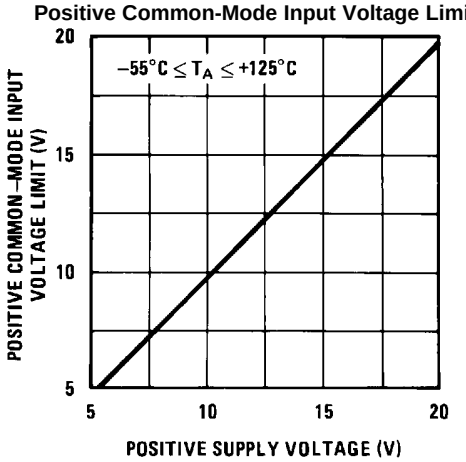


Figure 17.

Negative Common-Mode Input Voltage Limit

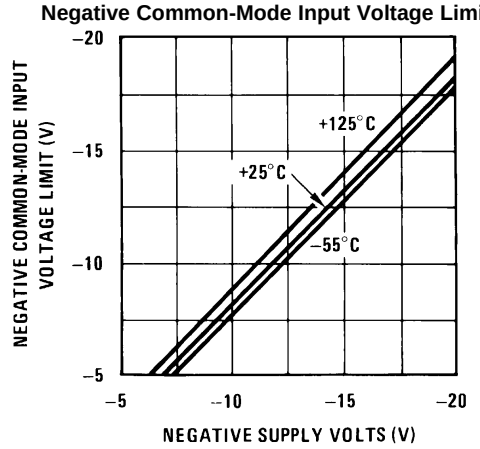


Figure 18.

APPLICATION HINTS

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

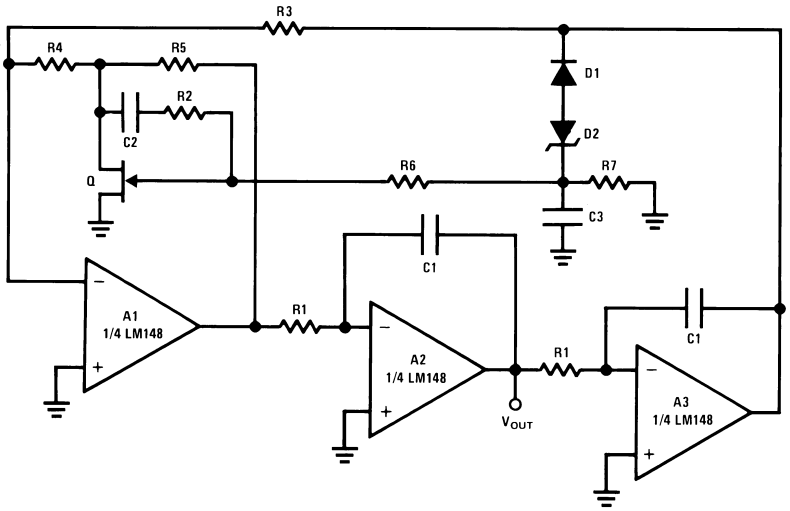
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications—LM148

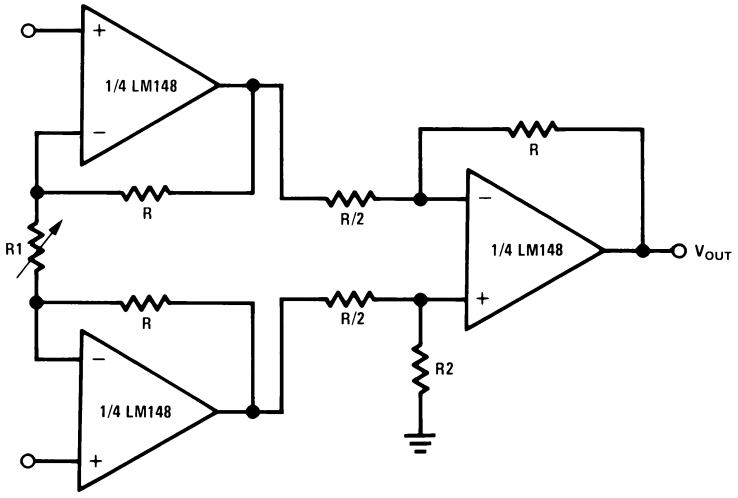
Figure 19. One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K}, K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right), \quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

f_{MAX} = 5 kHz, THD ≤ 0.03%
R1 = 100k pot. C1 = 0.0047 µF, C2 = 0.01 µF, C3 = 0.1 µF, R2 = R6 = R7 = 1M,
R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

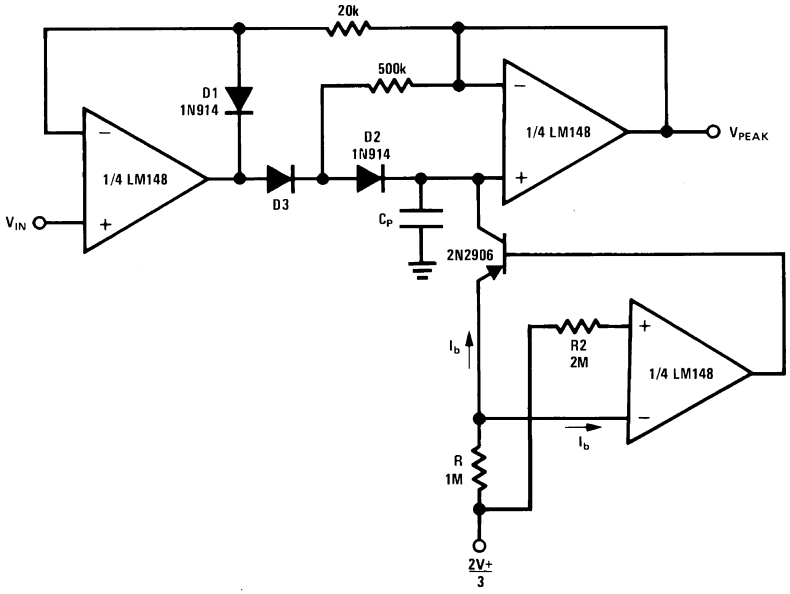
Figure 20. Low Cost Instrumentation Amplifier



$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right), V_S^- - 3V \leq V_{IN\,CM} \leq V_S^+ - 3V,$$

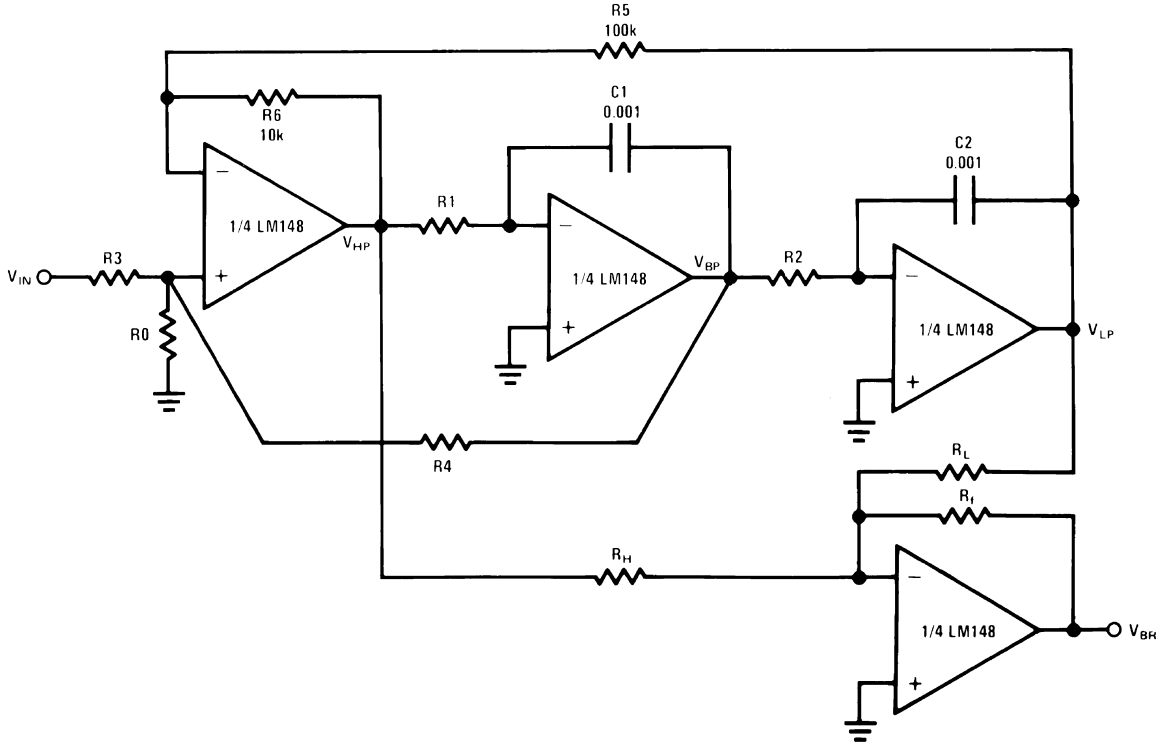
V_S = ±15V
R = R2, trim R2 to boost CMRR

Figure 21. Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
V_S = ±15V

Figure 22. Universal State-Variable Filter



Tune Q through R0,
For predictable results: f_O Q ≤ 4 × 10^4
Use Band Pass output to tune for Q

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}},\ D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o^2$$

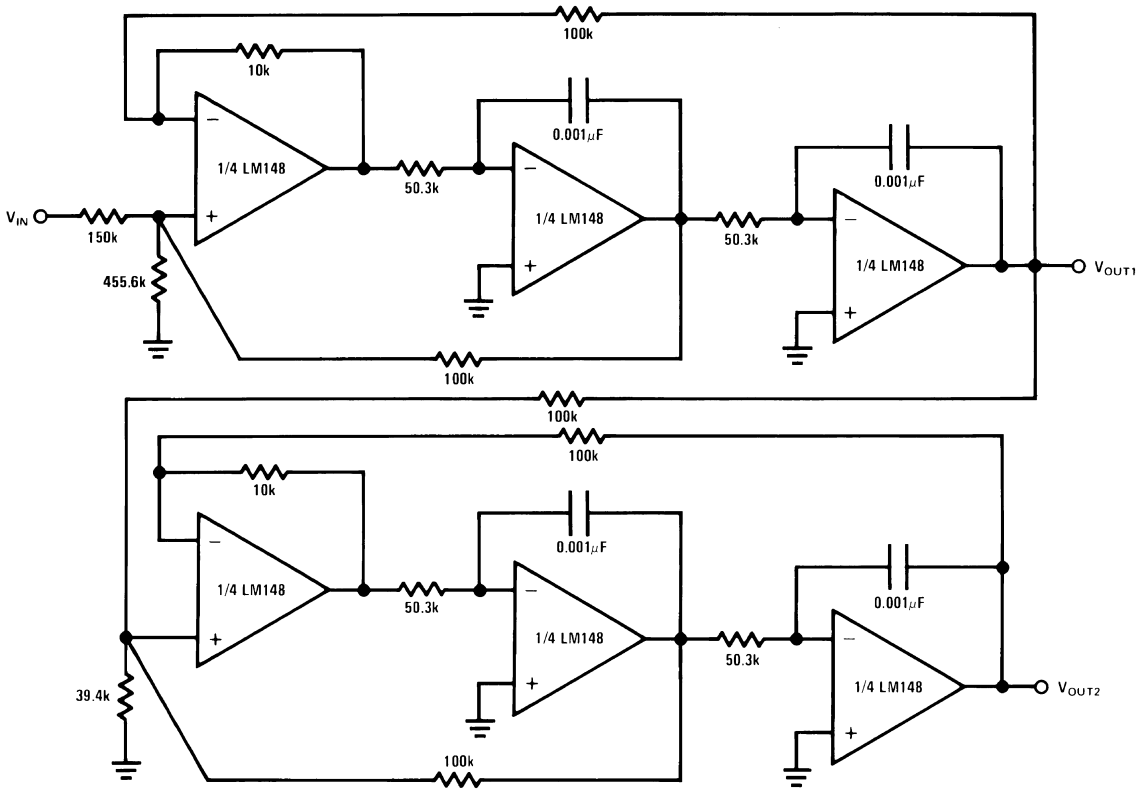
$$N_{HP(s)} = S^2\,H_{OHP},\ N_{BP(s)} = \frac{-s\omega_O\,H_{OBP}}{Q}\quad N_{LP} = \omega_o^2\,H_{OLP}.$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\,t_1\,t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

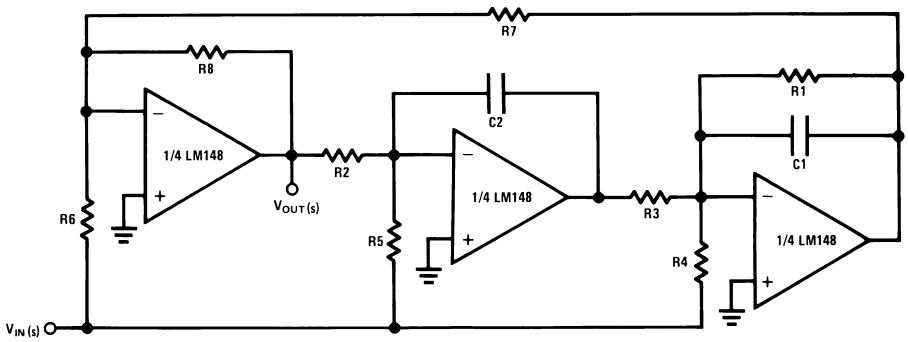
$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

Figure 23. A 1 kHz 4 Pole Butterworth



Use general equations, and tune each section separately
$Q_{1stSECTION} = 0.541,\ Q_{2ndSECTION} = 1.306$
The response should have 0 dB peaking

Figure 24. A 3 Amplifier Bi-Quad Notch Filter



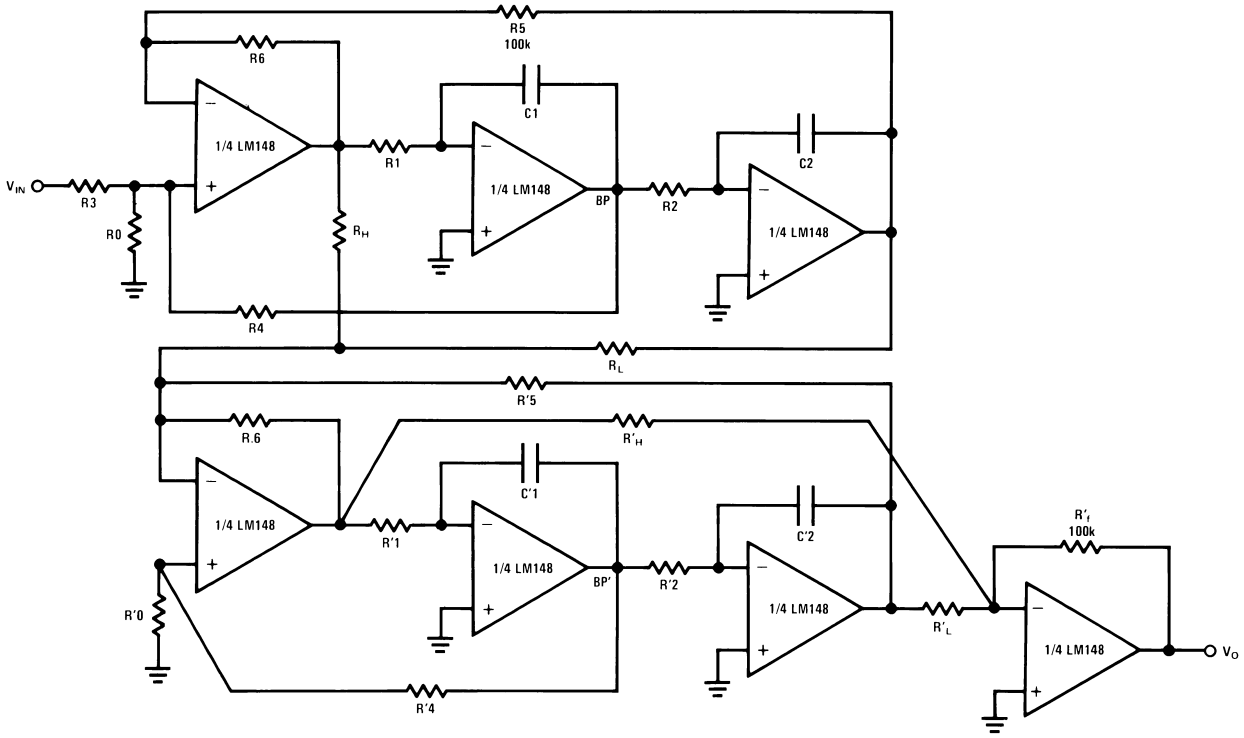
$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\ f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\ f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3 kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001 µF

Better noise performance than the state-space approach.

Figure 25. A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



R1C1 = R2C2 = t

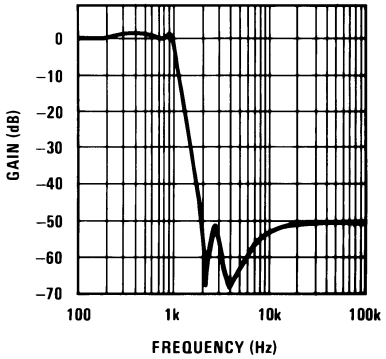
R′1C′1 = R′2C′2 = t′

f_C = 1 kHz, f_S = 2 kHz, f_p = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z = 4.92, Q′ = 4.403, normalized to ripple BW

$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

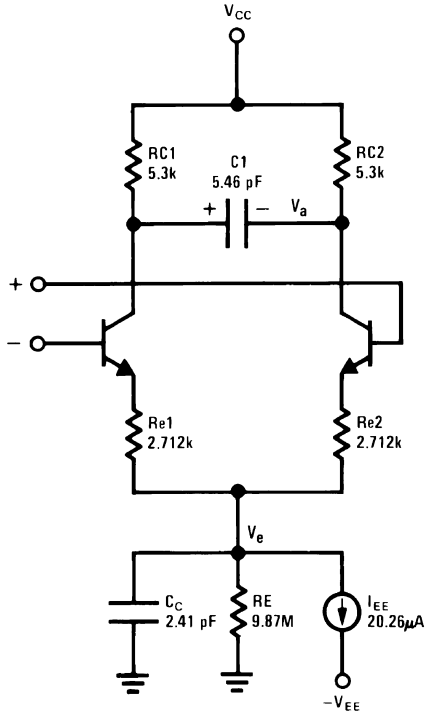
Use the BP outputs to tune Q, Q′, tune the 2 sections separately
R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,
R′1 = R′2 = 50.9k, R′4 = R′5 = 100k, R′6 = 10k, R′0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R′f = 100k. All capacitors are 0.001 µF.

Figure 26. Lowpass Response



Typical Simulation

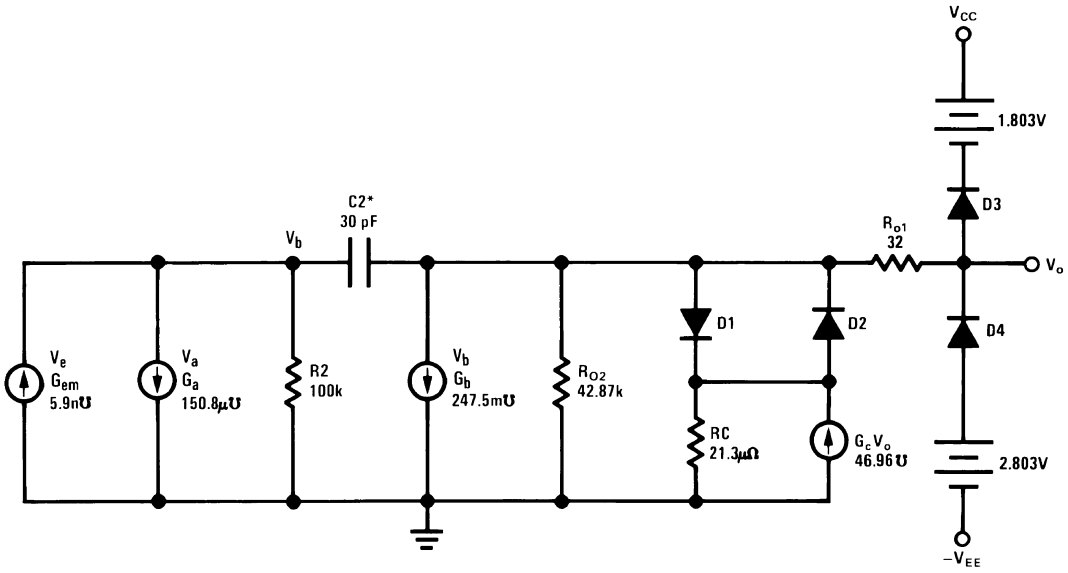
Figure 27. LM148, LM741 Macromodel for Computer Simulation



For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

$_{o1} = 112I_S = 8 \times 10^{-16}$

$_{o2}$ = 144*C2 = 6 pF for LM149



Connection Diagram

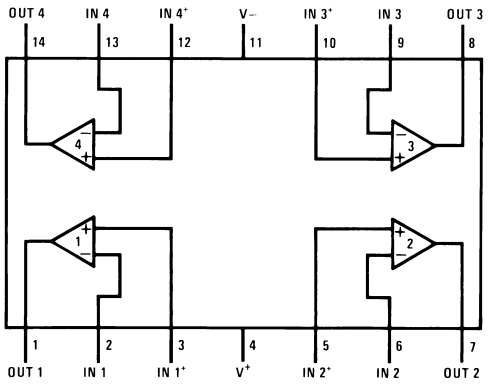


Figure 28. Top View
See Package Number J0014A, D0014A or NFF00014A

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM148J/PB	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI		LM148J	Samples
LM348M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM348M	
LM348M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM348M	Samples
LM348MX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70	LM348M	
LM348MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LM348M	Samples
LM348N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM348N	Samples
LM348N/PB	LIFEBUY	PDIP	NFF	14	25	TBD	Call TI	Call TI		LM348N	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

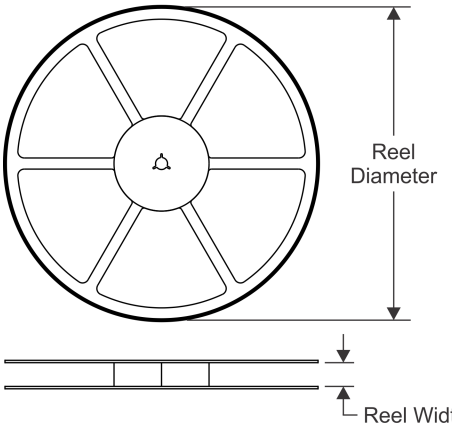
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

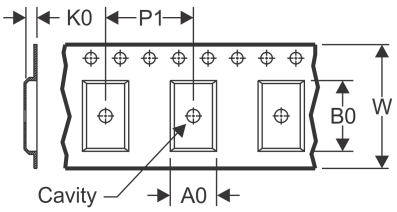
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

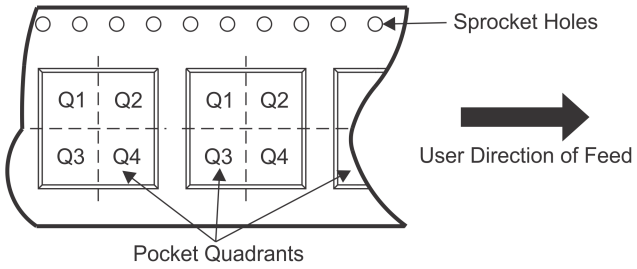


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

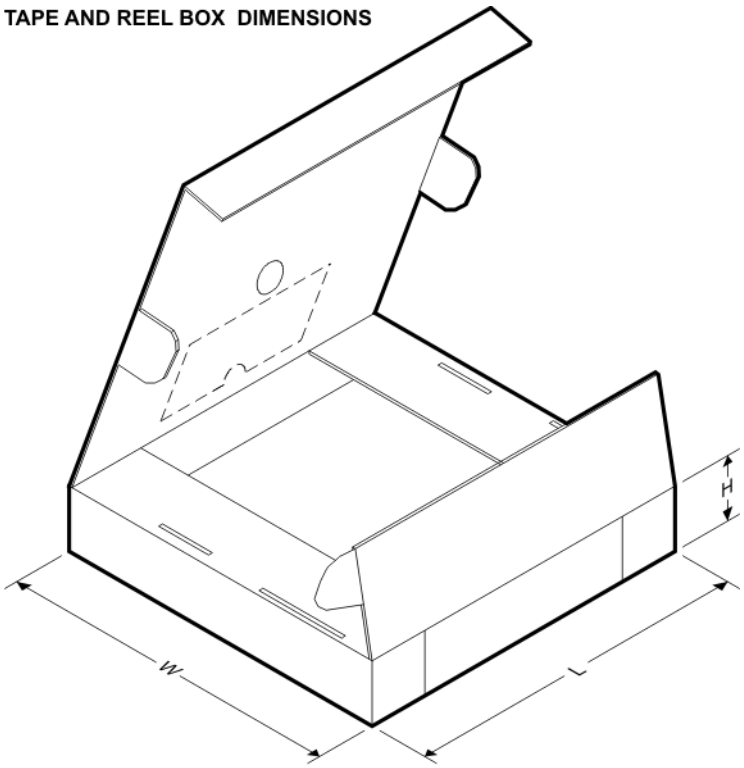
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM348MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM348MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



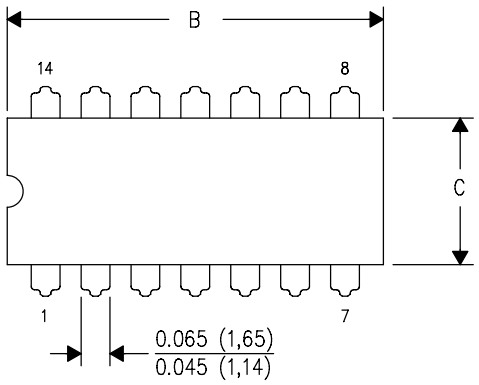
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM348MX	SOIC	D	14	2500	367.0	367.0	35.0
LM348MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

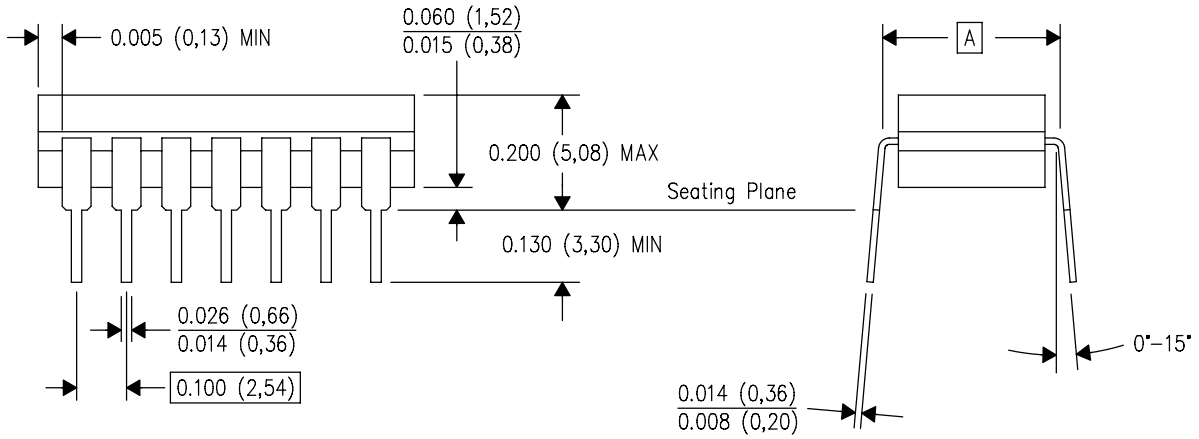
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



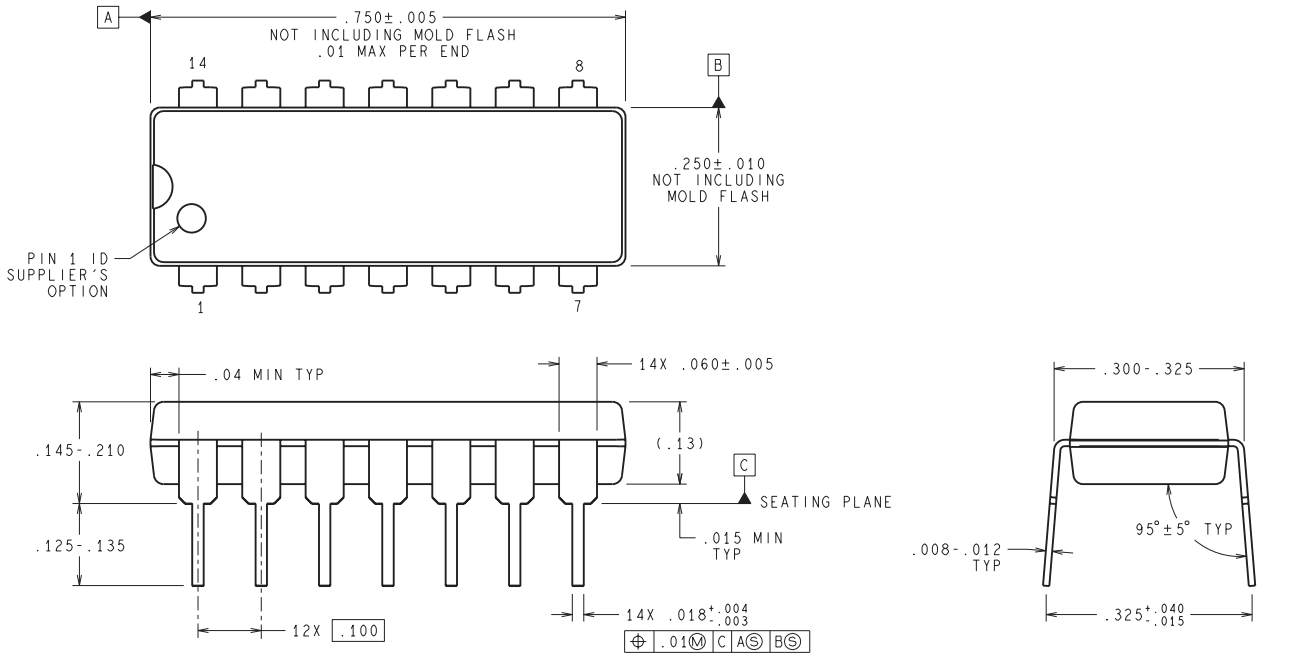
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

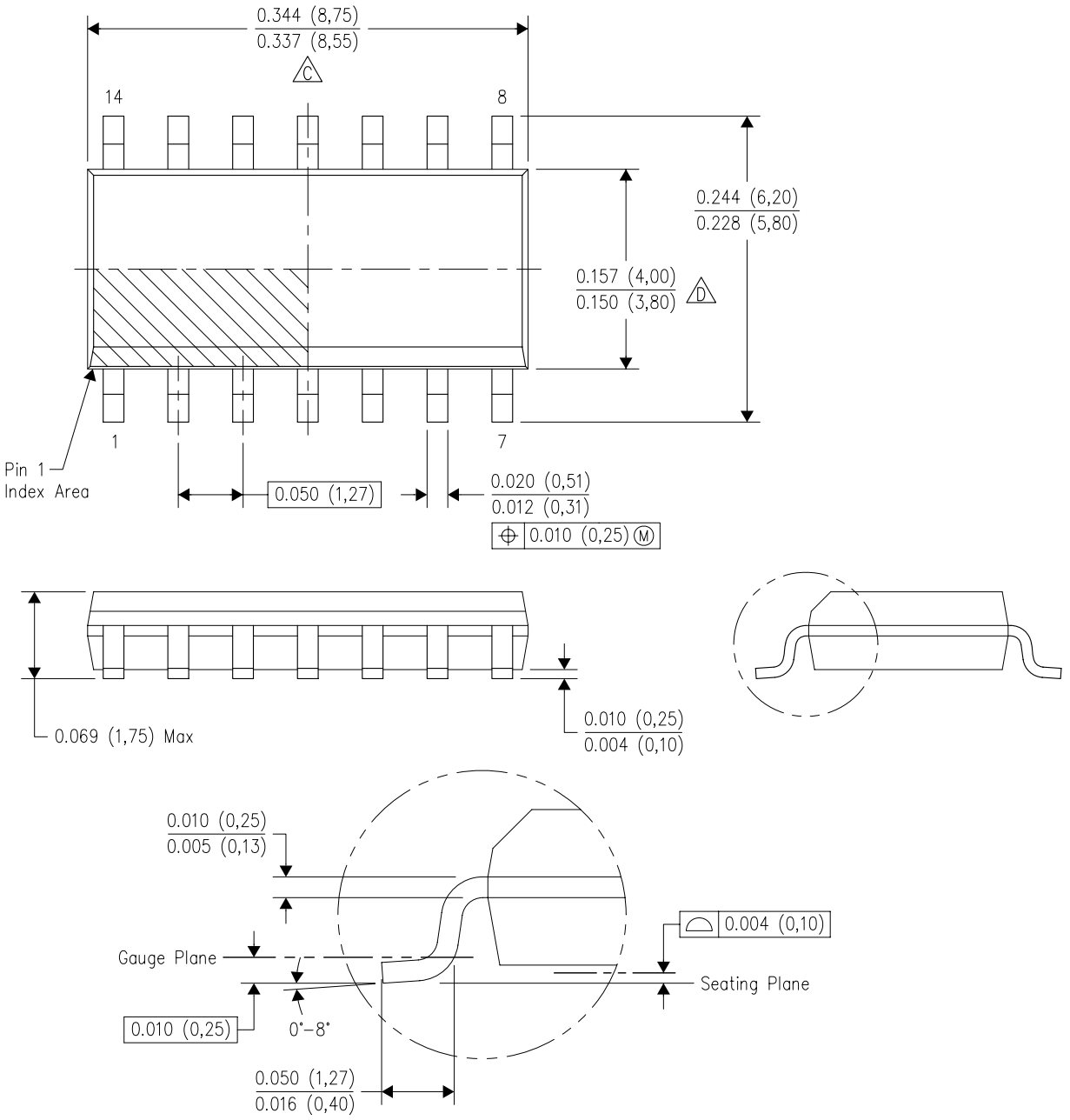
NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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