MOTOROLA

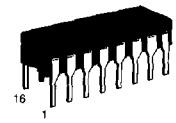
MC14541B

PROGRAMMABLE TIMER

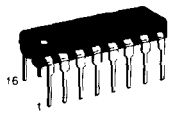
The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

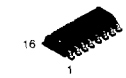
- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Built-in Low Power RC Oscillator
  (± 2% accuracy over temperature range and ± 20% supply and ± 3% over processing at < 10 kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/$\overline{Q}$ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow CLock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 = V_{DD})
  = 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 = V_{SS})



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



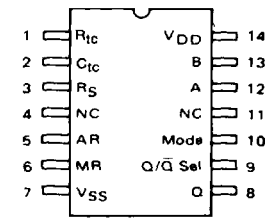
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = −55° to 125°C for all packages.

PIN ASSIGNMENT



NC = No Connection

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
I_{out}	Output Current (DC or Transient), per Pin	±45	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: All Packages: −7.0 mW/°C from 65°C to 125°C.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−7.96	—	−6.42	−12.83	—	−4.49	—	mAdc
(V_{OH} = 9.5 Vdc)		10	−4.19	—	−3.38	−6.75	—	−2.37	—	
(V_{OH} = 13.5 Vdc)		15	−16.3	—	−13.2	−26.33	—	−9.24	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.93	—	1.56	3.12	—	1.09	—	mAdc
(V_{OL} = 0.5 Vdc)		10	4.96	—	4.0	8.0	—	2.8	—	
(V_{OL} = 1.5 Vdc)		15	19.3	—	15.6	31.2	—	10.9	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Pin 5 is High) Auto Reset Disabled	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Auto Reset Quiescent Current (Pin 5 is low)	I_{DDR}	10	—	250	—	30	250	—	1500	μAdc
		15	—	500	—	82	500	—	2000	
Supply Current**† (Dynamic plus Quiescent)	I_D	5.0	I_D = (0.4 μA/kHz) f + I_{DD}							μAdc
		10	I_D = (0.8 μA/kHz) f + I_{DD}							
		15	I_D = (1.2 μA/kHz) f + I_{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†When using the on chip oscillator the total supply current (in μAdc) becomes: $I_T = I_D + 2\ C_{tc}\ V_{DD}\ f \times 10^{-3}$ where I_D is in μA, C_{tc} is in pF, V_{DD} in Volts DC, and f in kHz. (see Fig. 3) Dissipation during power-on with automatic reset enabled is typically 50 μA @ V_{DD} = 10 Vdc.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

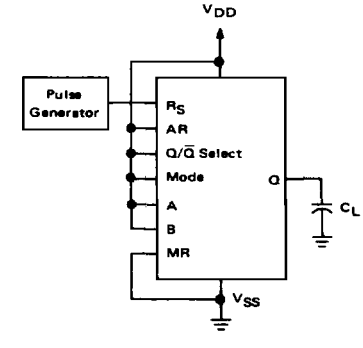
SWITCHING CHARACTERISITCS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay, Clock to Q (2^8 Output)	t_{PLH} t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3415 ns		5.0	–	3.5	10.5	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1217 ns		10	–	1.25	3.8	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 875 ns		15	–	0.9	2.9	
Propagation Delay, Clock to Q (2^{16} Output)	t_{PHL} t_{PLH}					μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	–	6.0	18	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 3467 ns		10	–	3.5	10	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2475 ns		15	–	2.5	7.5	
Clock Pulse Width	$t_{WH(cl)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0	–	1.5	0.75	MHz
		10	–	4.0	2.0	
		15	–	6.0	3.0	
MR Pulse Width	$t_{WH(R)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	
Master Reset Removal Time	t_{rem}	5.0	420	210	–	ns
		10	200	100	–	
		15	200	100	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



(R_{tc} and C_{tc} outputs are left open)

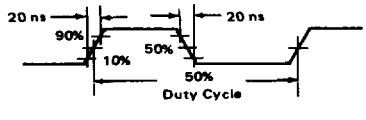
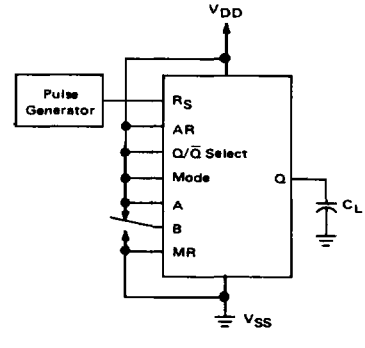
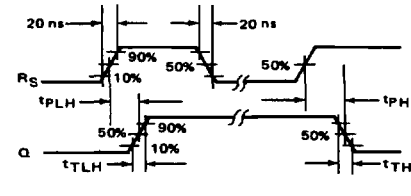


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





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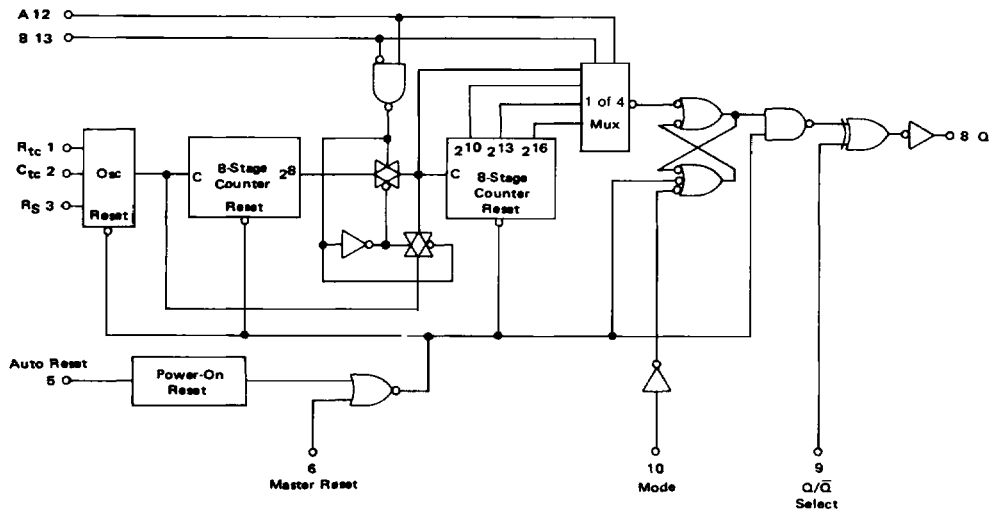
EXPANDED BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
Q/Q̄, 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode

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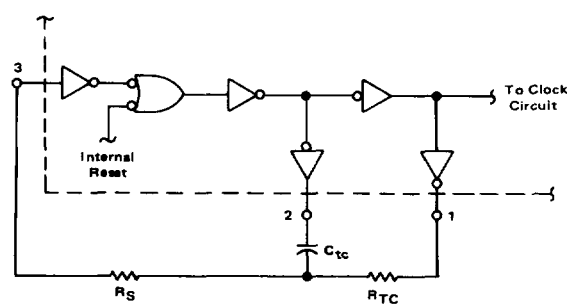
FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

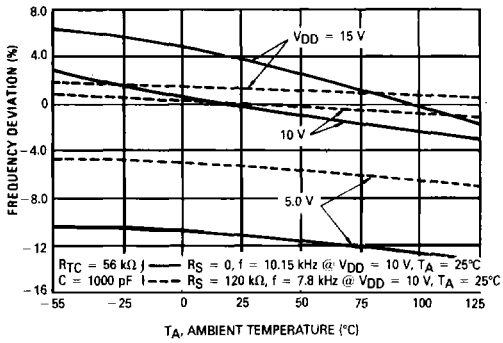
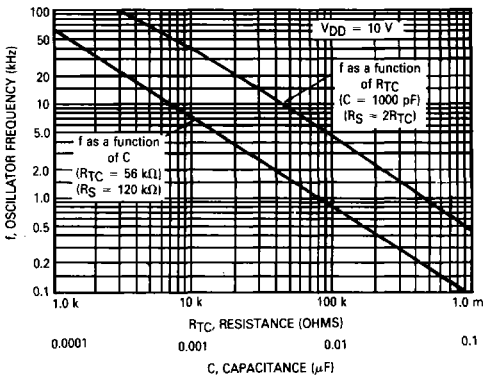


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C_{TC}



OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\,R_{tc}C_{tc}} \qquad \text{if } (1\text{ kHz} \leqslant f \leqslant 100\text{ kHz})$$

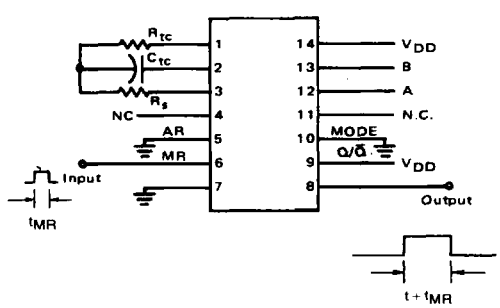
and $R_S \approx 2\,R_{tc}$ where $R_S \geqslant 10\text{ k}\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0", correspondingly when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1"

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commences, and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION



When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

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