MOTOROLA

MC3487

Quad Line Driver with Three-State Outputs

Motorola's Quad EIA–422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three–state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three–State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typical 15 ns)
- TTL Compatible
- Single 5.0 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source

QUAD EIA–422 LINE DRIVER WITH THREE–STATE OUTPUTS

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

P SUFFIX
PLASTIC PACKAGE
CASE 648

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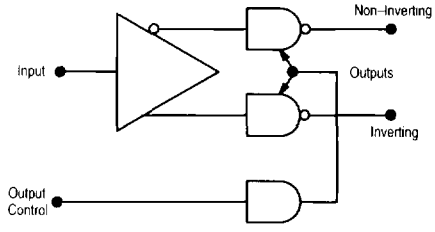
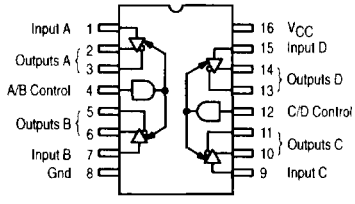
Driver Block Diagram



PIN CONNECTIONS



TRUTH TABLE

Input	Control Input	Non–Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third–State (High Impedance)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3487P	T_A = 0 to +70°C	Plastic DIP
MC3487D		SO–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	C
Operating Junction Temperature Range	T_J	150	C
Storage Temperature Range	T_{stg}	−65 to +150	C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 C ≤ T_A ≤ 70 C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25 C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	−400	µA
Input Current – High Logic State	I_{IH}				µA
(V_{IH} = 2.7 V)		–	–	+50	
(V_{IH} = 5.5 V)		–	–	+100	
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IK}	–	–	−1.5	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = −20 mA)	V_{OH}	2.5	–	–	V
Output Short–Circuit Current (V_{IH} = 2.0 V, Note 1)	I_{OS}	−40	–	−140	mA
Output Leakage Current – Hi–Z State	$I_{OL(Z)}$				µA
(V_{IL} = 0.5 V, $V_{IL(Z)}$ = 0.8 V)		–	–	+100	
(V_{IH} = 2.7 V, $V_{IL(Z)}$ = 0.8 V)		–	–	+100	
Output Leakage Current – Power OFF	$I_{OL(off)}$				µA
(V_{OH} = 6.0 V, V_{CC} = 0 V)		–	–	+100	
(V_{OL} = −0.25 V, V_{CC} = 0 V)		–	–	−100	
Output Offset Voltage Difference (Note 2)	$V_{OS} - V_{OS}$	–	–	±0.4	V
Output Differential Voltage (Note 2)	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference (Note 2)	$\lvert\Delta V_{OD}\rvert$	–	–	±0.4	V
Power Supply Current					mA
(Control Pins = Gnd, Note 3)	I_{CCX}	–	–	105	
(Control Pins = 2.0 V)	I_{CC}	–	–	85	

NOTES: 1. Only one output may be shorted at a time
2. See EIA Specification EIA–422 for exact test conditions.
3. Circuit in three–state condition

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25 C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					ns
High to Low Output	t_{PHL}	–	–	20	
Low to High Output	t_{PLH}	–	–	20	
Output Transition Times – Differential					ns
High to Low Output	t_{THL}	–	–	20	
Low to High Output	t_{TLH}	–	–	20	
Propagation Delay – Control to Output					ns
(R_L = 200 Ω, C_L = 50 pF)	$t_{PHZ(E)}$	–	–	25	
(R_L = 200 Ω, C_L = 50 pF)	$t_{PLZ(E)}$	–	–	25	
(R_L = [illegible], C_L = 50 pF)	$t_{PZH(E)}$	–	–	30	
(R_L = 200 Ω, C_L = 50 pF)	$t_{PZL(E)}$	–	–	30	

Figure 1. Three–State Enable Test Circuit and Waveforms

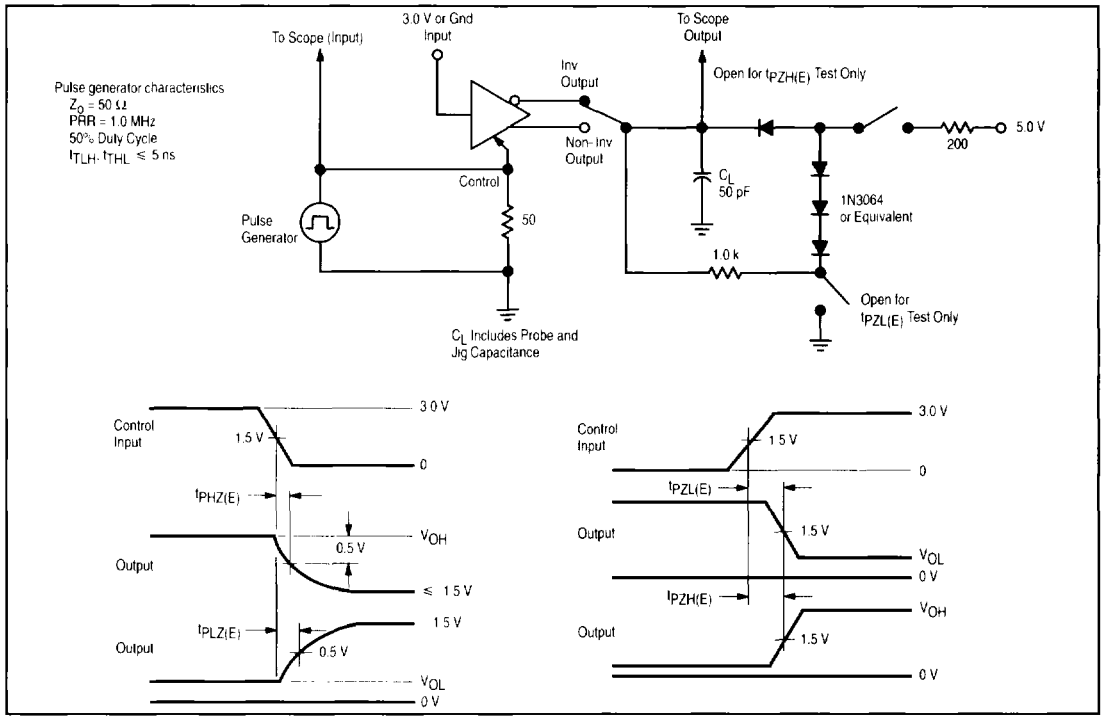


Figure 2. Propagation Delay Times Input to Output Waveforms and Test Circuit

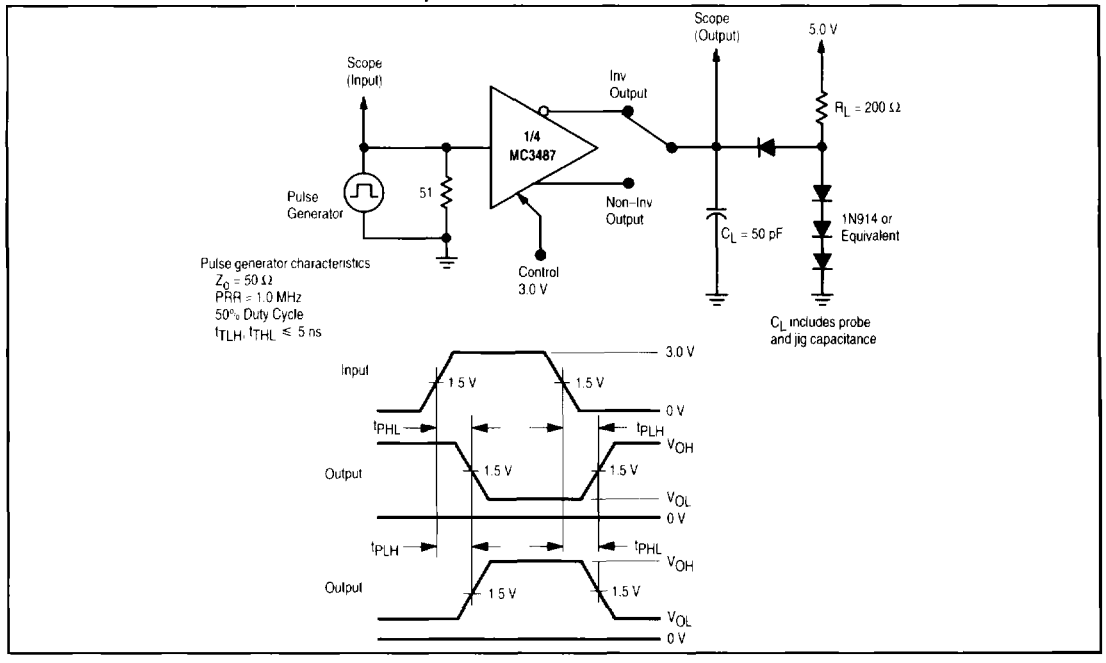


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Figure 3. Output Transition Times Test Circuit and Waveforms

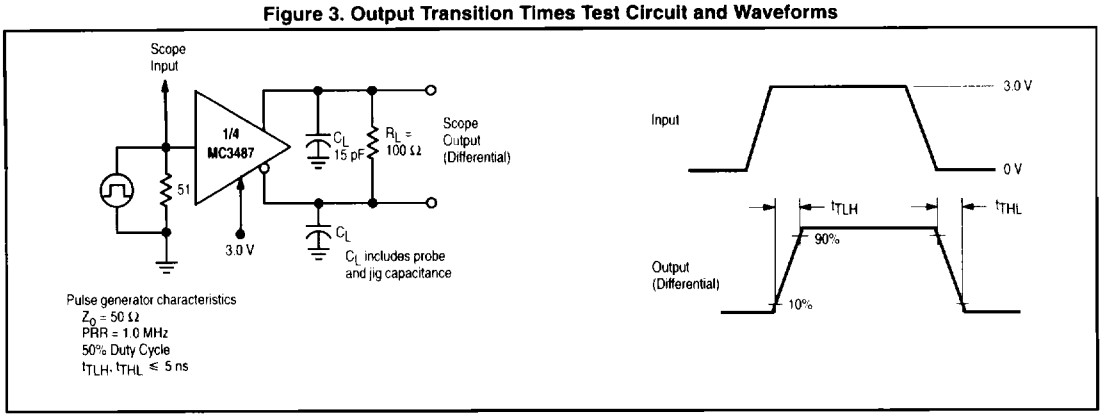

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Figure 4. Output Current versus Output Voltage

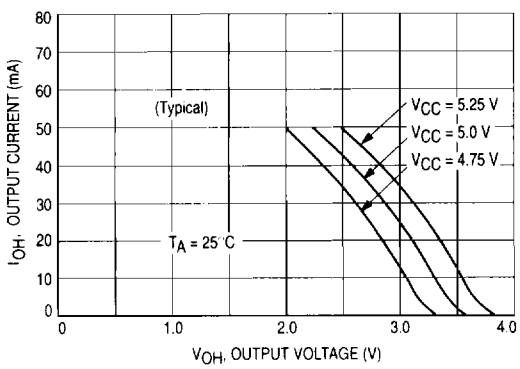

Figure 5. Output Sink Current versus Output Voltage