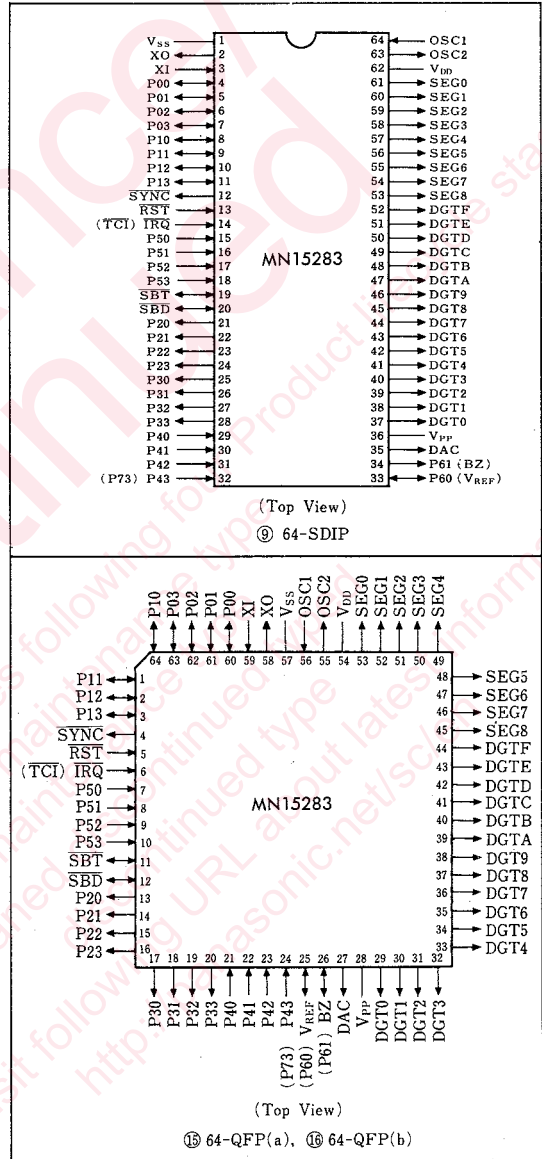


MN15283

■ Features

- ROM capacity: $8,192 \times 8$ bits
- RAM capacity: 512×4 bits
- Machine cycle: $1.91 \mu\text{s}$ (4.0 to 5.5 V)
 $6.15 \mu\text{s}$ (3.0 to 5.5 V)
- Interrupt: External interrupt 1
Timer interrupt 1
Serial interrupt 1
Watch/digit interrupt 1
Time base interrupt 1
- Timer/counter: Timer and event count functions provided by 8-bit programmable timer with 7-bit prescaler
- Serial interface: 8-bit synchronous type
- Fluorescent display tube direct drive pins: 16 for digit output, 9 for segment output
- Channel selecting function: 14-bit PWM system D/A converter
- Buzzer driver circuit incorporated: 2 kHz
- Pulse width measuring circuit incorporated: Pulse width measurable
- High impedance control: Port high impedance controllable
- System clock selector circuit incorporated: Programmable selection of system clock sources enabled. Clock sources are OSC1, OSC2 or XI, XO.
- Backup mode: STOP/HALT mode
- Operating voltage range: 3.0 to 5.5 V
- I/O pins: 8 for general purpose I/O
10 for general purpose output
8 for general purpose input
1 for serial data I/O
1 for serial clock I/O
1 for buzzer output
1 for analog input
1 for V_{REF} input
1 for PWM output
9 for fluorescent display tube segment output

■ Pin Configuration



16 for fluorescent display tube digit output
5 for LED driver output

- Process: Silicon gate CMOS
- Package: 64-QFP/SDIP
- Piggyback: EP15283

■ Pin Descriptions

Pin No.		Symbol	Pin Name	I/O	Description
64-SDIP	64-QFP				
62 1	54 57	V _{DD} V _{SS}	Power supply	I	Connect +3.0-5.5 V to V _{DD} , and 0 V to V _{SS} .
64 63	56 55	OSC1 OSC2	Clock input Clock output	I O	Oscillation terminals to connect f _{osc} ceramic oscillator or crystal oscillator. A feedback resistor is incorporated between OSC1 and OSC2.
3 2	59 58	XI XO	Clock input Clock output	I O	Event counter clock source terminals to connect a crystal oscillator. A feedback resistor between XI and XO can be selected with a mask option. They serve as an operating clock source when XI/XO is specified by clock selection.
13	5	RST	Reset input	I	Reset is applied if the "L" level is inputted over 0.3μs. A pull-up resistor can be specified with a mask option.
12	4	SYNC	SYNC. signal output	O	An internal timing signal is outputted every machine cycle at reset time.
14	6	IRQ (TCI)	External interrupt/pulse input	I	When used as an external interrupt, it receives an interrupt at a negative edge. A time base interrupt results in case of internal interrupt. TCI/IRQ can be selected through an internal port.
19	11	SBT	Serial interface clock I/O	I/O	Serial interface send/receive clock I/O terminal. It serves as an output terminal in the internal clock mode, and as an input terminal in the external clock mode. A pull-up resistor can be specified with a mask option.
20	12	SBD	Serial interface data I/O	I/O	Serial interface send/receive data I/O terminal. It inputs 8-bit serial data in the receive mode, and outputs 8-bit serial data in the send mode. An output type is either push-pull or N-channel open drain which can be selected with a mask option.
35	27	DAC	D/A converter output	O	14-bit D/A converter output terminal(PWM system). An output type is either push-pull or N-channel which can be selected with a mask option.
4~11	60~64 1~3	P00~P13	Parallel data I/O	I/O	4-bit parallel data I/O ports. Output, I/O or input can be selected with a mask option. A pull-up resistor can be specified with a mask option.
21~28	13~20	P20~P33	Parallel data output	O	4-bit parallel data output ports.
29~32 15~18	21~24 7~10	P40~P53	Parallel data input	I	4-bit parallel data input ports. A pull-up resistor can be specified with a mask option. P50-53 can be also specified for TTL level input with a mask option. P43 and P73 are commonly used.
32	24	P73	Analog input	I	Input terminal to compare with V _{REF} . P43 and P73 are commonly used.
33 34	25 26	P60(V _{REF}) ~P61 (BZ)	Parallel data output terminal/ input	O /I	2-bit parallel data output ports. P60 is the N-channel open drain output(LED directly drivable) and commonly used for V _{REF} . P61 can be specified for buzzer output with a mask option.
37~52	29~44	DGT0 ~DGTF	Fluorescent display tube digit output	O	High-voltage output terminal to be connected to a fluorescent display tube digit input terminal. Duty can be selected with a mask option. DGT0-4 can be specified for LED drivers with a mask option.

■ Pin Descriptions(Continued)

Pin No.		Symbol	Pin Name	I/O	Description
64-SDIP	64-QFP				
53~61	45~53	SEG0~ SEG8	Fluorescent display tube segment output	O	High-voltage output terminal to be connected to a fluorescent display tube segment input terminal.
36	28	V _{PP}	High - voltage power	I	High-voltage output transistor loading power supply. Normally, V _{PP} = -30 V.

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