1. FEATURES

1.1 84CXXX kernel

- 8-bit CPU, ROM, RAM, I/O in a single 42-lead shrink DIL package
- Over 80 instructions all of 1 or 2 cycles
- 29 quasi bidirectional standard I/O port lines
- Configuration of I/O lines individually selected by mask
- External interrupt T0/INTN
- 2 direct testable inputs T0, T1
- 8-bit programmable timer/event counter
- 3 single level vectored interrupts (external, timer/counter, I²C)
- Power-on-reset and low voltage detector
- Single power supply
- 2 power reduction modes: Idle and Stop
- Operating temperature range: −20 to +70 °C.
- Silicon gate CMOS fabrication process

1.2 Derivative features PCA84C640

- 6K bytes ROM
- 128 bytes RAM
- Multi-master I²C bus interface
- One 14-bit PWM output for VST
- AFC input (with 3-bit DAC and comparator)
- Five 6-bit PWM outputs for analog controls
- Eight port lines with 10 mA LED drive capability
- On screen display 2 rows of 16 characters
- OSD character set of 64 types
- Four programmable display dot sizes
- Seven colours for each character
- Half dot character rounding
- Programmable VSYNCN input polarity
- Programmable HSYNCN input polarity
- LC oscillator for on screen display function with the 84C441, 84C444, 84C641, 84C644, 84C841 and 84C844.
- RC oscillator for on screen display function with the 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843.

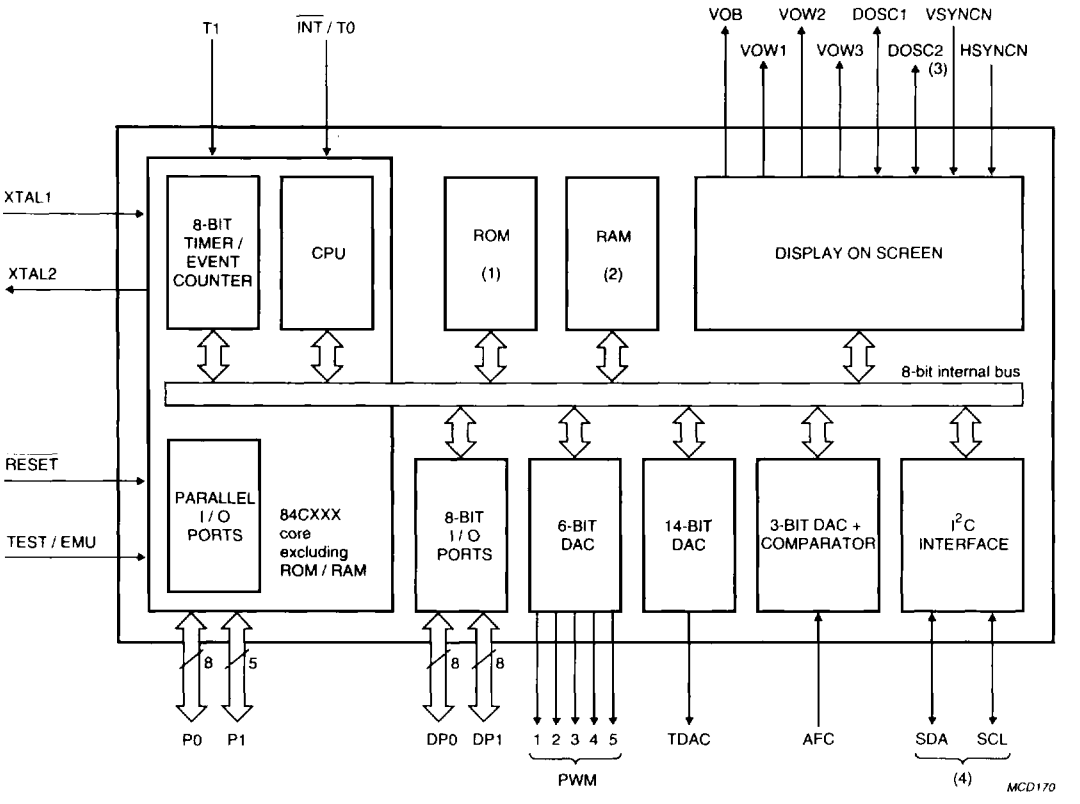
2. GENERAL DESCRIPTION

The 84C440, 84C441, 84C443, 84C444, 84C640, 84C641, 84C643, 84C644, 84C840, 84C841, 84C843 and 84C844 are 8-bit microcontrollers with On Screen Display (OSD) and Voltage Synthesized Tuning (VST) functions. All are members of the 84CXXX microcontroller family. Although the 84C640 is specifically referred to throughout this data sheet, the information applies to all the devices. The small differences between the 84C640 and the other devices are specified in the text and also highlighted in Section 12.

The 84C640 comprises the 84CXXX processor core, 6K bytes mask-programmable program ROM, 128 bytes RAM, a multi-master I²C bus interface, 2 direct testable lines, 18 general purpose bi-directional I/O lines plus 11 function-combined I/O lines, one 14-bit and five 6-bit PWM analog control outputs; AFC input for Voltage Synthesized Tuning and an On Screen Display facility for two rows of 16-characters.

Important

This data sheet details the specific properties of the 84C440, 84C441, 84C443, 84C444, 84C640, 84C641, 84C643, 84C644, 84C840, 84C841, 84C843, and 84C844. The shared characteristics of the 84CXXX family of microcontrollers are described in the 84CXXX family specification, which should be read in conjunction with this data sheet.



(1) 4 Kbytes for the 84C440, 84C441, 84C443 and 84C444. 6 Kbytes for the 84C640, 84C641, 84C643 and 84C644. 8 Kbytes for the 84C840, 84C841, 84C843 and 84C844.

(2) 128 bytes for the 84C440, 84C441, 84C443, 84C444, 84C640, 84C641, 84C643 and 84C644. 192 bytes for the 84C840, 84C841, 84C843 and 84C844.

(3) For use with an LC oscillator; only available with the 84C441, 84C444, 84C641, 84C644, 84C841 and 84C844.

(4) I²C-bus interface not available with the 84C443, 84C444, 84C643, 84C644, 84C843 and 84C844.

Fig.1 Block diagram.

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	MATERIAL	CODE	
PCA84C440	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C441	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C443	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C444	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C640	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C641	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C643	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C644	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C840	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C841	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C843	42	SDIL	plastic	SOT270	−20 to + 70
PCA84C844	42	SDIL	plastic	SOT270	−20 to + 70

Note

A 48-lead QFP package will be available shortly.

4. PINNING INFORMATION

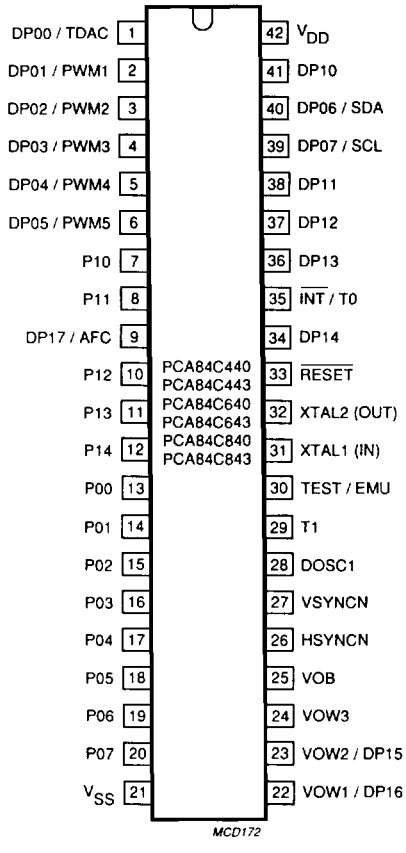


Fig.2 Pinning diagram; 84C440; 84C443; 84C640, 84C643, 84C840 and 84C843

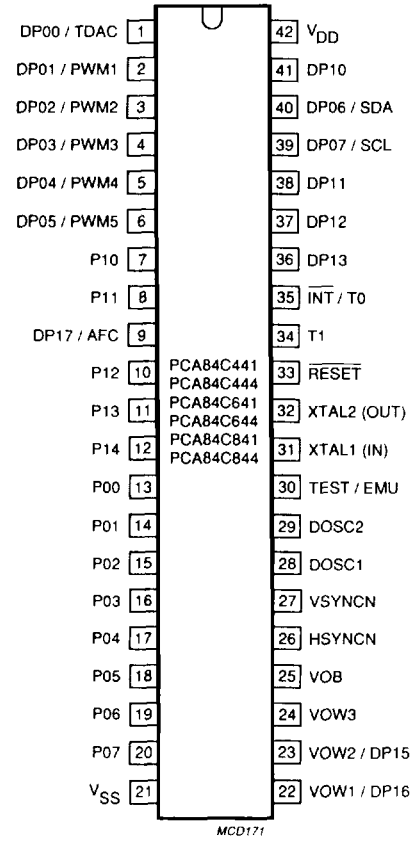


Fig.3 Pinning diagram; 84C441; 84C444; 84C641, 84C644, 84C841 and 84C844

Table 1 Pin description - 84C440; 84C443; 84C640, 84C643, 84C840 and 84C843

SYMBOL	PIN	DESCRIPTION
DP0.0/TDAC	1	Derivative Port 0 : quasi-bidirectional I/O line or 14-bit DAC PWM
DP0.1 to DP0.5/ PWM1 to PWM5	2 to 6	Derivative Port 1 : quasi-bidirectional I/O lines or 6-bit DAC PWM
P1.0 to P1.4	7, 8, 10 to 12	Port 1: quasi-bidirectional I/O lines
P0.0 to P0.7	13 to 20	Port 0: quasi-bidirectional I/O port
DP1.7/AFC	9	Derivative Port 1 : quasi-bidirectional I/O line or comparator input with 3-bit DAC
DP0.6/SDA	40	Derivative open drain I/O port or I²C-bus data line
DP0.7/SCL	39	Derivative open drain I/O port or I²C- bus clock line
$\overline{INT}$/T0	35	External interrupt or direct testable line
DP1.0 to DP1.4	41, 38, 37, 36, 34	Derivative Port 1: quasi-bidirectional I/O lines
DP1.5 to DP1.6/ VOW2 to VOW1	23, 22	Derivative Port 1 : quasi-bidirectional I/O lines or character video output
$\overline{RESET}$	33	Initialize input, active low
XTAL2, XTAL1	32, 31	Oscillator output or input terminal for system clock
TEST/EMU	30	Control input for testing and emulation mode. Ground for normal operation.
T1	29	Direct testable pin and event counter input
DOSC1	28	Connection to RC oscillator of OSD clock
VSYNCN	27	Vertical synchronous signal input
HSYNCN	26	Horizontal synchronous signal input
VOB	25	Blanking output
VOW3	24	Character video output of OSD
V_{SS}	21	Ground terminal
V_{DD}	42	Power supply terminal

Table 2 Pin description - 84C441; 84C444; 84C641, 84C644, 84C841 and 84C844

SYMBOL	PIN	DESCRIPTION
DP0.0/TDAC	1	Derivative Port 0 : quasi-bidirectional I/O line or 14-bit DAC PWM
DP0.1 to DP0.5/ PWM1 to PWM5	2 to 6	Derivative Port 1 : quasi-bidirectional I/O lines or 6-bit DAC PWM
P1.0 to P1.4	7, 8, 10 to 12	Port 1: quasi-bidirectional I/O lines
P0.0 to P0.7	13 to 20	Port 0: quasi-bidirectional I/O port
DP1.7/AFC	9	Derivative Port 1 : quasi-bidirectional I/O line or comparator input with 3-bit DAC
DP0.6/SDA	40	Derivative open drain I/O port or I²C-bus data line
DP0.7/SCL	39	Derivative open drain I/O port or I²C-bus clock line
$\overline{INT}$/T0	35	External interrupt or direct testable line
DP1.0 to DP1.3	41, 38, 37, 36	Derivative Port 1: quasi-bidirectional I/O lines
DP1.5 to DP1.6/ VOW2 to VOW1	23, 22	Derivative Port 1 : quasi-bidirectional I/O lines or character video output
$\overline{RESET}$	33	Initialize input, active low
XTAL2, XTAL1	32, 31	Oscillator output/input terminals for system clock
TEST/EMU	30	Control input for testing and emulation mode. Ground for normal operation.
T1	34	Direct testable pin and event counter input
DOSC1/DOSC2	28, 29	Connections to LC oscillator of OSD clock
VSYNCN	27	Vertical synchronous signal input
HSYNCN	26	Horizontal synchronous signal input
VOB	25	Blanking output
VOW3	24	Character video output of OSD
V_{SS}	21	Ground terminal
V_{DD}	42	Power supply terminal

5. RESET

The $\overline{\text{RESET}}$ pin is used as an active low input to initialize the microcontroller to a defined state. The Reset configuration is shown in Fig.5.

The Power-on-reset circuit monitors the voltage level of V_{DD}. If V_{DD} remains below the internal reference voltage level V_{ref} (typically 3.6 V), the oscillator is inhibited. When V_{DD} rises above V_{ref}, the oscillator is released and the internal reset is active for a period of t_d (typically 50 µs).

Three modes of Power-on-reset are possible:

1. An external $\overline{\text{RESET}}$ signal is applied during power-on.
2. If V_{DD} rises above the minimum operation voltage before time period t_d is exceeded, no external components are necessary, (See Fig 6).
3. External components are required if V_{DD} has a slow rise time, such that after the time period ($t_{Vref} + t_d$) has elapsed the supply voltage is still below the minimum operation voltage (V_{min}). See Figs 7 and 4. In order to ensure a correct reset operation the time constant RC must be $\geq 8t_{VDD}$.

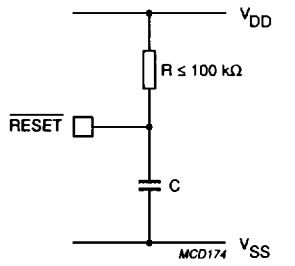


Fig.4 External components for $\overline{\text{RESET}}$ pin.

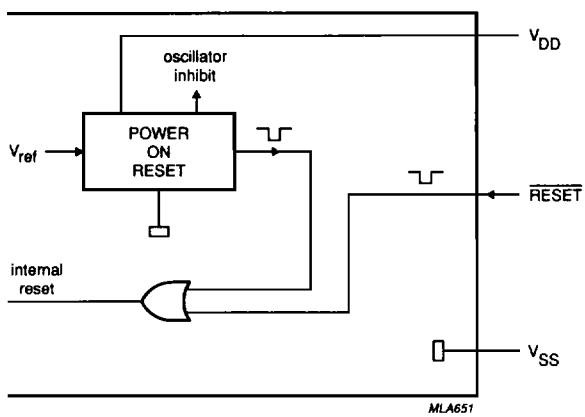


Fig.5 Reset configuration.

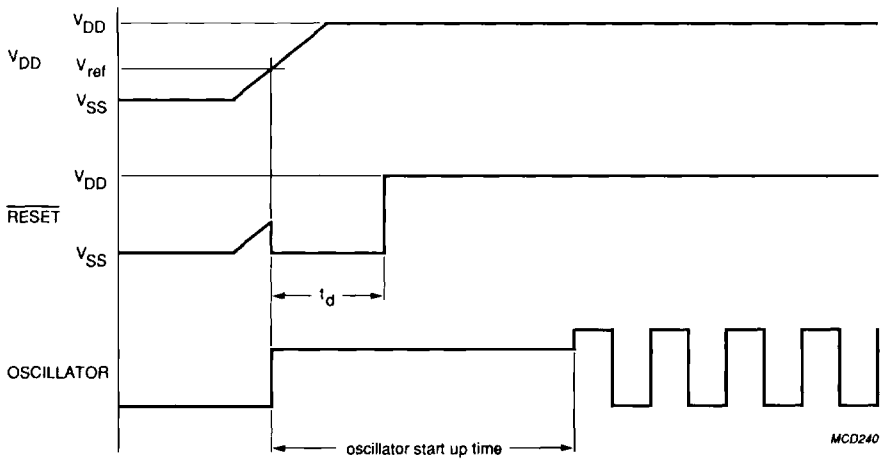


Fig.6 Reset with fast rising V_{DD}.

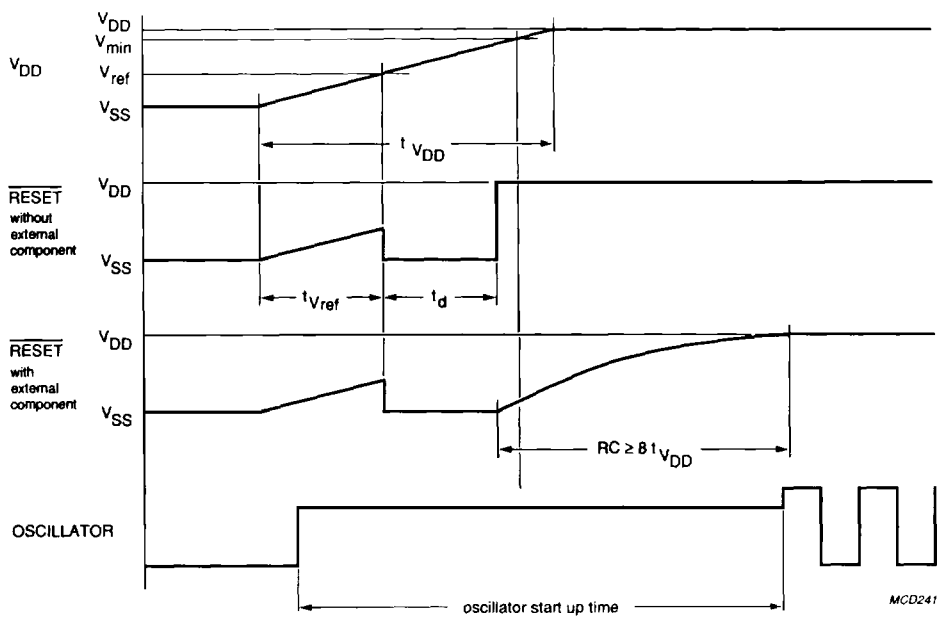


Fig.7 Reset with slow rising V_{DD}.

6. ANALOG CONTROL; 6-BIT PWM DACs

Five PWM outputs are available for analog control purposes e.g. volume, balance, brightness, saturation etc. The block diagram of a typical 6-bit PWM DAC is shown in Fig.8. Each PWM output can generate pulses of programmable length that have a repetition frequency of $f_{PWM}/64$, (where $f_{PWM} = f_{XTAL}/3$). The polarity of all five PWM outputs is selected by the state of the polarity control bit (P6LVL). Setting P6LVL to a logic 1 inverts all five PWM outputs. If the state of P6LVL is a logic 0, then the PWM outputs are not inverted. The PWM outputs PWM1 to PWM5, share the same pins as the Derivative Port lines DP0.1 to DP0.5. The PWM output function, for individual pins, is selected by setting the relevant PWM enable bit (PWMxE) to '1'. The Derivative Port function is selected by setting the relevant PWMxE bit to '0'.

A DC voltage proportional to the PWM control setting may be obtained by connecting an integrating network to each of the PWM outputs (see Fig.9). The analog value is calculated by multiplying the ratio of the high time and the repetition time of the pulse, by V_O.

The high time of any PWM output is: $t_{HIGH} = t_0 \times PWMDL$.

where: $t_0 = 3/f_{XTAL}$ and PWMDL is the decimal value of the contents of the PWM data latch.

The repetition time of any PWM output is: $t_R = t_0 \times 64$

Therefore, the analog output voltage is:
$V_A = (PWMDL/64) \times V_0$

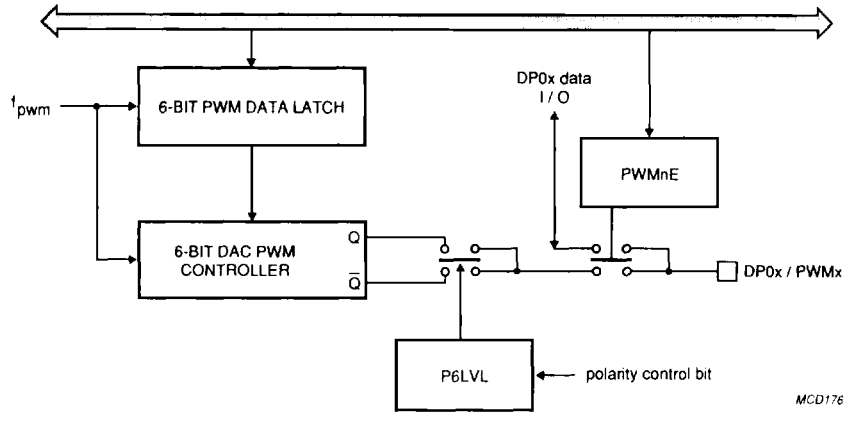


Fig.8 Block diagram; 6-bit PWM DAC.

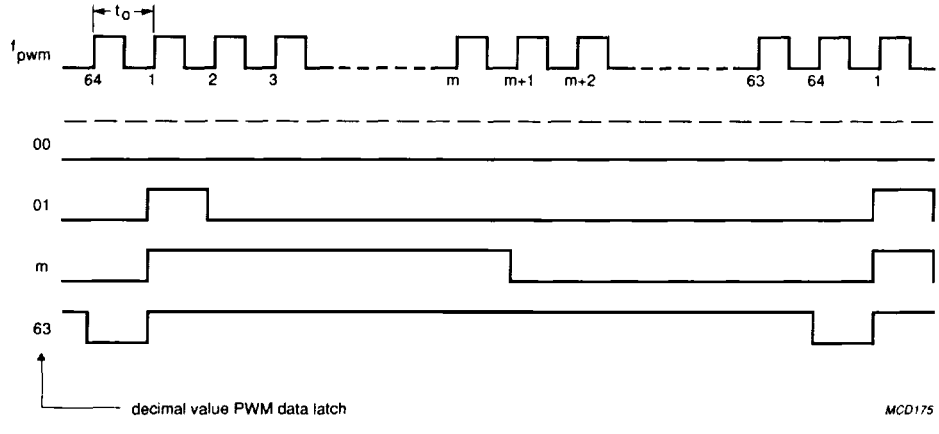


Fig.9 PWM output patterns (P6LVL = 0).

7. VST CONTROL; 14-BIT PWM DAC

The PCA84C640 has one 14-bit PWM DAC output with a resolution of 16384 levels for Voltage Synthesized Tuning. The PWM DAC is shown in Fig. 10 and consists of the following:

- two 7-bit DAC interface latches
- one 14-bit DAC data latch
- 14-bit counter
- pulse control

The 14-bit counter is continuously running and is clocked by f_0. The period (t_0) of the clock is $3/f_{XTAL}$.

The repetition time for one complete cycle of the 14-bit counter is: $t_r = t_0 \times 16384$.

The repetition time for one cycle of the lower 7-bits of the counter is: $t_{sub} = t_0 \times 128$.

Therefore, the number of t_{sub} periods in a complete cycle t_r is: $N = t_0 \times 16384/t_0 \times 128 = 128$

In order to ensure correct operation, data latch VSTH is loaded first and then data latch VSTL. The contents of VSTH are used for coarse adjustment; the contents of VSTL for fine adjustment. At the beginning of the first t_{sub} period following the loading of VSTL, both data latches are downloaded into data latch VSTREG. After the contents of VSTH and VSTL are latched into VSTREG one t_{sub} period is needed to generate the appropriate pulse pattern. To ensure correct DAC conversion two t_{sub} periods should be allowed before beginning the next sequence.

7.1 Coarse adjustment

The coarse adjustment output (OUT1) is reset LOW (inactive) at the start of each t_{sub} period. It will remain LOW until the time $t_0 \times (VSTH + 1)$ has elapsed and then will go HIGH and remain so until the next t_{sub} period starts.

7.2 Fine adjustment

Fine adjustment is achieved by generating additional pulses at the start of particular sub-periods. These pulses have a width of t_0. The subperiod in which a pulse is added is determined by the contents of VSTL data latch. Table 3 gives the subperiod numbers at the start of which an additional pulse is generated, depending on the bit in VSTL being '0'. When more than one bit is '0' a combination of additional pulses are generated. For example if VSTL = 1111010 additional pulses will be given in subperiods 16, 48, 64, 80 and 112; this is illustrated in Fig.12.

If VSTH = 0011101, VSTL = 1111010 and P14LVL = 0, then the TDAC output is as shown in Fig. 13.

Table 3 Additional pulse distribution

LOWER 7 BITS (VSTL)	ADDITIONAL PULSE IN SUBPERIODS t_{SUBN}
111 1110	64
111 1101	32, 96
111 1011	16, 48, 80, 112
111 0111	8, 24, 40, 56, 72, 88, 104, 120
110 1111	4, 12, 20, 28, 36, 44, 52, 60 .... 116, 124
101 1111	2, 6, 10, 14, 18, 22, 26, 30, ... 122, 126
011 1111	1, 3, 5, 7, 9, 11, 13, 15, 17, ... 125, 127

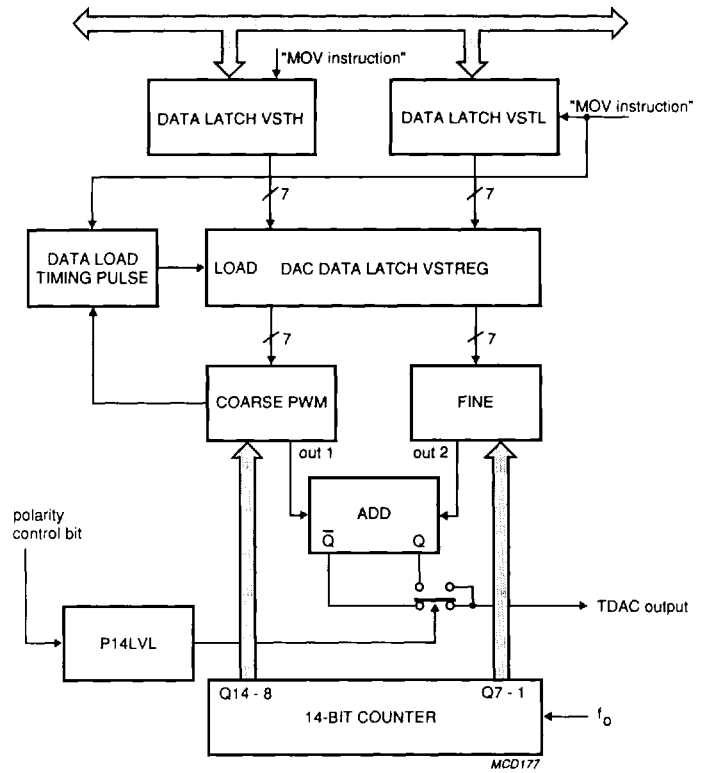


Fig.10 Block diagram: 14-bit PWM DAC.

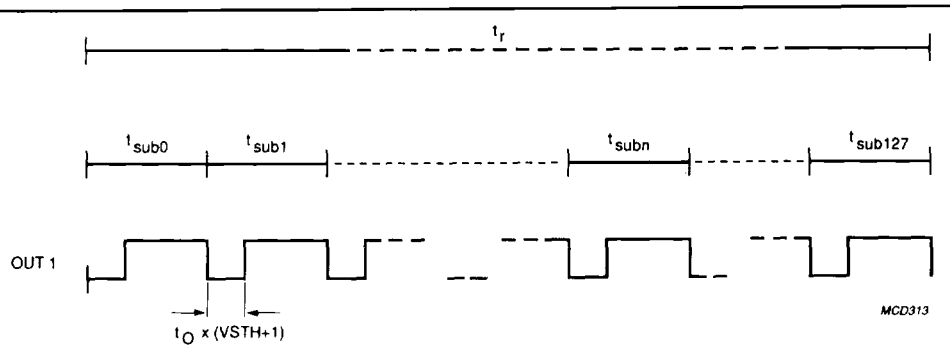


Fig.11 Coarse adjustment output (Out1).

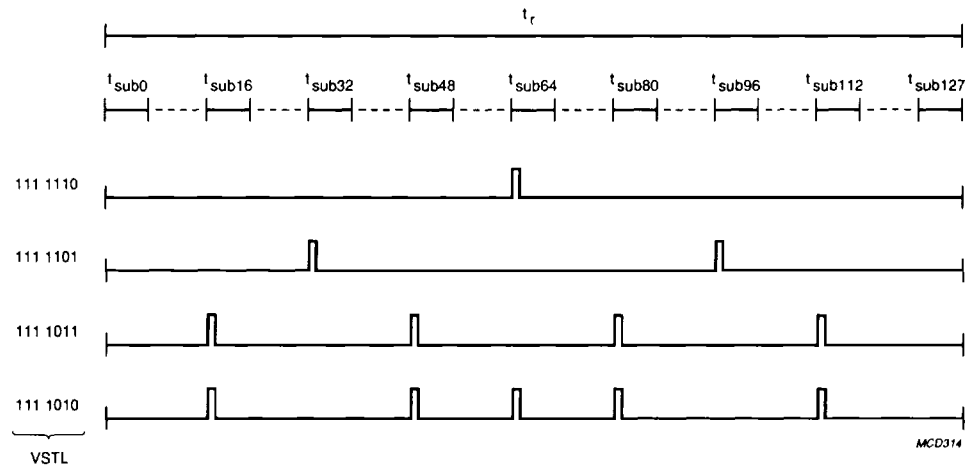


Fig.12 Fine adjustment output (Out2).

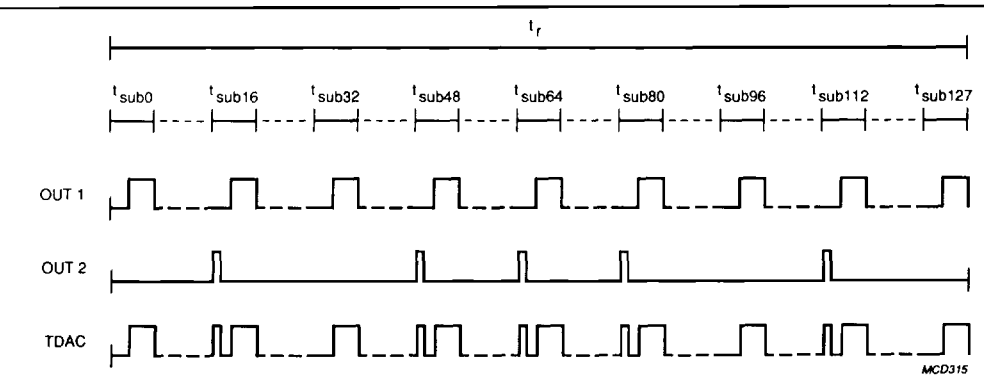


Fig.13 TDAC output.

8. AFC INPUT

The AFC input is used to measure the level of the Automatic Frequency Control signal. This is achieved by comparing the AFC input signal with the output of a 3-bit DAC as shown in Fig.14. DAC analog switches select one of 8 resistor taps connected between V_{DD} and V_{SS}. Consequently, eight different voltages may be selected (see Table 4). The compare signal AFCC, can be tested to determine whether the AFC input is higher or lower than the DAC level. The AFC input shares the same pin as the Derivative Port line DP1.7. The AFC function is selected by setting the enable bit AFCE to a logic 1. The Derivative Port function is selected by setting the AFCE bit to a logic 0.

Table 4 Selection of V_{ref}

AFC2	AFC1	AFC0	V_{ref}	V_{ref} (V_{DD} = 5.0 V)
0	0	0	V_{DD} x 0.125	0.625 V
0	0	1	V_{DD} x 0.250	1.250 V
0	1	0	V_{DD} x 0.375	1.875 V
0	1	1	V_{DD} x 0.500	2.500 V
1	0	0	V_{DD} x 0.625	3.125 V
1	0	1	V_{DD} x 0.750	3.750 V
1	1	0	V_{DD} x 0.875	4.375 V
1	1	1	V_{DD}	5.000 V

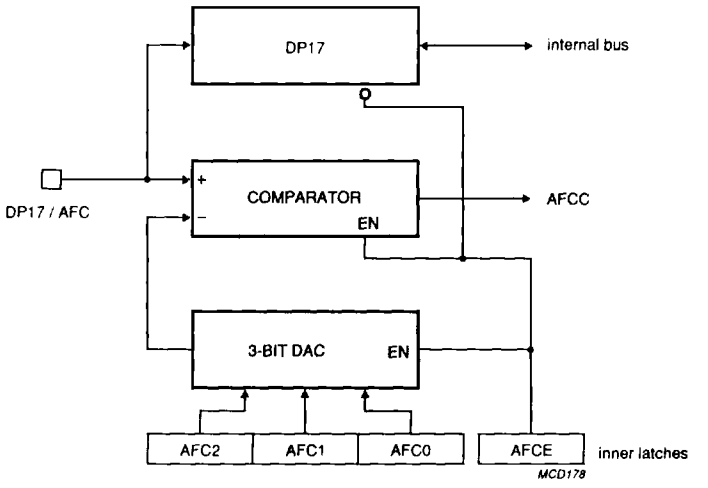


Fig.14 AFC circuit.

9. I/O

Each parallel I/O port line may be individually configured using one of three possible I/O mask options. The three I/O mask options are specified below:-

Option 1: Standard port with switched pull-up current source (see Fig. 15).

Option 2: Open drain (see Fig. 16).

Option 3: Push-pull (output only, see Fig. 17).

Table 5 specifies the possible port option list. When these devices are used for emulation purposes, in order to match the piggy back device provided it is recommended that the port options listed in Table 6 are used.

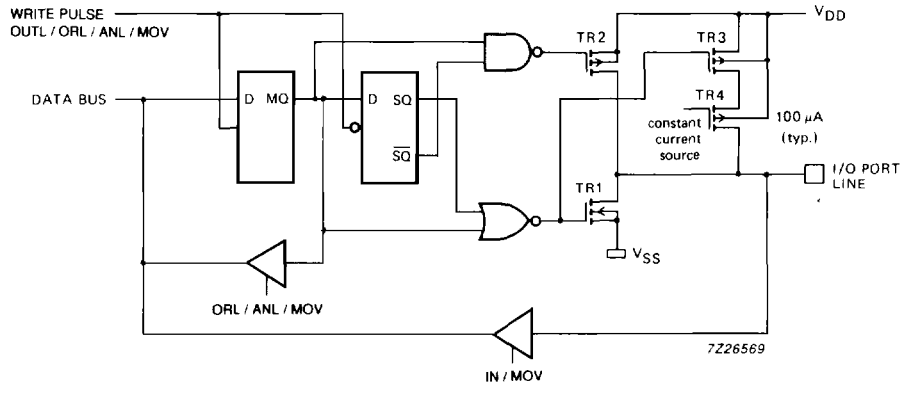


Fig.15 Standard output with switched pull-up current source (Option 1).

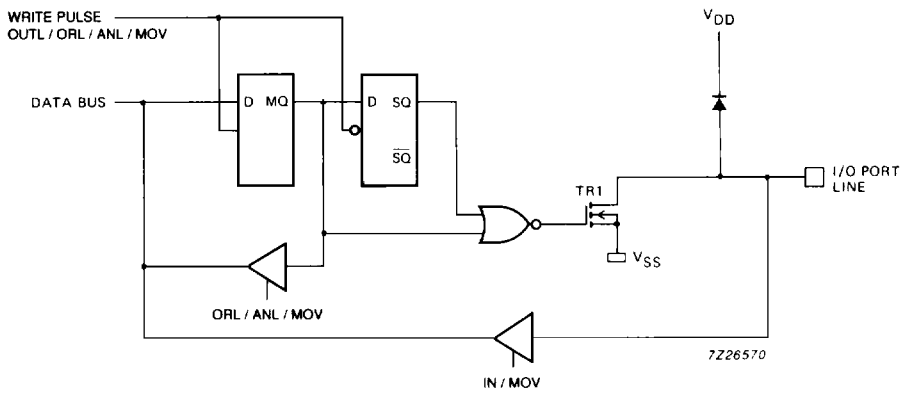


Fig.16 Open drain type I/O (Option 2).

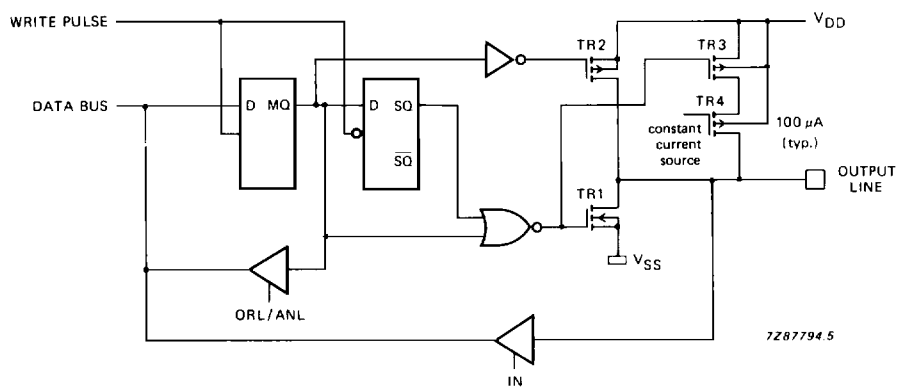


Fig.17 Push-pull type output (Option 3).

Table 5 User mask programmable port option list

PORT	PIN
P0.0	13
P0.1	14
P0.2	15
P0.3	16
P0.4	17
P0.5	18
P0.6	19
P0.7	20
P1.0	7
P1.1	8
P1.2	10
P1.3	11
P1.4	12
DP0.0	1
DP0.1	2
DP0.2	3
DP0.3	4
DP0.4	5
DP0.5	6
DP0.6	40
DP0.7	39
DP1.0	41
DP1.1	38
DP1.2	37
DP1.3	36
DP1.4	34
DP1.5	23
DP1.6	22
DP1.7	9
VOB	25.
VOW3	24.

Table 6 Port options for the 84C640 in emulation mode

PORT	PIN	OPTION
P0.0	13	1
P0.1	14	1
P0.2	15	1
P0.3	16	1
P0.4	17	1
P0.5	18	1
P0.6	19	1
P0.7	20	1
P1.0	7	1
P1.1	8	1
P1.2	10	1
P1.3	11	1
P1.4	12	1
DP0.0	1	
DP0.1	2	
DP0.2	3	
DP0.3	4	
DP0.4	5	
DP0.5	6	
DP0.6	40	2 S
DP0.7	39	2 S
DP1.0	41	
DP1.1	38	
DP1.2	37	
DP1.3	36	
DP1.4	34	
DP1.5	23	
DP1.6	22	
DP1.7	9	
VOB	25	
VOW3	24	

Notes

1. DP1.4 available only with the 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843.
2. VOB and VOW3 pins; Option 1 not available.
3. Each pin can be configured to a High (S) or Low (R) state after power-on-reset. The required state of each pin is therefore specified by R or S.

10. ON SCREEN DISPLAY

10.1 Features

- Display format: 2 rows x 16 characters
- Software controlled vertical and horizontal display position
- 64 different characters in ROM - mask programmable
- Black box background
- Four programmable display character sizes
- Four programmable character dot matrix sizes: 6 x 9, 8 x 9, 6 x 13 or 8 x 13
- Half-dot rounding - for whole screen
- 4 from 7 colours possible on screen
- LC oscillator for on screen display function with the 84C441, 84C444, 84C641, 84C644, 84C841 and 84C844.
- RC oscillator for on screen display function with the 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843.

HORIZONTAL DISPLAY POSITION CONTROL

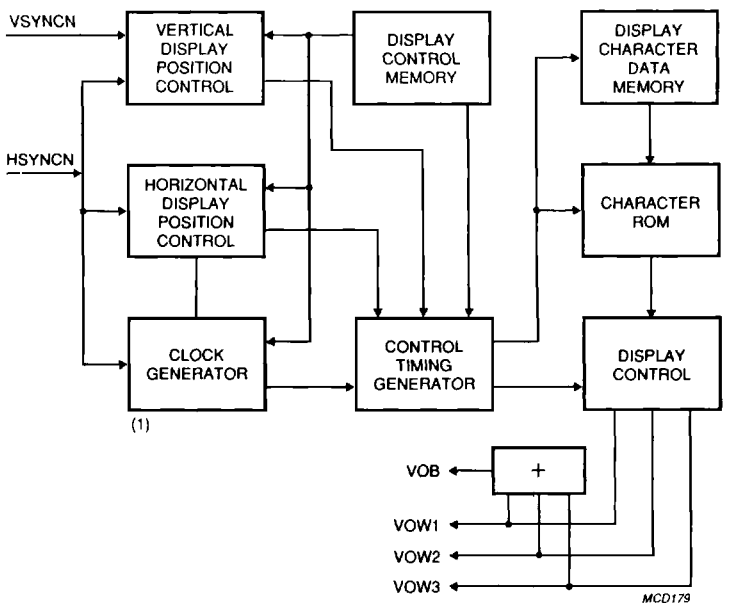
The horizontal position counter is incremented every OSD cycle after the programmed level of HSYNCN occurs at the HSYNCN pin. The counter is reset when the opposite polarity of the HSYNCN pulse is reached.

VERTICAL DISPLAY POSITION CONTROL

The vertical position counter is incremented every HSYNCN cycle and is reset by the VSYNCN signal.

CLOCK GENERATOR

The clock generator consists of an LC oscillator; the external LC network being connected across pins 28 and 29, see Fig.20. (The 84C440, 84C443, 84C640, 84C643, 84C840 and 84C843 use an RC oscillator connected between pin 28 and V_{SS}, see Fig.19). The OSD oscillator must be externally adjusted to the desired frequency (decreasing the OSD frequency gives broader characters). The oscillator is triggered on the trailing edge of HSYNC when the OSD logic is enabled and stops on the following leading edge of HSYNC.



(1) See Figs 19 and 20 for connection of external components.

Fig.18 OSD block diagram.

10.2 Display data registers

The display data registers consists of a group of 32 derivative registers located at addresses 20H to 3FH inclusive. The 16 registers located in memory at addresses 20H to 2FH contain display data for the first line. The remaining 16 registers located in memory at addresses 30H to 3FH, contain display data for the second line. At power-up the contents of the display data registers are undefined. The format of each Display data register is shown in Fig.21.

CC1 and CC0 - COLOUR CODE

The state of these two bits enable individual characters to be displayed in one of four colours.

MD0 to MD5 - CHARACTER CODE

The character set is stored in ROM and consists of 64 different characters. The selection of each character is dependent on the state of the 6 bits, MD0 to MD5.

10.3 Display control registers

The display control registers consists of a group of 6 derivative registers located at addresses 40H to 45H inclusive. (See Table 7 Display control registers). Each register may be read from or written to. After a reset operation the contents of the display control registers are zero.

Derivative register OSDCA

This register resides at address 40H.

HLVL - HORIZONTAL SYNCHRONOUS SIGNAL LEVEL

This bit selects the active level of the HSYNCN input signal. When HLVL is a logic 1, HSYNCN is active HIGH. When HLVL is a logic 0, HSYNCN is active LOW. See Fig.23.

VLVL - VERTICAL SYNCHRONOUS SIGNAL LEVEL

This bit selects the active level of the VSYNCN input signal. When VLVL is a logic 1, VSYNCN is active HIGH. When VLVL is a logic 0, VSYNCN is active LOW. See Fig.23.

STBY - STANDBY

This bit is used to enable or disable the OSD facility. If the STBY bit is a logic 1, the OSD oscillator is disabled. If the STBY bit is a logic 0, the OSD oscillator is enabled and the OSD facility is available. Before the oscillation frequency can be adjusted HSYNCN must be HIGH (if HLVL = 1). Oscillation stops by setting the HSYNCN pin LOW when HLVL = 1.

ROUND - CHARACTER ROUNDING CONTROL

The rounding function generates half dots where the corners of two dots meet. See Figs 24 and 25. The rounding function also works with multiple cell characters. When the Round bit is a logic 1, the rounding function is selected. When the Round bit is a logic 0, the rounding function is disabled.

RBLK - RASTER BLANKING CONTROL

When the RBLK bit is a logic 1, the VOB output is driven high to display the OSD characters on a blank screen. When the RBLK bit is a logic 0, the VOB output returns to its normal output state on the trailing edge of VSYNCN. See Fig.26.

CC34, CC24 and CC14 - CHARACTER COLOUR BITS

These bits are used for colour selection purposes. See Tables 9 to 14.

Table 7 Display control registers

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
40H	OSDCA	CC34	CC24	CC14	RBLK	ROUND	STBY	VLVL	HLVL
41H	LINE 0A	SZ01	SZ00	VP05	VP04	VP03	VP02	VP01	VP00
42H	LINE 0B	BLK0	VB0	HP05	HP04	HP03	HP02	HP01	HP00
43H	OSDCB	CDTW	CDTH	CC33	CC23	CC32	CC12	CC21	CC11
44H	LINE 1A	SZ11	SZ10	VP15	VP14	VP13	VP12	VP11	VP10
45H	LINE 1B	BLK1	VB1	HP15	HP14	HP13	HP12	HP11	HP10

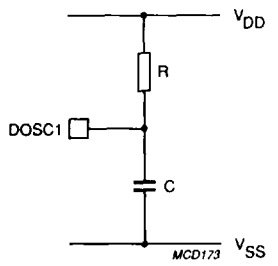


Fig.19 RC oscillator (84C440; 84C443; 84C640; 84C643; 84C840 and 84C843).

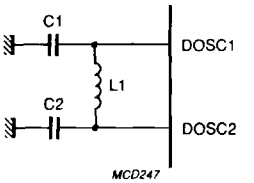


Fig.20 LC oscillator (84C441; 84C444; 84C641; 84C644; 84C841 and 84C844).

CC1 (MSB)	CC0	MD5	MD4	MD3	MD2	MD1	MD0 (LSB)

Fig.21 Display data register.

CC34 (MSB)	CC24	CC14	RBLK	ROUND	STBY	VLVL	HLVL (LSB)

Fig.22 Derivative register OSDCA.

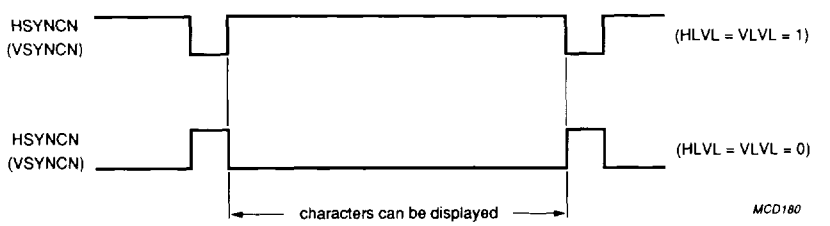


Fig.23 VSYNCN and HSYNCN active level.

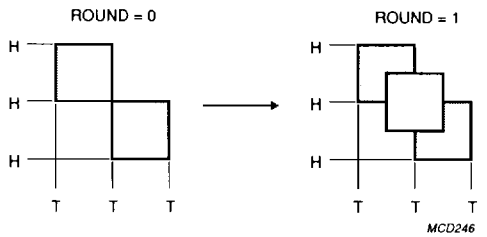


Fig.24 Rounding function.

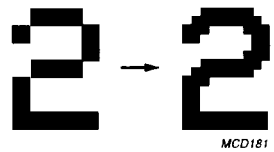


Fig.25 Rounding effect.

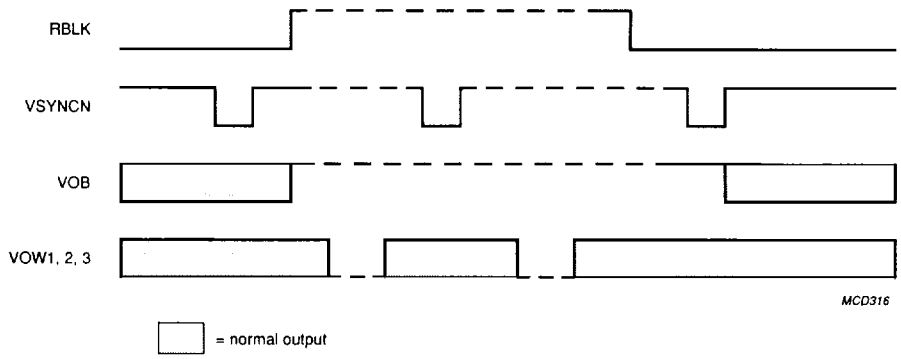


Fig.26 Raster blanking timing RLBK.

Derivative register LINE 0A

This register resides at address 41H. Its contents determine the character size and vertical position of the first row of display.

SZ00 and SZ01 - CHARACTER SIZE

The state of these two bits enable one of four possible character sizes to be selected for Row 0. Character sizes include background.

VP00 to VP05 - VERTICAL POSITION CONTROL

The vertical position of the first display row is selected by the state of the 6 bits, VP00 to VP05. The line number of the vertical start position for Row 0 is 4 x (decimal value of bits VP00 to VP05).

Row 0 and Row 1 must not overlap each other and therefore VP1 must be greater than or equal to (VP0 + H0), see Fig. 28. H0 is the character height of the characters in Row 0 and is a function of the number of dots per character and the state of the Size control bits SZ00 and SZ01. The four possible character heights are shown in Table 8.

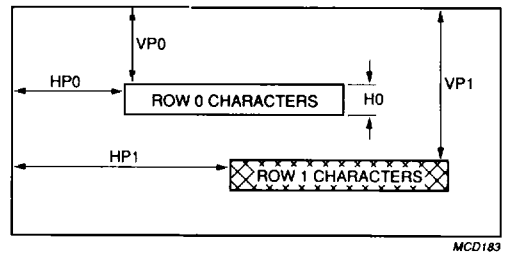


Fig.28 Display position.

SZ01 (MSB)	SZ00	VP05	VP04	VP03	VP02	VP01	VP00 (LSB)

Fig.27 Derivative register LINE 0A.

Table 8 OSD character sizes

DATA		CHARACTER SIZE				DOT MATRIX POINT	
SZx1	SZx0	VERTICAL		HORIZONTAL		VERTICAL	HORIZONTAL
		9D	13D	6D	8D		
0	0	18H	26H	12T	16T	2H	2T
0	1	36H	52H	24T	32T	4H	4T
1	0	54H	78H	36T	48T	6H	6T
1	1	72H	104H	48T	64T	8H	8T

Note

H denotes one horizontal line, T denotes one OSDC clock period and D denotes dots per character width/height.

Derivative register LINE 0B

The Derivative register LINE 0B resides at address 42H. Its contents determine the horizontal position of the first row of the display and whether the background and blanking functions are selected.

BLK0 - BLANKING

This bit enables or disables the character display. When BLK0 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are disabled; consequently no characters are displayed. When BLK0 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are enabled and characters are displayed.

VB0 - BACKGROUND

The state of the VB0 bit determines whether the background display is selected or not. If the VB0 bit is set to a logic 1, the characters in this line are displayed with background. If the VB0 bit is logic 0 the background is disabled and only the character is displayed.

HP01 to HP05 - HORIZONTAL POSITION CONTROL

These 6 bits determine the start position of the first display row. The horizontal position control is only active during OSDC clock cycles. (See Fig. 28).

The horizontal start position (HP) of Row 0 may be calculated using:

HP = 4 x (decimal value of bits HP00 to HP05) + 5 x (OSD C periods)

The decimal value of bits HP00 to HP05 must be greater than 10. Therefore, HP ≥ 45 (OSDC clock pulses).

Fig.30 Background versus no background.

BLK0 (MSB)	VB0	HP05	HP04	HP03	HP02	HP01	HP00 (LSB)

Fig.29 Derivative register LINE 0B.

Derivative register OSDCB

The OSDCB register resides at address 43H. The contents of this register permit the size of the dot matrix grid to be selected and also enable four colours from a possible seven to be chosen for the display.

CDTW - CHARACTER DOT WIDTH CONTROL

The state of this bit determines the dot width of the character. When the CDTW bit is set to a logic 1, the character width is 6 dots. When the CDTW bit is set to a logic 0, the character width is 8 dots.

CDTH - CHARACTER DOT HEIGHT CONTROL

The state of this bit determines the dot height of the character. When the CDTH bit is set to a logic 1, the character height is 13 dots. When the CDTH bit is set to a logic 0, the character height is 9 dots.

CCXX - COLOUR CONTROL BITS

In every VSYNCN cycle one screen can select any 4 colours from 7 and in addition a blank or black screen. Colour selection is achieved using bits CC34, CC24 and CC14 in the OSDCA register; bits CC33, CC23, CC32, CC12, CC21, and CC11 in the OSDCB register and bits CC1 and CC0 from the display data registers. (See Table 9). Bits CC1X control VOW1 (red), bits CC2X control VOW2 (green) and bits CC3X control VOW3 (blue). Combinations of CCV2 and CCV3 control VOW1, VOW2 and VOW3.

In this way every combination of four colours can be made (black and white can not be displayed at the same time). Table 11 shows the possible combinations. The user may choose one colour out of each block. For example see Table 10.

Derivative register LINE 1A

This register resides at address 44H. Its contents determine the character size and vertical position of the second row of display.

SZ10 and SZ11 - CHARACTER SIZE

The state of these two bits enable one of four possible character sizes to be selected for Row 1. Character sizes include background. See Table 8 for character size selection.

VP10 to VP15 - VERTICAL POSITION CONTROL

The vertical position of the second display row is selected by the state of the 6 bits, VP10 to VP15. The line number of the vertical start position for Row 1 is 4 x (decimal value of bits VP15 to VP10).

Row 0 and Row 1 must not overlap each other and therefore VP1 must be greater than or equal to (VP0 + H0), see Fig. 28. H0 is the character height of the characters in Row 0 and is a function of the number of dots per character and the state of the size control bits SZ00 and SZ01. The four possible character heights are shown in Table 8.

CDTW (MSB)	CDTH	CC33	CC23	CC32	CC12	CC21	CC11 (LSB)

Fig.31 Derivative register OSDCB

Table 9 Character colour control

CC1	CC0	VOW1	VOW2	VOW3
0	0	CC11	CC21	$\overline{CC11 + CC21}$
0	1	CC12	$\overline{CC12 + CC32}$	CC32
1	0	$\overline{CC23 + CC33}$	CC23	CC33
1	1	CC14	CC24	CC34

Table 10 Example of selecting colours by programming CCxx

CHARACTER DATA	CHARACTER OUTPUT PINS		
VOW1 (Red)	VOW2 (Green)	VOW3 (Blue)	COLOUR
0	0	0	black
0	0	1	blue (2)
0	1	0	green (3)
0	1	1	cyan
1	0	0	red
1	0	1	magenta (4)
1	1	0	yellow (1)
1	1	1	white

Notes

If VOW1 = Red, VOW2 = Green, VOW3 = Blue, then using the bit combination CC11:1, CC21:1, CC12:0, CC32:1, CC23:1, CC33:0, CC14:1, CC24:0, CC34:1 the following colours may be selected.

1. Yellow; (CC1, CC0 = 00)
2. Blue; (CC1, CC0 = 01)
3. Green; (CC1, CC0 = 10)
4. Magenta; (CC1, CC0 = 11)

SZ11 (MSB)	SZ10	VP15	VP14	VP13	VP12	VP11	VP10 (LSB)

Fig.32 Derivative register LINE 1A.

Derivative register LINE 1B

The Derivative register LINE 1B resides at address 45H. Its contents determine the horizontal position of the second line of the display (Line 1) and whether the background and blanking functions are selected.

BLK1 - BLANKING

This bit enables or disables the character display. When BLK1 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are disabled; consequently no characters are displayed. When BLK1 is a logic 1, the outputs VOW1, VOW2, VOW3 and VOB are enabled and characters are displayed.

VB1 - BACKGROUND

The state of the VB1 bit determines whether the background display is selected or not. If the VB1 bit is set to a logic 1, the characters in this line are displayed with background. If the VB1 bit is logic 0, the background is disabled and only the character is displayed. The visual effect of background versus no background is shown in Fig.30.

HP11 to HP15 - HORIZONTAL POSITION CONTROL

These 6 bits determine the start position of the second display line (Line 1). The horizontal position control is only active during OSDC clock cycles. (See Fig. 28). The horizontal start position (HP) of Line 1 may be calculated using:

HP = 4 x (decimal value of bits HP10 to HP15)) + 5 x (OSD C periods)

The decimal value of bits HP10 to HP15 must be greater than 10. Therefore, HP ≥ 45 (OSDC clock pulses)

Character ROM

Character ROM contains the dot character fonts. 13 x 8 dots are reserved for each character, regardless of the dot matrix size actually selected. The dot matrix grid is shown in Fig.34.

The document 'How to prepare the character ROM code for the OSD part of the PCA84C640' is available on request.

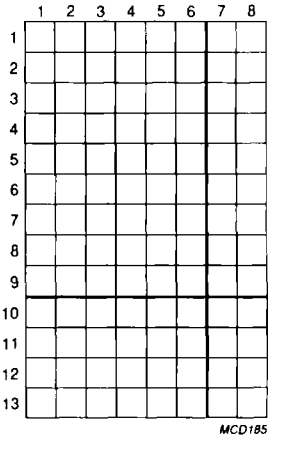


Fig.34 Character ROM.

BLK1 (MSB)	VB1	HP15	HP14	HP13	HP12	HP11	HP10 (LSB)

Fig.33 Derivative register LINE 1B.

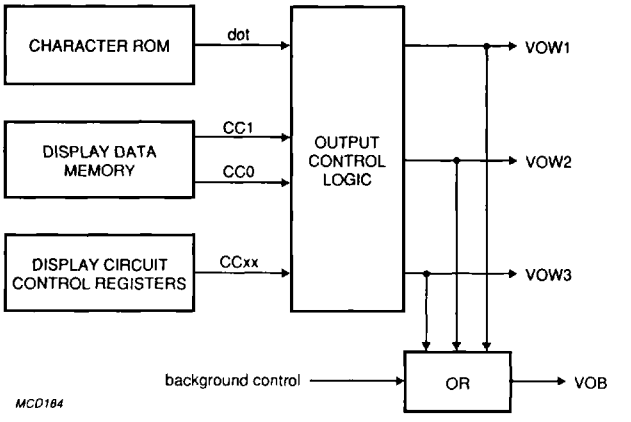


Fig.35 Colour control.

Table 11 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	CC11	CC21	$\overline{CC11+CC21}$	
0	0	0	0	1	blue
0	0	0	1	0	green
0	0	1	0	0	red
0	0	1	1	0	yellow

Table 12 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	CC12	$\overline{CC12+CC32}$	CC32	
0	1	0	0	1	blue
0	1	0	1	0	green
0	1	1	0	0	red
0	1	1	0	1	magenta

Table 13 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	$\overline{CC23+CC33}$	CC23	CC33	
1	0	0	0	1	blue
1	0	0	1	0	green
1	0	0	1	1	cyan
1	0	1	0	0	red

Table 14 Possible colour combinations

CHARACTER DATA		VOW1	VOW2	VOW3	COLOUR
CC1	CC0	CC14	CC24	CC34	
1	1	0	0	0	black
1	1	0	0	1	blue
1	1	0	1	0	green
1	1	0	1	1	cyan
1	1	1	0	0	red
1	1	1	0	1	magenta
1	1	1	1	0	yellow
1	1	1	1	1	white

11. EMULATION MODE

The emulation mode configuration is shown in Fig.36.

In the emulation mode configuration the PCA84C640's CPU is disabled and only its derivative logic is active. The device is controlled by the PCF84C00 bond-out chip. The PCA84C640's two derivative ports act as additional ports for the PCF84C00. The interaction between the two devices is as follows:

1. During the first machine cycle the PCF84C00 fetches an instruction from EPROM and then decodes that instruction.
2. During the second machine cycle the PCF84C00 executes the decoded instruction. If the instruction is related to the derivative ports then DXALE, DXRDN and/or DXWRN become active and the PCA84C640 operates as a peripheral of the PCF84C00.
3. Depending on the type of instruction executed during the second machine cycle the following data transfer happens:
   (a) During TS1 data from the EPROM is available on P0.0 to P0.7 which is then available on IB0.0 of the PCF84C00.
   (b) During TS4 data from the PCA84C640 can be transferred to the PCF84C00.
   (c) During TS6 data from the PCF84C00 can be transferred to the PCA84C640.

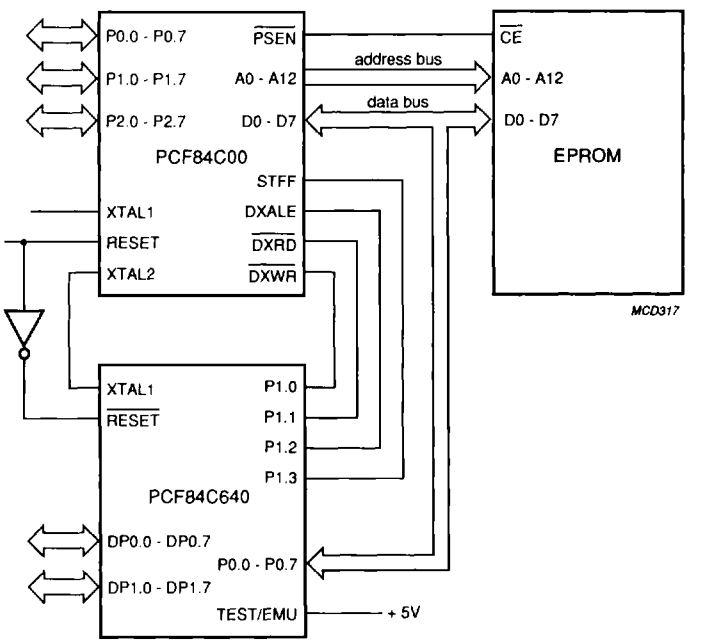


Fig.36 Emulation mode configuration.

12. DIFFERENCES BETWEEN THE 84C44X, 84C64X AND 84C84X

Table 15 Differences between the 84C440; 84C441; 84C443 and 84C444

FEATURE	84C440	84C441	84C443	84C444
ROM	4 Kbytes	4 Kbytes	4 Kbytes	4 Kbytes
RAM	128 bytes	128 bytes	128 bytes	128 bytes
OSD oscillator	RC	LC	RC	LC
general purpose I/O lines	18	17	18	17
pin assignment	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2
Register DP1 - pin; bit DP1.4	available	not available	available	not available
Register DP1 - latch; bit DP1.4	available	not available	available	not available
port line DP14	available	not available	available	not available
I²C interface	available	available	not available	not available

Table 16 Differences between the 84C640; 84C641; 84C643 and 84C644

FEATURE	84C640	84C641	84C643	84C644
ROM	6 Kbytes	6 Kbytes	6 Kbytes	6 Kbytes
RAM	128 bytes	128 bytes	128 bytes	128 bytes
OSD oscillator	RC	LC	RC	LC
general purpose I/O lines	18	17	18	17
pin assignment	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2
Register DP1 - pin; bit DP1.4	available	not available	available	not available
Register DP1 - latch; bit DP1.4	available	not available	available	not available
port line DP14	available	not available	available	not available
I²C interface	available	available	not available	not available

Table 17 Differences between the 84C840; 84C841; 84C843 and 84C844

FEATURE	84C840	84C841	84C843	84C844
ROM	8 Kbytes	8 Kbytes	8 Kbytes	8 Kbytes
RAM	192 bytes	192 bytes	192 bytes	192 bytes
OSD oscillator	RC	LC	RC	LC
general purpose I/O lines	18	17	18	17
pin assignment	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2	pin 34 = DP1.4 pin 29 = T1	pin 34 = T1 pin 29 = DOSC2
Register DP1 - pin; bit DP1.4	available	not available	available	not available
Register DP1 - latch; bit DP1.4	available	not available	available	not available
port line DP14	available	not available	available	not available
I²C interface	available	available	not available	not available

13. REGISTER MAP

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER
00H	DP0.7 (x) R	DP0.6 (x) R	DP0.5 (x) R	DP0.4 (x) R	DP0.3 (x) R	DP0.2 (x) R	DP0.1 (x) R	DP0.0 (x) R	DP0R (pin)
01H	DP1.7 (x) R	DP1.6 (x) R	DP1.5 (x) R	DP1.4[1] (x) R	DP1.3 (x) R	DP1.2 (x) R	DP1.1 (x) R	DP1.0 (x) R	DP1R (pin)
02H	DP0.7 (1) R/W	DP0.6 (1) R/W	DP0.5 (1) R/W	DP0.4 (1) R/W	DP0.3 (1) R/W	DP0.2 (1) R/W	DP0.1 (1) R/W	DP0.0 (1) R/W	DP0R (latch)
03H	DP1.7 (1) R/W	DP1.6 (0) R/W	DP1.5 (0) R/W	DP1.4[1] (1) R/W	DP1.3 (1) R/W	DP1.2 (1) R/W	DP1.1 (1) R/W	DP1.0 (1) R/W	DP1R (latch)
10H	-	-	PWM15 (0) R/W	PWM14 (0) R/W	PWM13 (0) R/W	PWM12 (0) R/W	PWM11 (0) R/W	PWM10 (0) R/W	PWM1
11H	-	-	PWM22 (0) R/W	PWM24 (0) R/W	PWM23 (0) R/W	PWM22 (0) R/W	PWM21 (0) R/W	PWM20 (0) R/W	PWM2
12H	-	-	PWM35 (0) R/W	PWM34 (0) R/W	PWM33 (0) R/W	PWM32 (0) R/W	PWM31 (0) R/W	PWM30 (0) R/W	PWM3
13H	-	-	PWM45 (0) R/W	PWM44 (0) R/W	PWM43 (0) R/W	PWM42 (0) R/W	PWM41 (0) R/W	PWM40 (0) R/W	PWM4
14H	-	-	PWM55 (0) R/W	PWM54 (0) R/W	PWM53 (0) R/W	PWM52 (0) R/W	PWM51 (0) R/W	PWM50 (0) R/W	PWM5
15H	-	VST06 (0) R/W	VST05 (0) R/W	VST04 (0) R/W	VST03 (0) R/W	VST02 (00 R/W	VST01 (0) R/W	VST00 (0) R/W	VSTL
16H	-	VST13 (0) R/W	VST12 (0) R/W	VST11 (0) R/W	VST10 (0) R/W	VST09 (0) R/W	VST08 (0) R/W	VST07 (0) R/W	VSTH
17H	-	-	-	-	-	AFC2 (0) R/W	AFC1 (0) R/W	AFC0 (0) R/W	AFCO
18H	-	-	-	-	-	-	-	AFCC (x) R	AFCC
19H	SCLE (0) R/W	SDAE (0) R/W	PWM5E (0) R/W	PWM4E (0) R/W	PWM3E (0) R/W	PWM2E (0) R/W	PWM1E (0) R/W	TDACE (0) R/W	DP0E/PWME
1AH	-	-	-	AFCE (0) R/W	P14LVL (0) R/W	P6LVL (0) R/W	VOW2E (0) R/W	VOW1E (0) R/W	DP1E/ PWMLVL
20H-3FH	CC1 (x) W	CC0 (x) W	MD5 (x) W	MD4 (x) W	MD3 (x) W	MD2 (x) W	MD1 (x) W	MD0 (x) W	DATA DISPLAY MEMORY

ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER
40H	CC34 (0) R/W	CC24 (0) R/W	CC14 (0) R/W	RBLK (0) R/W	ROUND (0) R/W	STBY (1) R/W	VLVL (0) R/W	HLVL 0 R/W	OSDCA
41H	SZ01 (0) R/W	SZ00 (0) R/W	VP05 (0) R/W	VP04 (0) R/W	VP03 (0) R/W	VP02 (0) R/W	VP01 (0) R/W	VP00 (0) R/W	LINE 0A
42H	BLK0 (0) R/W	VB0 (0) R/W	HP05 (0) R/W	HP04 (0) R/W	HP03 (0) R/W	HP02 (1) R/W	HP01 (0) R/W	HP00 (0) R/W	LINE 0B
43H	CDTW (0) R/W	CDTH (0) R/W	CC33 (0) R/W	CC23 (0) R/W	CC32 (0) R/W	CC12 (1) R/W	CC21 (0) R/W	CCV11 (0) R/W	OSDCB
44H	SZ11 (0) R/W	SZ10 (0) R/W	VP15 (0) R/W	VP14 (0) R/W	VP13 (0) R/W	VP12 (1) R/W	VP11 (0) R/W	VP10 (0) R/W	LINE 1A
45H	BKL1 (0) R/W	VB1 (0) R/W	HP15 (0) R/W	HP14 (0) R/W	HP13 (0) R/W	HP12 (1) R/W	HP11 (0) R/W	HP10 (0) R/W	LINE 1B

Notes

1. These bits are not available in the 84C441, 84C444, 84C641, 84C644, 84C841 and the 84C844.
2. The number within parentheses denotes the initial state; 'x' denotes don't care.

14. LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.3	+7.0	V
V_I	all input voltages	−0.3	V_{DD} + 0.3	V
$-I_{OH}$	maximum source current - all port lines	-	10	mA
$-I_{OL}$	maximum sink current - all port lines	-	30	mA
P_{tot}	total power dissipation	-	900	mW
T_{stg}	storage temperature range	−55	+ 125	°C
T_{amb}	operating ambient temperature range - all devices	−20	+ 70	°C

15. DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; all voltages with respect to V_{SS} unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating voltage		4.5	5.0	5.5	V
I_{DD}	operating current	f_{OSDCRC} = f_{OSDCLC} = f_{XTAL}; see note 1				
		V_{DD} = 5 V; f_{XTAL} = 10 MHz	-	5	10	mA
		V_{DD} = 5 V; f_{XTAL} = 6 MHz	-	3.5	8	mA
I_{DD}	operating current	f_{OSDCRC} = f_{OSDCLC} = STOP; see note 1				
		V_{DD} = 5 V; f_{XTAL} = 10 MHz	-	3	7	mA
		V_{DD} = 5 V; f_{XTAL} = 6 MHz	-	1.5	3.5	mA
I_{DD}	Idle mode current	V_{DD} = 5 V; f_{XTAL} = 10 MHz	-	1.3	3	mA
		V_{DD} = 5 V; f_{XTAL} = 6 MHz; see note 1	-	0.8	1.5	mA
I_{DD}	Stop mode current	V_{DD} = 5.5 V; see notes 1 and 2	-	5	10	µA
Inputs						
V_{IL}	input LOW voltage; Ports P0; P1; DP0; DP1; HSYNCN; VSYNCN		0	-	0.3V_{DD}	V
V_{IH}	input HIGH voltage; Ports P0; P1; DP0; DP1; HSYNCN; VSYNCN		0.7V_{DD}	-	V_{DD}	V
I_{IH}	input current RESET	V_{in} = 0.5 V	20	-	-	µA
V_{AI}	input voltage; DP1.7; AFC1		V_{SS}	-	V_{DD}	V
V_{AE}	conversion error range (AFC)		-	-	± 1/2	LSB
$\pm I_{LI}$	input leakage current; Ports P0; P1; DP0; DP1	V_{SS}< V_I<V_{DD}	-	-	10	µA
$\pm I_{LI}$	input leakage current INTN/T0; T1	V_{SS}< V_I<V_{DD}	0.01	0.20	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
I_{OL}	output LOW sink current; Port P0	V_{DD} = 5 V ±10%; V_O = 1.2 V	10	-	-	mA
I_{OL}	output LOW sink current; Ports P1; DP0; DP1; VOB; VOW3	V_{DD} = 5 V ±10%; V_O = 0.4 V	1.2	3	-	mA
I_{OH}	pull-up output HIGH source current; Ports P0; P1; DP0; DP1	V_{DD} = 5 V ± 10%; V_O = 0.7V_{DD}	40	-	-	µA
I_{OH}	pull-up output HIGH source current; Ports P0; P1; DP0; DP1	V_{DD} = 5 V ± 10%; V_O = V_{SS}	-	-	400	µA
I_{OH}	push-pull output HIGH source current; Ports P0; P1; DP0; DP1; VOB; VOW3	V_{DD} = 5 V ± 10%; V_O = V_{DD}–0.4V	1.2	3	-	mA

Notes

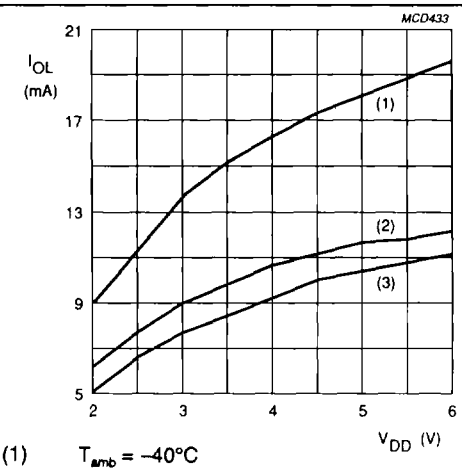
1. V_{IL} = V_{SS}; V_{IH} = V_{DD}; all outputs and sense input lines unloaded. All open drain ports connected to V_{SS}.
2. Crystal is connected between XTAL1 and XTAL2; T1 = V_{SS}; INTN/T0 = V_{DD}.

16. AC CHARACTERISTICS

16.1 Oscillator requirements

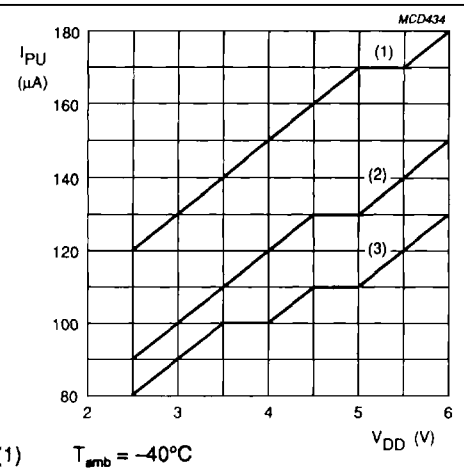
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{XTAL}	crystal frequency	V_{DD} = 5 V ±10%	1	10	MHz
f_{DOSC}	DOS oscillator frequency	V_{DD} = 5 V ±10%	-	10	MHz

16.2 Characteristic curves



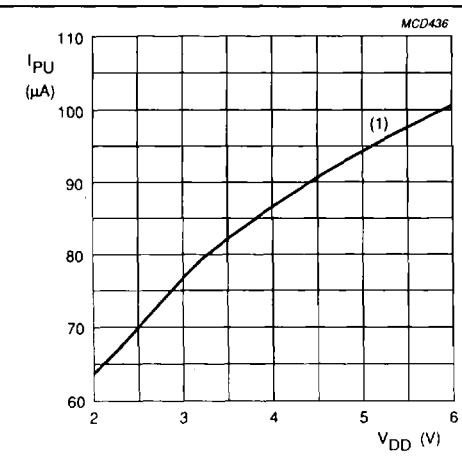
(1) T_{amb} = −40°C
(2) T_{amb} = 25°C
(3) T_{amb} = 85°C

Fig.37 Typical output sink current as a function of supply voltage; V_O = 0.4 V.



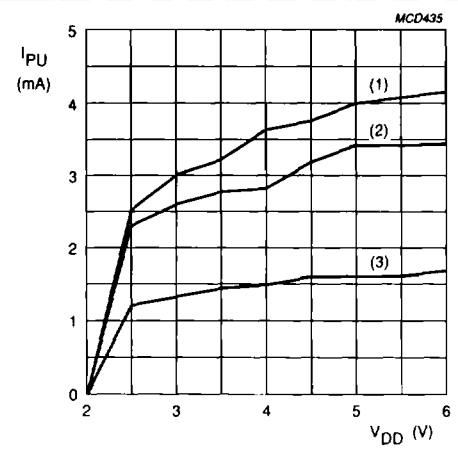
(1) T_{amb} = −40°C
(2) T_{amb} = 25°C
(3) T_{amb} = 85°C

Fig.38 Typical pull-up current as a function of supply voltage; V_O = 0 V.



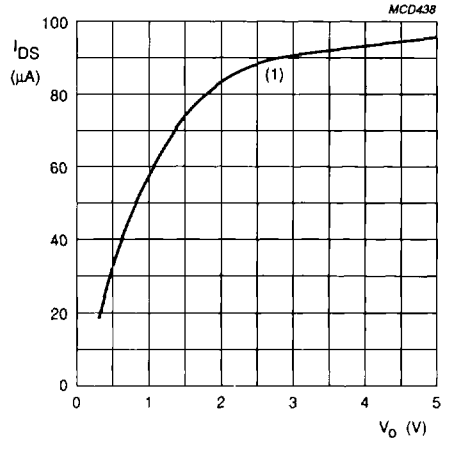
(1) T_{amb} = 25°C

Fig.39 Typical pull-up current as a function of supply voltage; $V_O = 0.7V_{DD}$.



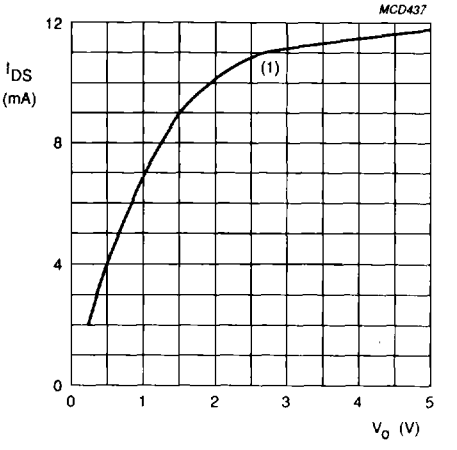
(1) T_{amb} = −40°C
(2) T_{amb} = 25°C
(3) T_{amb} = 85°C

Fig.40 Typical booster current as a function of supply voltage; $V_O = V_{DD} - 0.4$ V.



(1) T_{amb} = 25°C

Fig.41 Typical open drain sink capability as a function of V_O; Port 0



(1) T_{amb} = 25°C

Fig.42 Typical open drain sink capability as a function of V_O; DP0.0 to DP0.7, DP1.5 to DP1.7 and P1.0 to P1.4

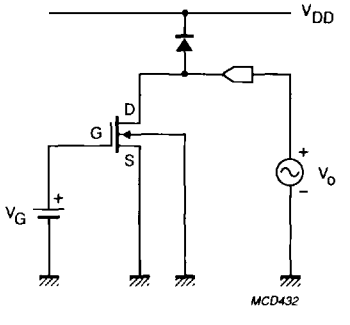
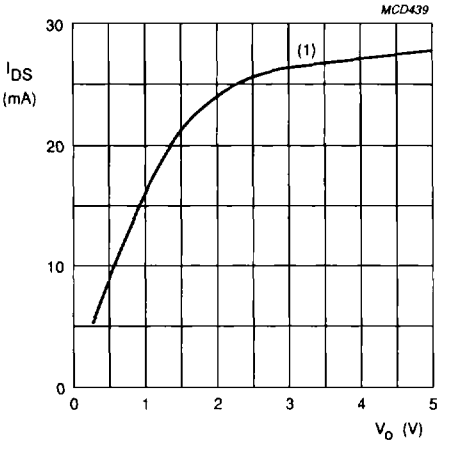


Fig.43 Open drain test circuit; DP0.0 to DP0.7, DP1.5 to DP1.7 and P1.0 to P1.4



(1) T_{amb} = 25°C

Fig.44 Typical open drain sink capability as a function of V_O; VOW3 and VOB0

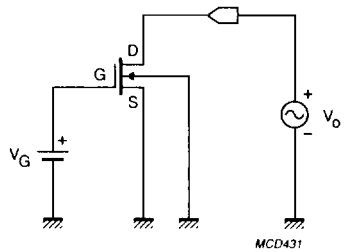


Fig.45 Open drain test circuit; VOW3 and VOB

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.