SAA3027

Infrared Remote Control Transmitter (RC-5)

Product Specification

DESCRIPTION

The SAA3027 is intended for a general purpose (RC-5) infrared remote control system. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

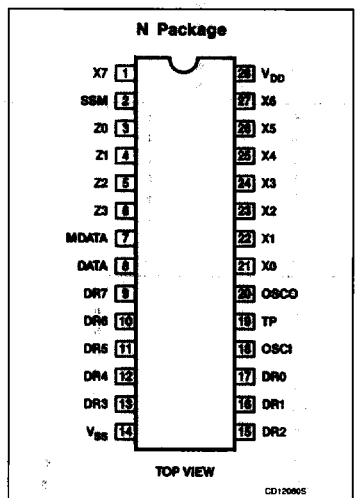
FEATURES

- **Transmitter for 32 × 64 commands**
- **One transmitter controls 32 systems**
- **Very low current consumption**
- **For infrared transmission link**
- **Transmission by biphase technique**
- **Short transmission times; speed-up of system reaction time**
- **LC oscillator; no crystal required**
- **Input protection**
- **Test mode facility**

APPLICATION

- **Remote control systems**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	X7	Keyboard command inputs with P-channel pull-up transistors
21	X0	
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
2	SSM	System mode selection input
3	Z0	Keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
7	MDATA	Remote signal outputs (3-state outputs)
8	DATA	
9	DR7	Scan driver outputs with open-drain N-channel transistors
10	DR6	
11	DR5	
12	DR4	
13	DR3	
15	DR2	
16	DR1	
17	DR0	
14	V_{SS}	Negative supply (ground)
18	OSCI	Oscillator input
19	TP	Test pin
20	OSCO	Oscillator output
28	V_{DD}	Positive supply

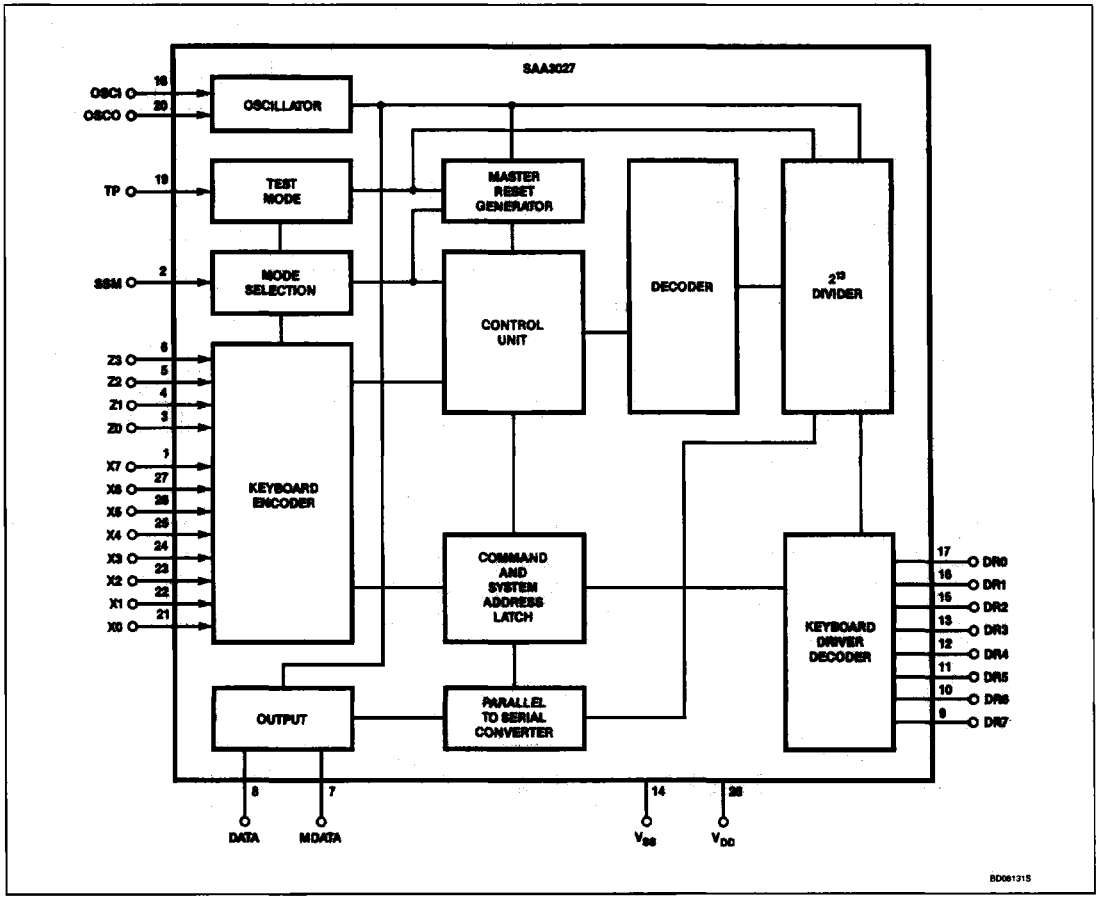
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +85°C	SAA3027PN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range with respect to V_{SS}	−0.5 to +15	V
V_I	Input voltage range	−0.5 to (V_{DD} + 0.5)	V
$\pm I_I$	Input current	10	mA
V_O	Output voltage range	−0.5 to (V_{DD} + 0.5)	V
$\pm I_O$	Output current	10	mA
P_O	Power dissipation output OSCO	50	mW
P_O	Power dissipation per output (all other outputs)	100	mW
P_{TOT}	Total power dissipation per package	200	mW
T_A	Operating ambient temperature range	−25 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM

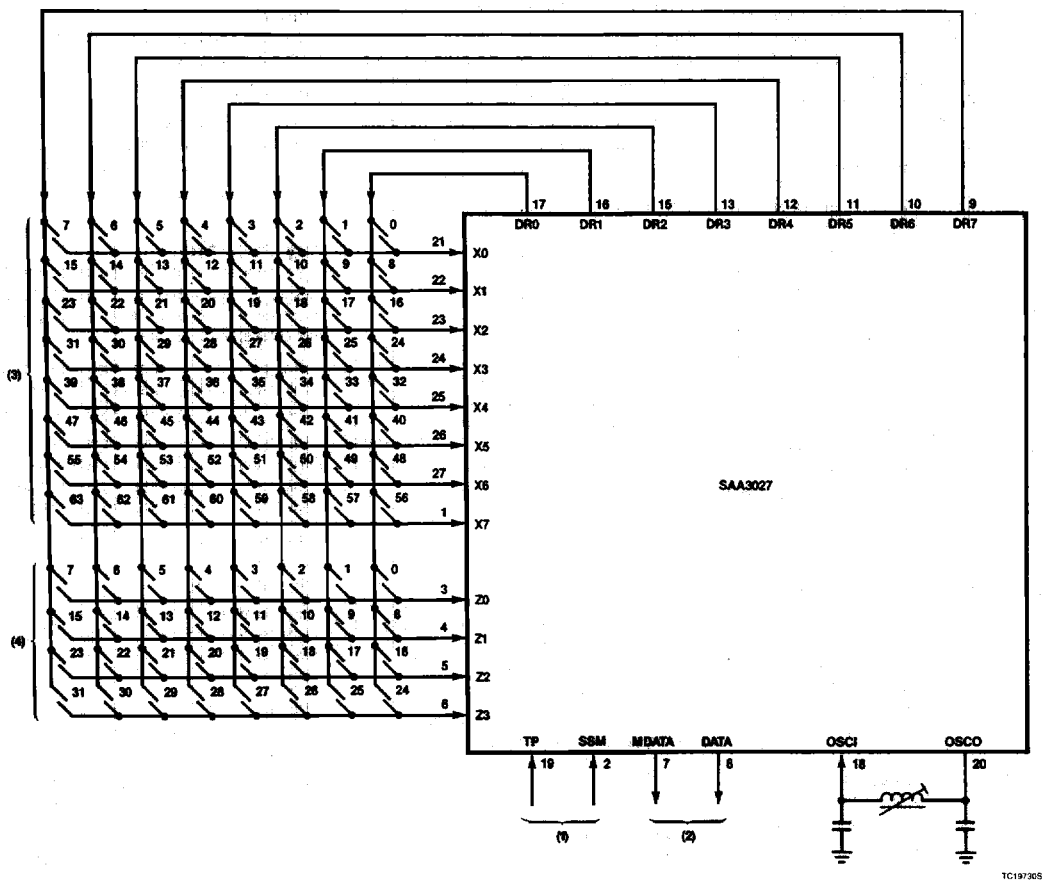


DC AND AC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; T_A = −25°C to 85°C, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.75		12.6	V
	Supply current at I_O = 0mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs;					
I_{DD}	T_A = 25°C	12.6			10	µA
Inputs Keyboard inputs X and Z with P-channel pull-up transistors						
$-I_I$	Input current (each input) at V_I = 0V; TP = SSM = LOW	4.75 to 12.6	10		300	µA
V_{IH}	Input voltage HIGH	4.75 to 12.6	0.7 × V_{DD}		V_{DD}	V
V_{IL}	Input voltage LOW	4.75 to 12.6	0		0.3 × V_{DD}	V
	Input leakage current at T_A = 25°C; TP = HIGH;					
I_{IR}	V_I = 12.6V	12.6			1	µA
$-I_{IR}$	V_I = 0V	12.6			1	µA
SSM, TP and OSCI inputs						
V_{IH}	Input voltage HIGH	4.75 to 12.6	0.7 × V_{DD}		V_{DD}	V
V_{IL}	Input voltage LOW	4.75 to 12.6	0		0.3 × V_{DD}	V
	Input leakage current at T_A = 25°C;					
I_{IR}	V_I = 12.6V	12.6			1	µA
$-I_{IR}$	V_I = 0V	12.6			1	µA
Outputs **DATA, MDATA**						
V_{OH}	Output voltage HIGH at $-I_{OH}$ = 0.8mA	4.75 to 12.6	V_{DD} −0.6			V
V_{OL}	Output voltage LOW at I_{OL} = 0.8mA	4.75 to 12.6			0.4	V
	Output leakage current at:					
I_{OR}	V_O = 12.6V	12.6			10	µA
$-I_{OR}$	V_O = 0V	12.6			20	µA
	T_A = 25°C;					
I_{OR}	V_O = 12.6V	12.6			1	µA
$-I_{OR}$	V_O = 0V	12.6			2	µA
DR0 to DR7 outputs						
V_{OL}	Output voltage LOW at I_{OL} = 0.35mA	4.75 to 12.6			0.4	V
I_{OR}	Output leakage current at V_O = 12.6V	12.6			10	µA
	at V_O = 12.6V;					
I_{OR}	T_A = 25°C	12.6			1	µA
OSCO output						
V_{OH}	Output voltage HIGH at $-I_{OH}$ = 0.2mA; OSCI = V_{SS}	4.75 to 12.6	V_{DD} − 0.6			V
V_{OL}	Output voltage LOW at $-I_{OL}$ = 0.45mA; OSCI = V_{DD}	4.75 to 12.6			0.5	V
Oscillator						
f_{OSCI}	Maximum oscillator frequency at C_L = 40pF (Figures 4 and 5)	4.75	75	72		kHz
f_{OSCI}		6	120	72		kHz
f_{OSCI}		12.6	300	72		kHz

Handling

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.



NOTES:
(1) Programming inputs for operating modes, test mode and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 × 8.
(4) Keyboard system code matrix 4 × 8.

Figure 1. Keyboard Interconnection

FUNCTIONAL DESCRIPTION

Combined System Mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches; depending on whether sensing was found in the Z or X-input matrix. After latching a system address number, the device will generate the last command (i.e., all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single System Mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off; those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

OSCI and OSCO are the input/output, respectively, of a two-pin oscillator. The oscillator is formed externally by one inductor and two capacitors and operates at 72kHz (typical).

Key-Release Detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

Outputs

The output DATA carries the generated information according to the format given in Figure 2 and Tables 1 and 2. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Figure 3.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1')
- Control part formed by 1 bit
- System part formed by 5 bits
- Command part formed by 6 bits

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of half the oscillator frequency, so that each bit is presented as a burst of 32 oscillator periods. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation, a scanning procedure is started so that they are switched into the conducting state one after the other.

Reset Action

The circuit will be reset immediately when a key release occurs during:

- Debounce time
- Between two codes

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- The key is released while one of the driver outputs is in the low-ohmic '0' state;
- The key is released before detection of that key;
- There is no wired connection in the Z-DR matrix while SSM is HIGH.

Test Pin

The test pin TP is an input which can be used for testing purposes.

When LOW, the circuit operates normally.

When HIGH, all pull-up transistors are switched off, the control bit is set to zero and the output data is 2^6 times faster than normal.

When Z2 = Z3 = LOW, the counter will be reset to zero.

Key Activities

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 10kΩ

Z2 or Z3 must be connected to V_{DD} to avoid unwanted supply current.

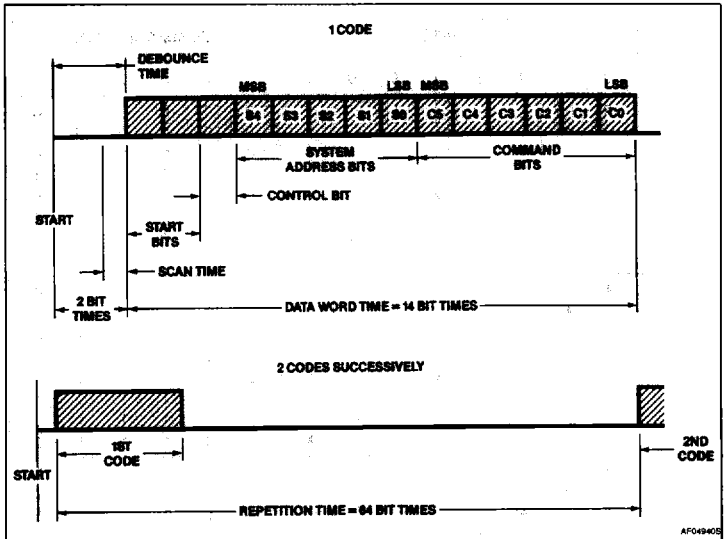
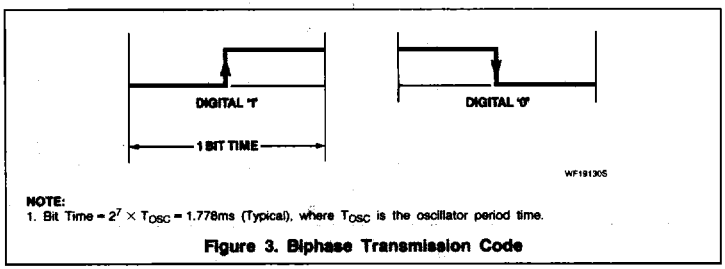


Figure 2. DATA Output Format (RC-5)



NOTE:
1. Bit Time = $2^7 \times T_{OSC}$ = 1.778ms (Typical), where T_{OSC} is the oscillator period time.

Figure 3. Biphase Transmission Code

Table 1. Command Matrix X-DR

CODE NO	X-LINES X								DR-LINES DR								COMMAND BITS C					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

Table 1. Command Matrix X-DR (Continued)

CODE NO	X-LINES X								DR-LINES DR								COMMAND BITS C					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					•				•								1	0	0	0	0	0
33					•					•							1	0	0	0	0	1
34					•						•						1	0	0	0	1	0
35					•							•					1	0	0	0	1	1
36					•								•				1	0	0	1	0	0
37					•									•			1	0	0	1	0	1
38					•										•		1	0	0	1	1	0
39					•											•	1	0	0	1	1	1
40						•			•								1	0	1	0	0	0
41						•				•							1	0	1	0	0	1
42						•					•						1	0	1	0	1	0
43						•						•					1	0	1	0	1	1
44						•							•				1	0	1	1	0	0
45						•								•			1	0	1	1	0	1
46						•									•		1	0	1	1	1	0
47						•										•	1	0	1	1	1	1
48							•		•								1	1	0	0	0	0
49							•			•							1	1	0	0	0	1
50							•				•						1	1	0	0	1	0
51							•					•					1	1	0	0	1	1
52							•						•				1	1	0	1	0	0
53							•							•			1	1	0	1	0	1
54							•								•		1	1	0	1	1	0
55							•									•	1	1	0	1	1	1
56								•	•								1	1	1	0	0	0
57								•		•							1	1	1	0	0	1
58								•			•						1	1	1	0	1	0
59								•				•					1	1	1	0	1	1
60								•					•				1	1	1	1	0	0
61								•						•			1	1	1	1	0	1
62								•							•		1	1	1	1	1	0
63								•								•	1	1	1	1	1	1

Table 2. System Matrix Z-DR

SYSTEM NO	Z-LINES Z				DR-LINES DR								SYSTEM BITS S				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

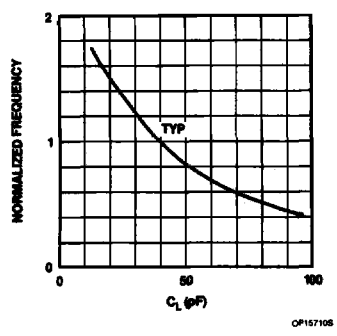


Figure 4. Typical Normalized Input Frequency as a Function of the Load (Keyboard) Capacitance

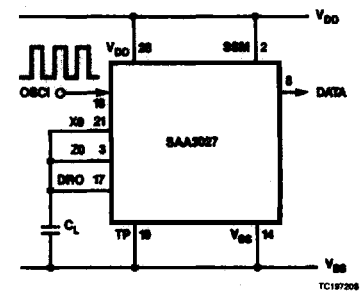


Figure 5. Test Circuit for Measurement of Maximum Oscillator Frequency