ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUITS
(ECCT)

GENERAL DESCRIPTION

The SAA5243 series are MOS N-channel integrated circuits which perform all the digital logic functions of a 625-line World System Teletext decoder. The SAA5243 series operate in conjunction with the teletext video processor SAA5231, standard static RAMs and are controlled via the 2-wire I²C-bus. The devices can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- $\overline{\text{Odd}}$/even field output for de-interlaced displays

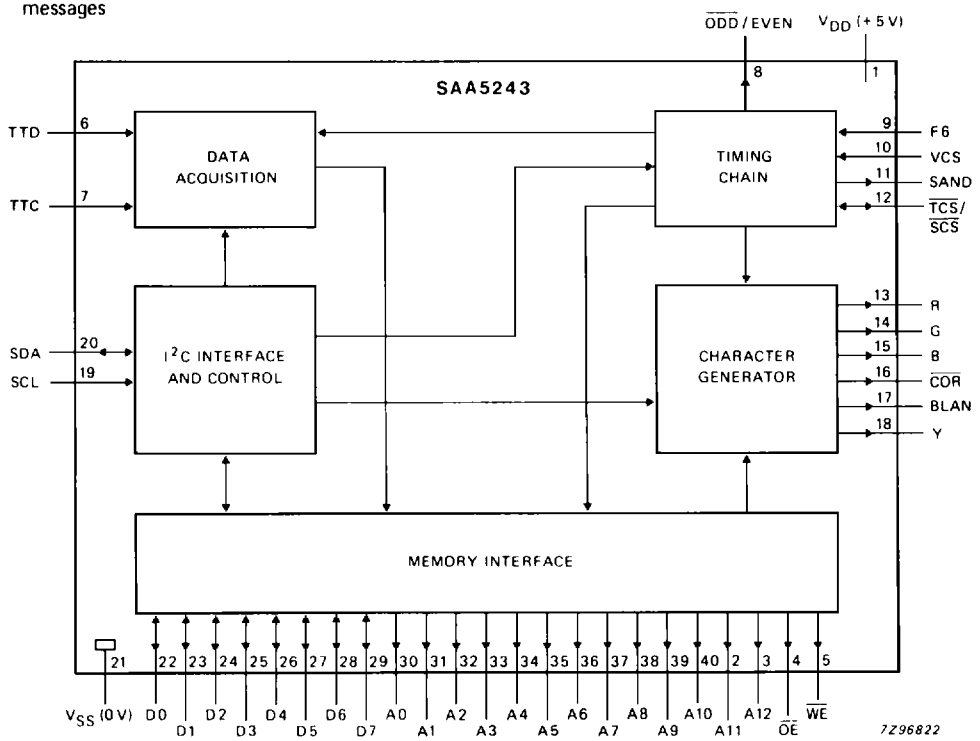


Fig.1 Block diagram.

PACKAGE OUTLINE 40-lead DIL; plastic (SOT129).

ORDERING INFORMATION

type number	version
SAA5243P/E/M2	West European languages
SAA5243P/H	East European languages
SAA5243P/K	Arabic and English languages
SAA5243P/L	Arabic and Hebrew languages
SAA5243P/T	West European and Turkish languages

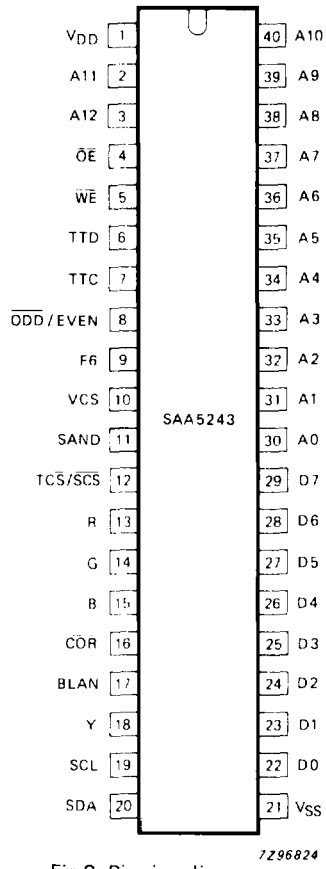


Fig.2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.

5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.
7	TTC	**Teletext Clock**: 6.9375 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{ODD}$/EVEN	**$\overline{Odd}$/Even**: for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{TCS}/\overline{SCS}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig.6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{COR}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	D0-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 1	V_{DD}	−0.3	7.5	V
Input voltage range					
VCS, SDA, SCL, D0-D7		V_I	−0.3	7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$		V_I	−0.3	10.0	V
Output voltage range					
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}$/EVEN, R, G, B, BLAN, $\overline{COR}$, Y		V_O	−0.3	7.5	V
$\overline{TCS}/\overline{SCS}$		V_O	−0.3	10.0	V
Storage temperature range		T_{stg}	−20	+125	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	6.9375	–	MHz
F6 clock frequency	f_{F6}	–	6.0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig.3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig.4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig.3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig.8.
8. For details of RAM timing see Fig.9.
9. For details of synchronization timing see Fig.5.
10. For details of display output timing see Fig.7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig.8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig.9.

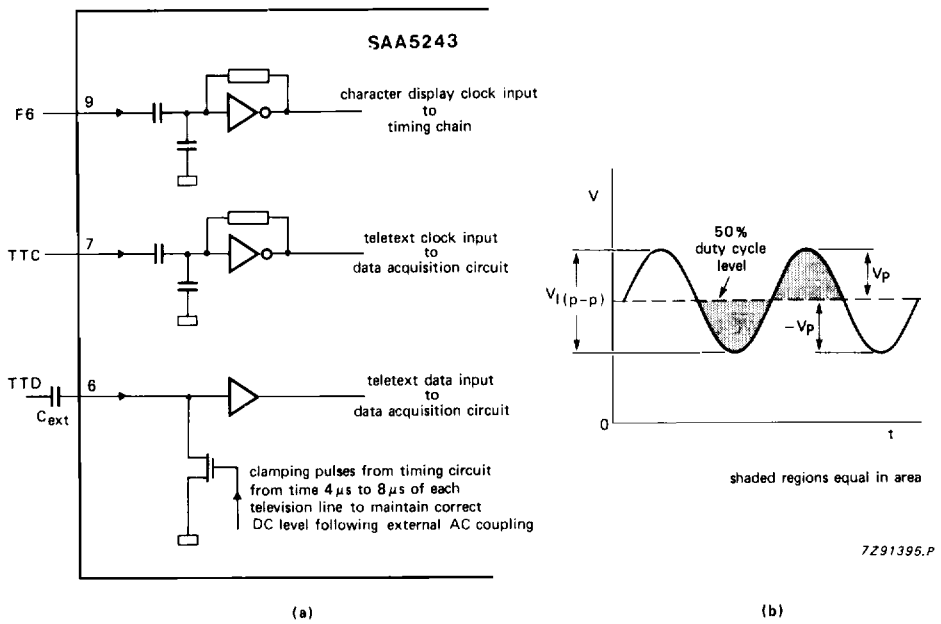
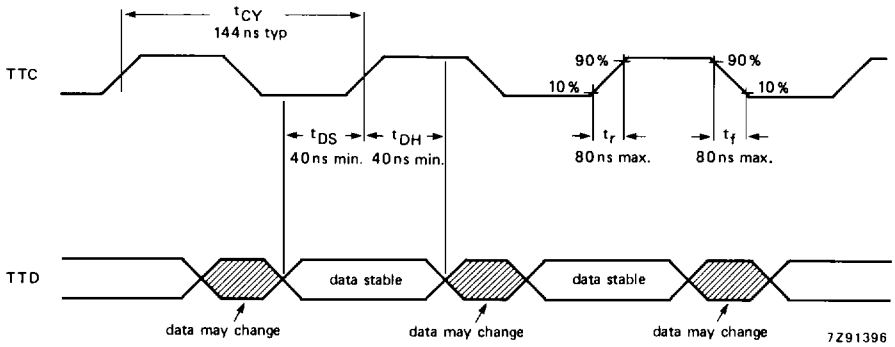


Fig.3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig.4 Teletext data input timing.

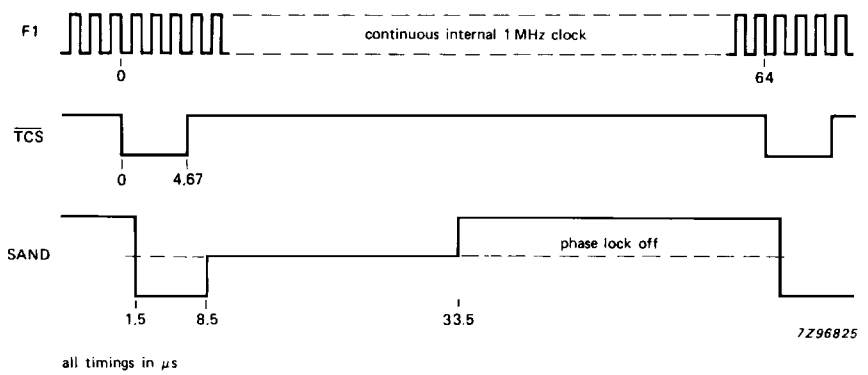


Fig.5 Synchronization timing.

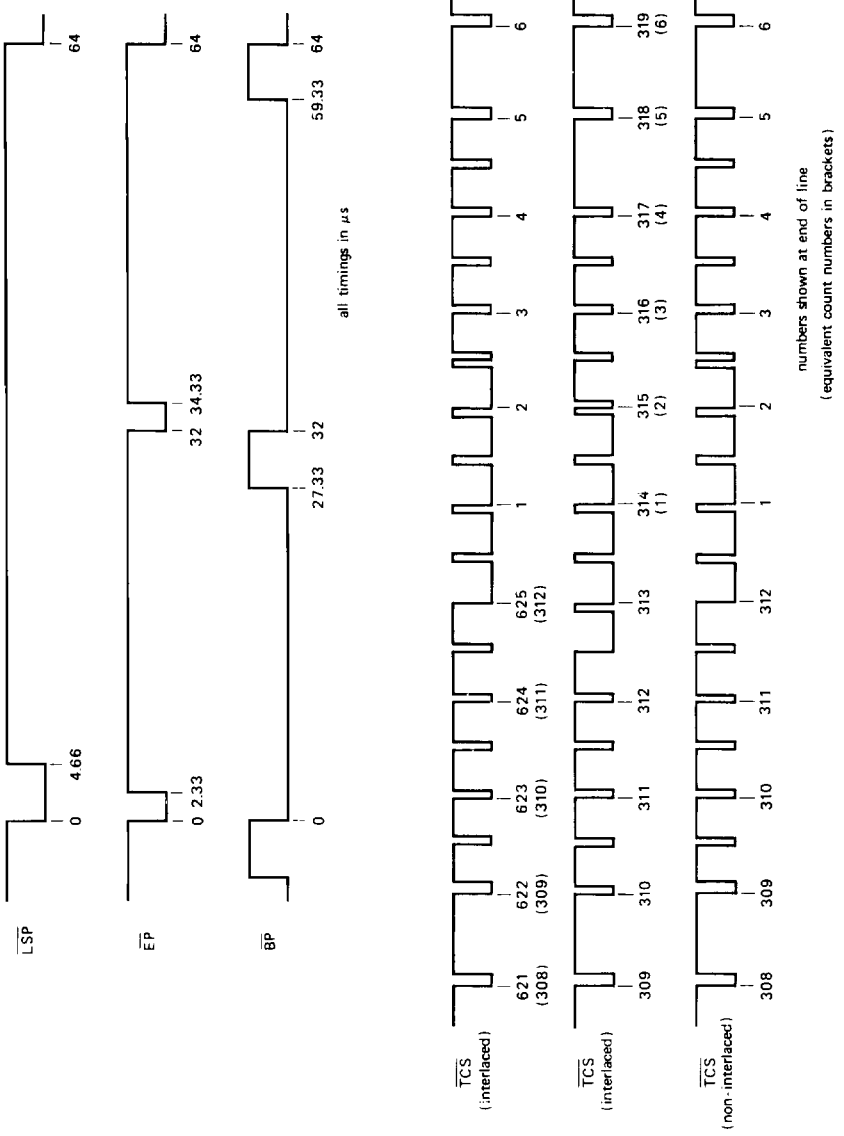


Fig.6 Composite sync waveforms.

Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

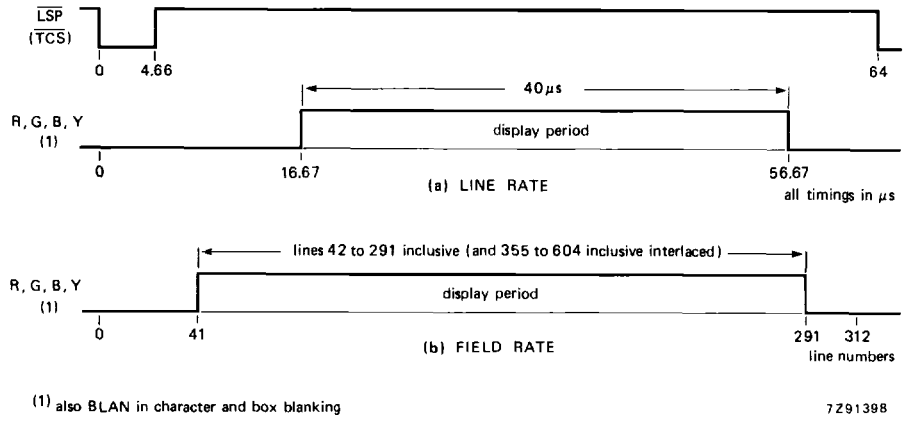


Fig.7 Display output timing (a) line rate (b) field rate.

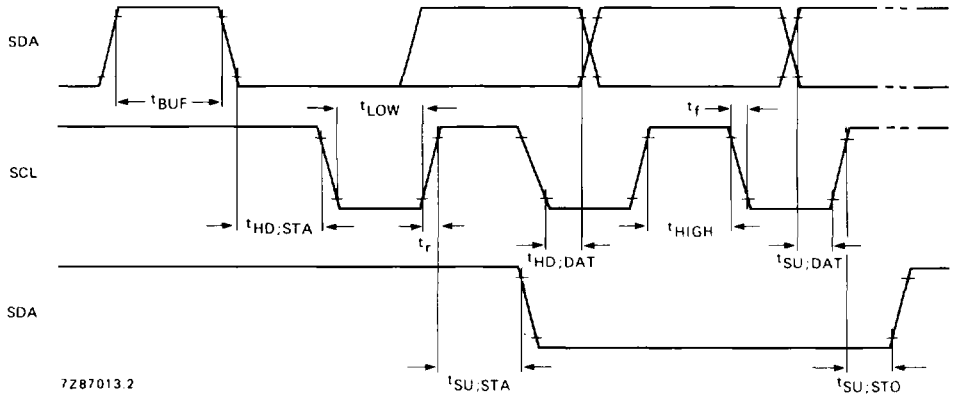


Fig.8 I^2C-bus timing.

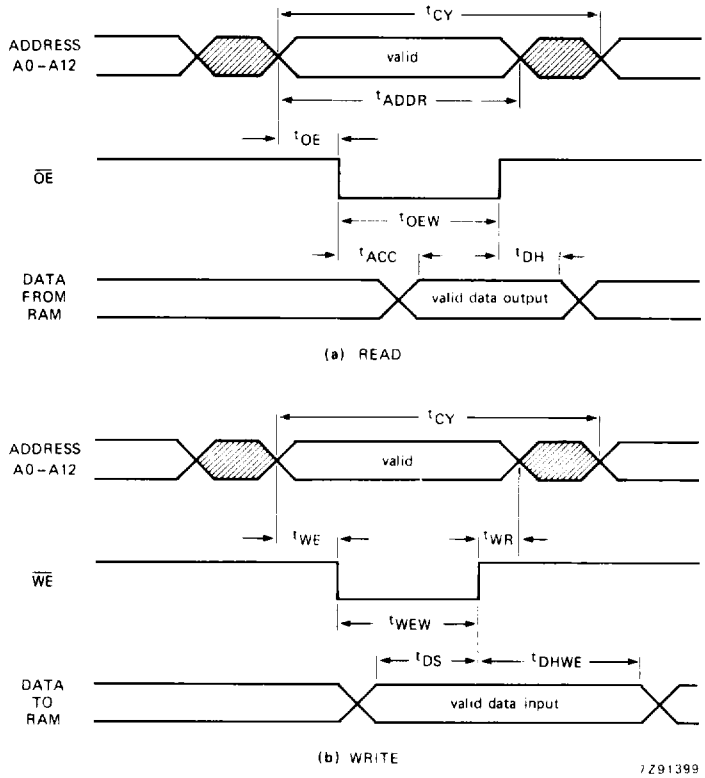
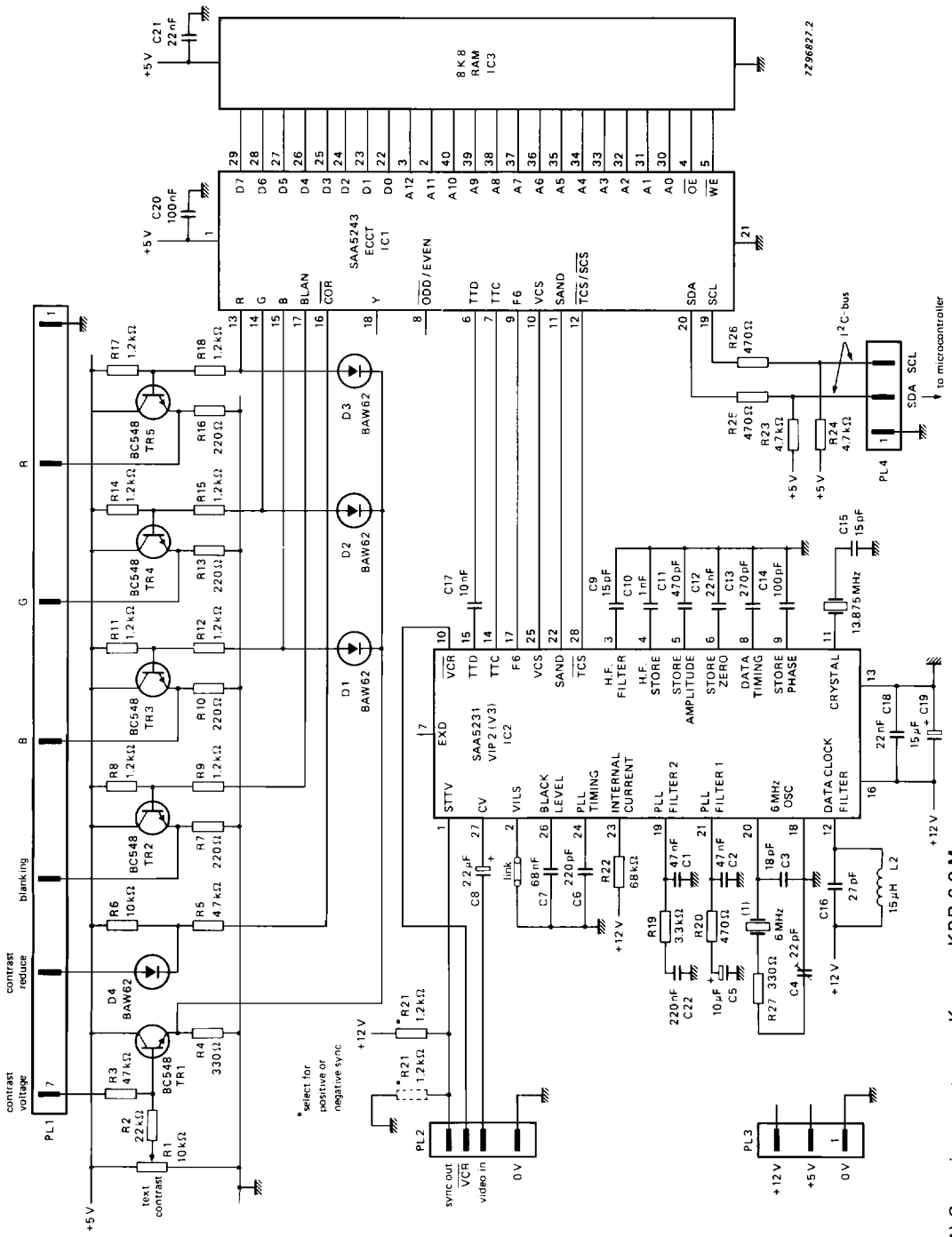


Fig.9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6.0 M.

Fig. 10 ECCT based multi ~ge decoder circuit diagram.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig.11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

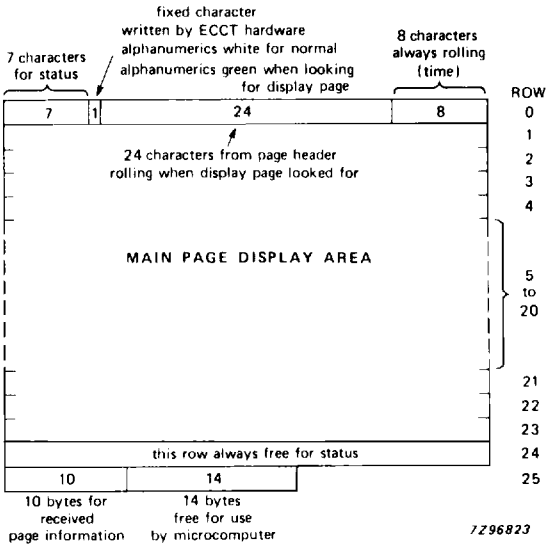


Fig.11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
$\overline{\text{PBLF}}$	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
—	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
—	—	—	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
—	—	—	—	—	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
—	—	—	—	CLEAR MEM.	A2	A1	A0	R8	Active chapter
—	—	—	R4	R3	R2	R1	R0	R9	Active row
—	—	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

— bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode

T0, T1	interlace/non-interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C-bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for DO CARE bits.
When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

Several versions of the ECCT are available, offering a variety of character sets. The full character sets are shown in Tables 4a to 4d.

The world system teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14. These bits are automatically decoded by the ECCT, the resulting character sets are shown in Tables 6a to 6d. For certain languages, control software processing of the extension packet data may be required for optimum useage of the range of available characters. See Fig. 12 for alphanumeric and graphic options.

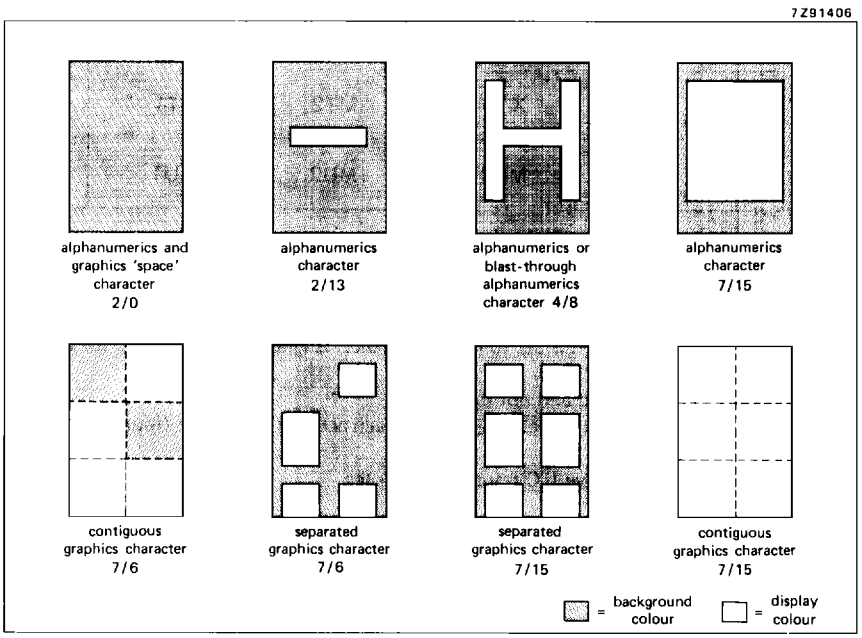
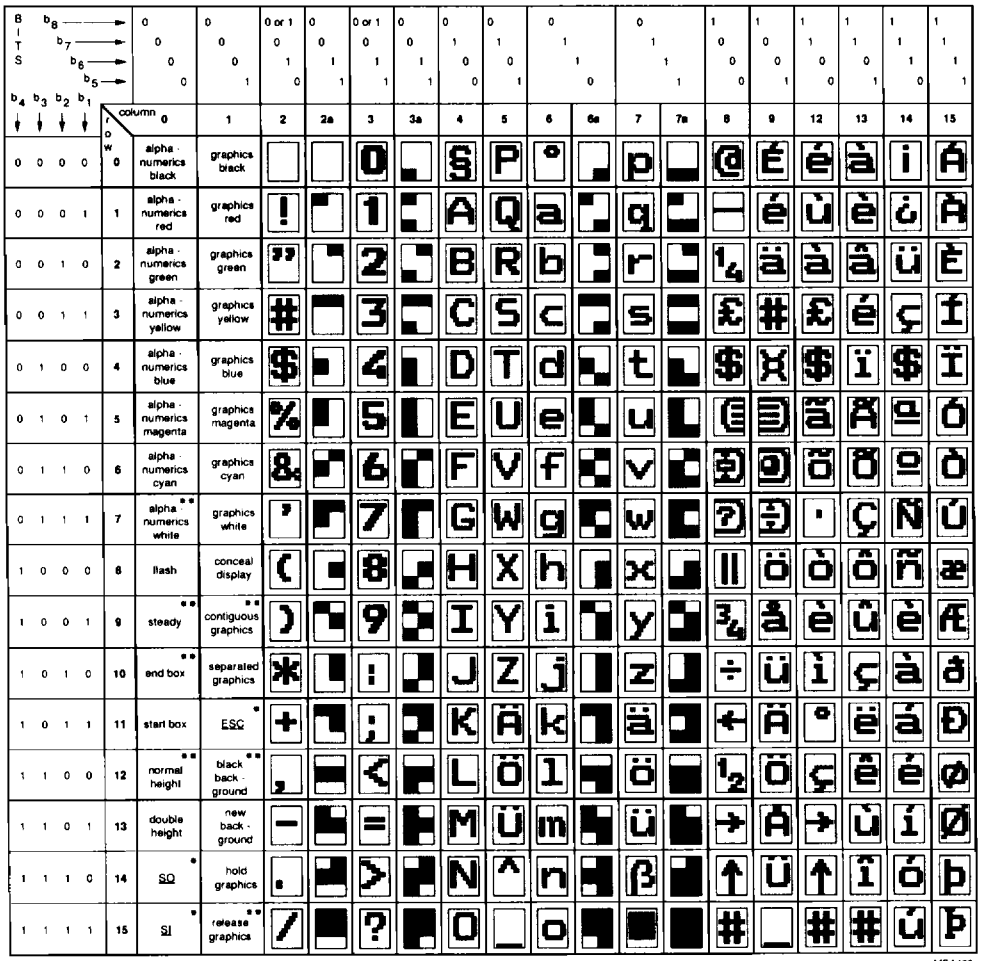


Fig.12 Alphanumeric and graphic options.

Table 4a Character data input decoding, West European languages (SAA5243P/E/M2)

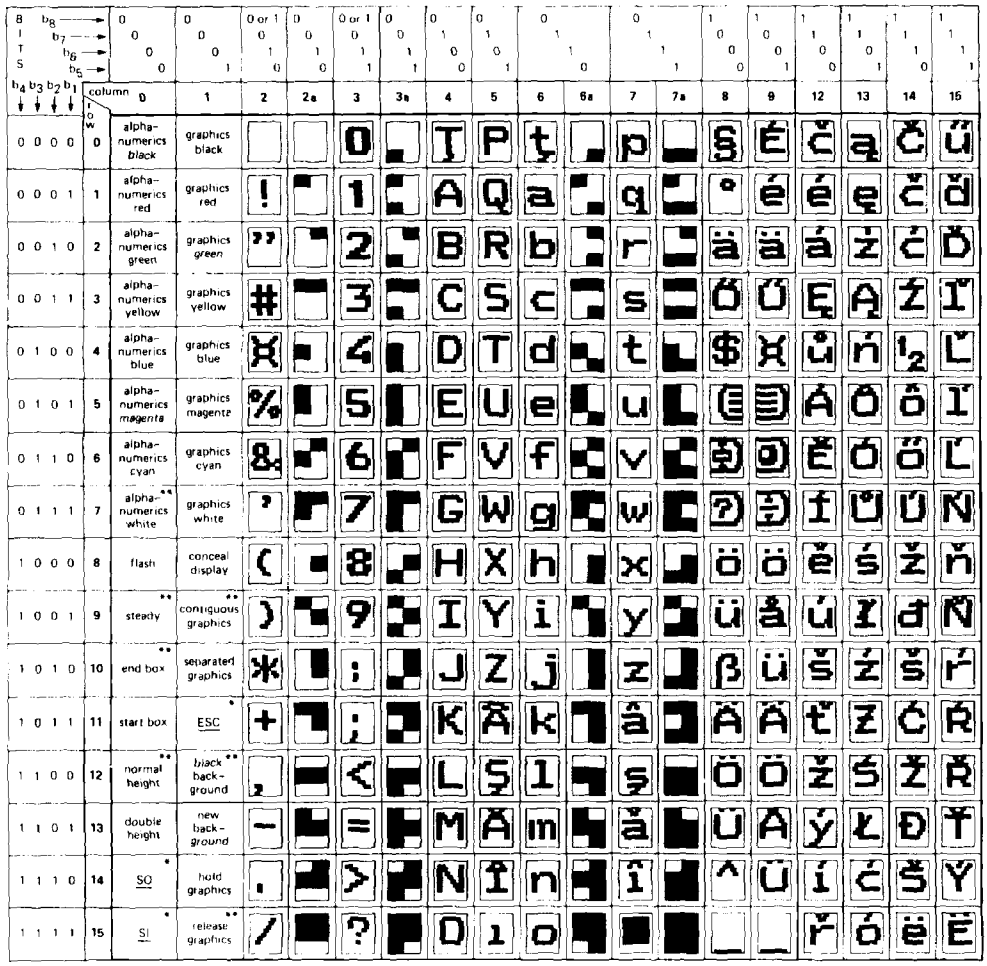


* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4b Character data input decoding, East European languages (SAA5243P/H)



7Z22497.5

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 4c Character data input decoding, Arabic and English languages (SAA5243P/K)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1	1
b_7	0	0	0	1	1	1	0	0	1	1	1	1	0	0	0	1	1	1
b_6	0	1	0	0	1	1	0	1	0	1	1	1	0	0	1	0	1	1
b_5	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column → 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black			0		@	P	—		p		ڈ	•	ڈ	ـ	—	ي
0 0 0 1	1	alpha-numerics red	graphics red	!		1		A	Q	a		q		ڤ	ا	ء	و	ق	ـه
0 0 1 0	2	alpha-numerics green	graphics green	"		2		B	R	b		r		ٹ	ر	ب	ز	ق	ـغ
0 0 1 1	3	alpha-numerics yellow	graphics yellow	£		3		C	S	c		s		ٹ	٣	ب	س	ك	ـق
0 1 0 0	4	alpha-numerics blue	graphics blue	$		4		D	T	d		t		ڤ	٤	ټ	ش	ل	ـق
0 1 0 1	5	alpha-numerics magenta	graphics magenta	%		5		E	U	e		u		!	٥	ټ	ص	م	ـه
0 1 1 0	6	alpha-numerics cyan	graphics cyan	&		6		F	V	f		v		ـ	٦	ا	ض	ن	ـق
0 1 1 1	7	alpha-numerics white **	graphics white	'		7		G	W	g		w		ي	٧	ا	ط	ه	ك
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		)	٨	ب	ظ	و	ـل
1 0 0 1	9	steady **	contiguous graphics **	)		9		I	Y	i		y		(	٩	ة	ع	ى	ـل
1 0 1 0	10	end box **	separated graphics	*		:		J	Z	j		z		ڭ	ڤ	ټ	غ	ب	ـه
1 0 1 1	11	start box	TWIST	+		;		K	←	k		¼		!	ڤ	ڎ	ـ	ټ	ـم
1 1 0 0	12	normal height **	black background **	,		<		L	½	l		‖		>	٨	ج	ج	ح	ـن
1 1 0 1	13	double height	new background	−		=		M	→	m		¾		ڭ	ڤ	ح	ح	خ	ن
1 1 1 0	14	SO *	hold graphics	.		>		N	↑	n		÷		<	ڈ	خ	خ	خ	ـلا
1 1 1 1	15	SI *	release graphics **	/		?		O	#	o		■		؟	٥	ڍ	#	ـ	■

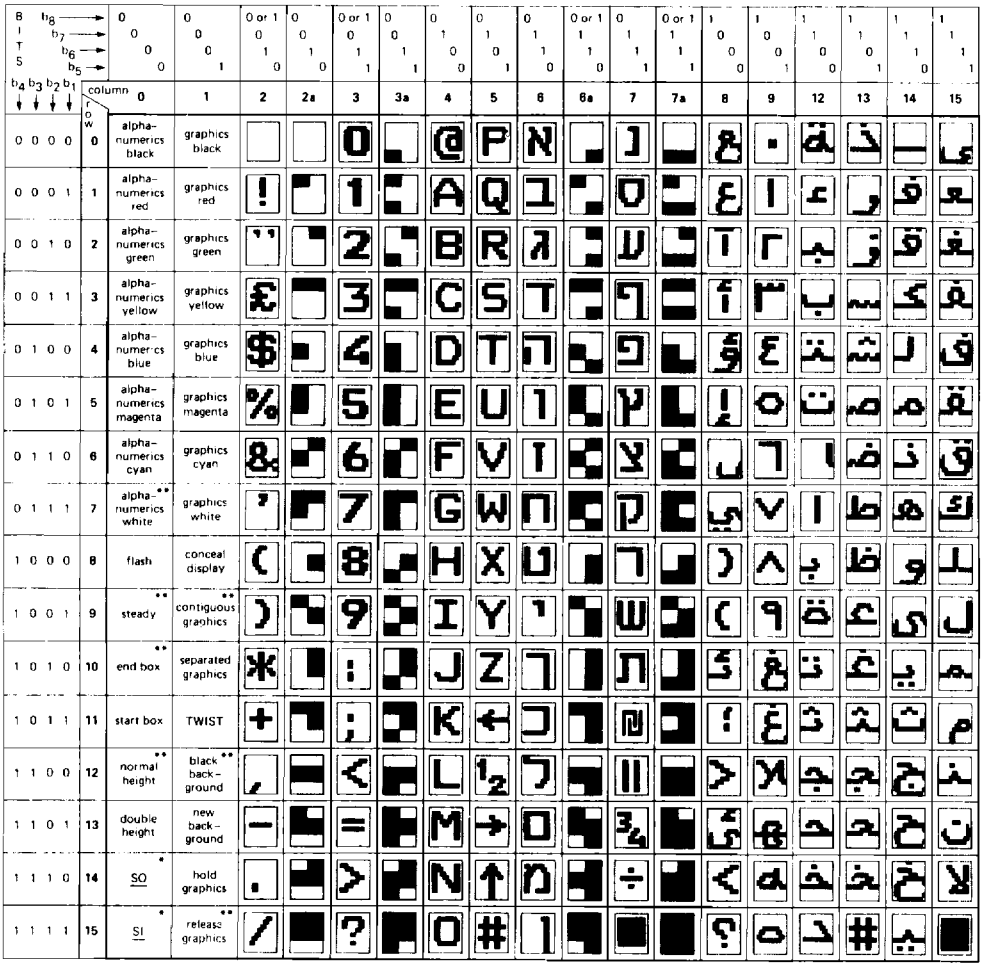
7Z22660.4

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

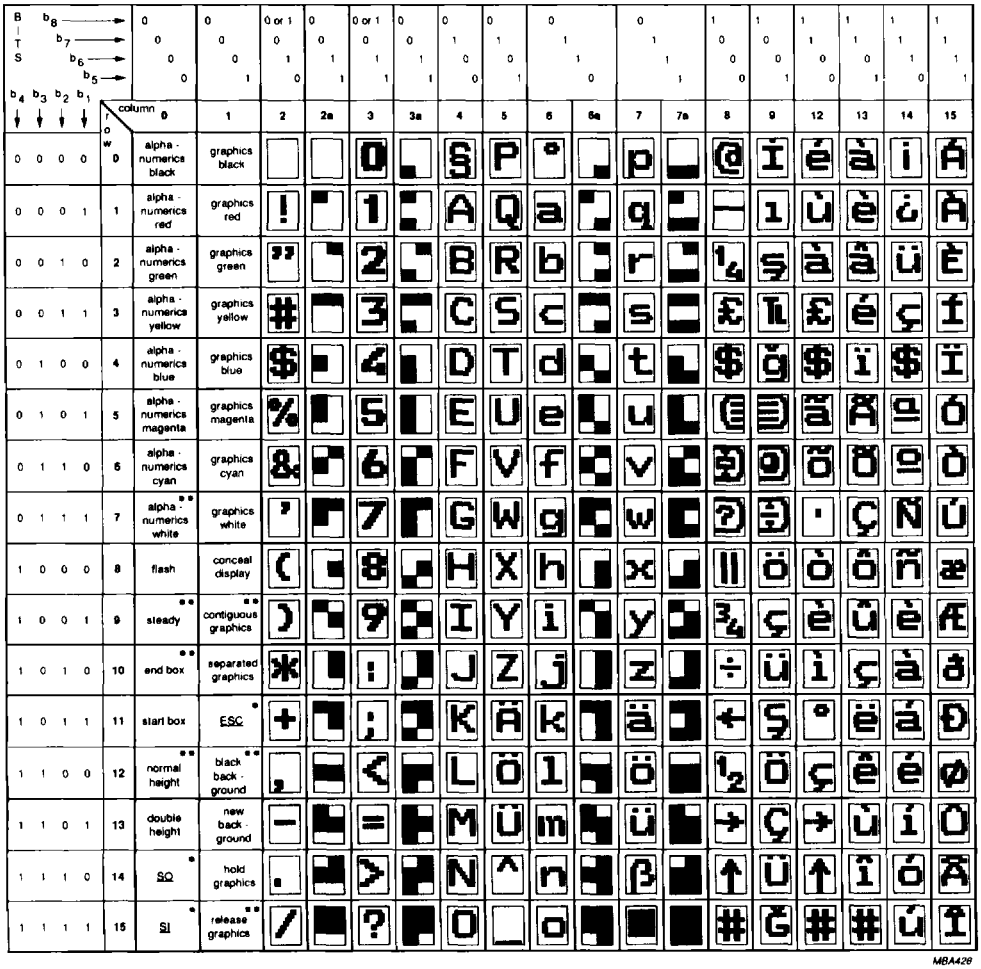
Table 4d Character data input decoding, Arabic and Hebrew languages (SAA5243P/L)



1Z22679.4

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins.

Table 4e Character data input decoding, West European and Turkish languages (SAA5243P/T)



* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4f Character data input decoding, Baltic and Cyrillic Russian (SAA5243P/R)

b_4 b_3 b_2 b_1	column → / row ↓	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha · numerics black	graphics black			0		Š	P	š		p		ā	ī	Ю	П	ю	п
0 0 0 1	1	alpha · numerics red	graphics red	!		1		A	Q	a		q		Ā	Ī	А	Я	а	я
0 0 1 0	2	alpha · numerics green	graphics green	"		2		B	R	b		r		ä	ē	Б	Р	б	р
0 0 1 1	3	alpha · numerics yellow	graphics yellow	#		3		C	S	c		s		Ė	Ē	Ц	С	ц	с
0 1 0 0	4	alpha · numerics blue	graphics blue	$		4		D	T	d		t		ö	ķ	Д	Т	д	т
0 1 0 1	5	alpha · numerics magenta	graphics magenta	%		5		E	U	e		u		Č	Ķ	Е	У	е	у
0 1 1 0	6	alpha · numerics cyan	graphics cyan	ы		6		F	V	f		v		&	ļ	Ф	Ж	ф	ж
0 1 1 1	7	alpha · numerics white **	graphics white	'		7		G	W	g		w		ģ	Ļ	Г	В	г	в
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		ö	Ą	Х	Ь	х	ь
1 0 0 1	9	steady **	contiguous graphics **	)		9		I	Y	i		y		Ų	Ū	И	Ь	и	ь
1 0 1 0	10	end box **	separated graphics	*		:		J	Z	j		z		ü	ņ	Й	З	й	з
1 0 1 1	11	start box	ESC *	+		;		K	ė	k		ą		Ä	Ņ	К	Ш	к	ш
1 1 0 0	12	normal height **	black back · ground **	,		<		L	ę	l		ų		Ö	Į	Л	Э	л	э
1 1 0 1	13	double height	new back · ground	−		=		M	Ž	m		ž		Ģ	Ę	М	Щ	м	щ
1 1 1 0	14	SO *	hold graphics	.		>		N	č	n		į		Ü	°	Н	Ч	н	ч
1 1 1 1	15	SI *	release graphics **	/		?		O	ū	o				ö	½	О	Ы	о	

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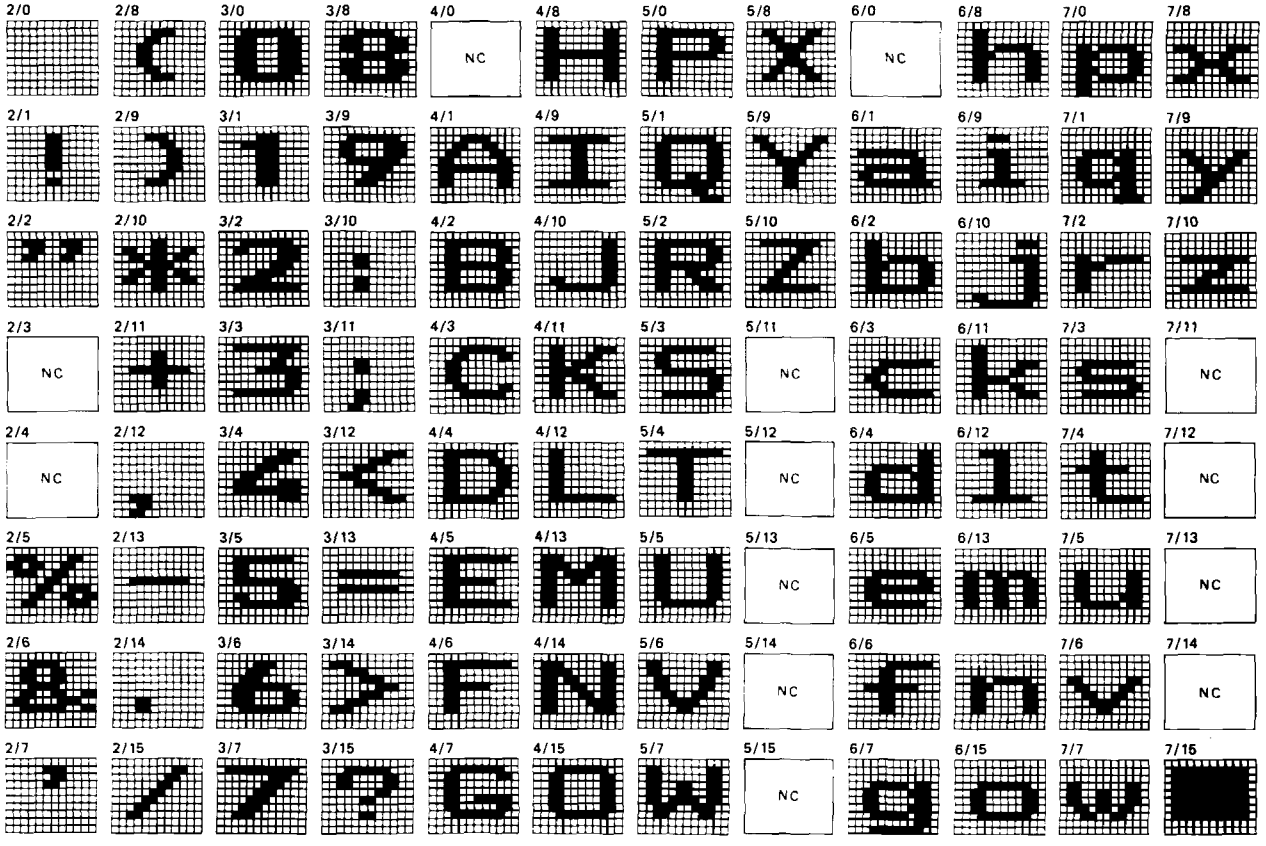
* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 4

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. National option characters are shown in Table 6.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters (for /E and /H character tables only) to combine with character 8/5.
7. With bit 8 = 0 national option character will be decoded according to the setting of control bits C12 to C14 (see Table 6).

Table 5 SAA5243 basic character matrix



Where: *NC national option character position.*

APPLICATION INFORMATION (continued)

Table 6a SAA5243P/E/M2 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)													
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6b SAA5243P/H national option character set

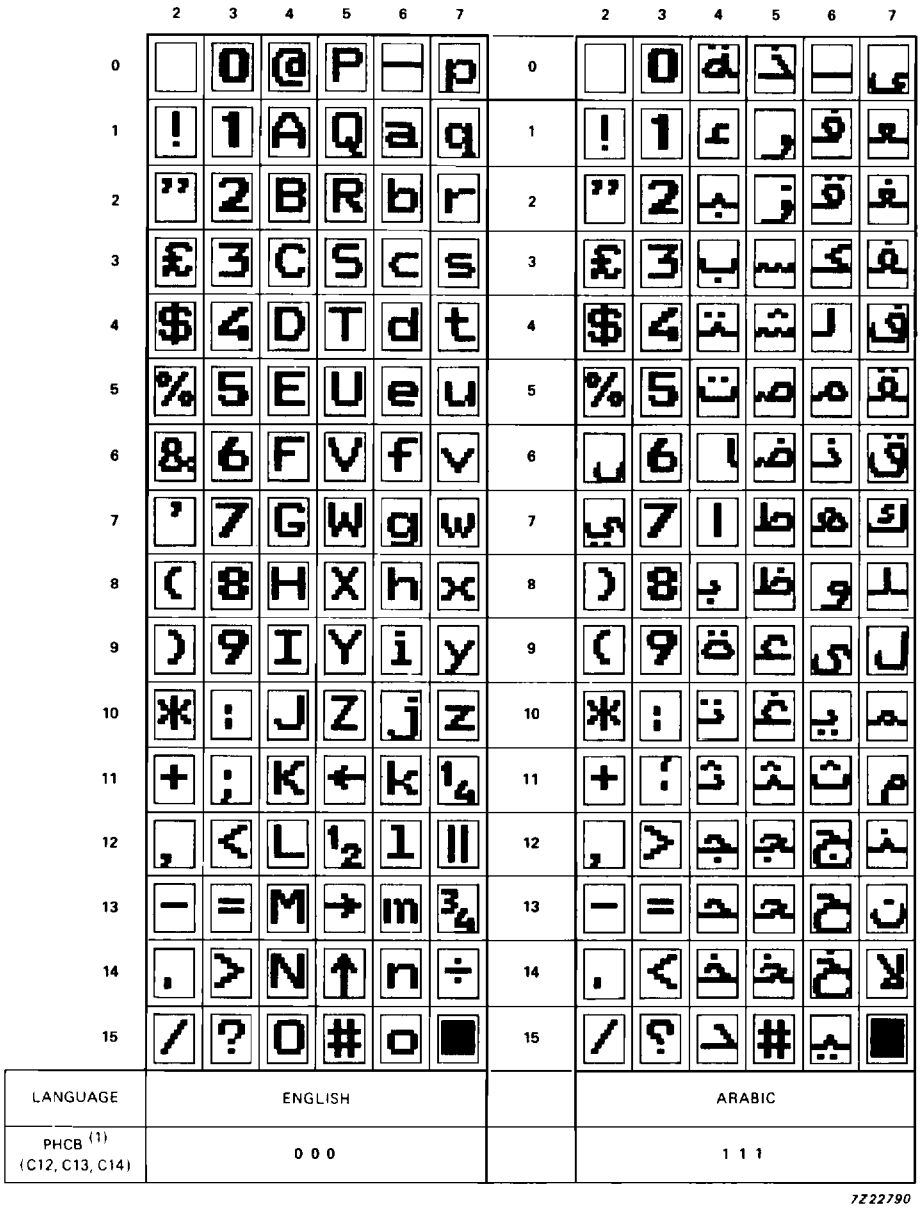
LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

7Z22658.1

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

APPLICATION INFORMATION (continued)

Table 6c SAA5243P/K national option character set

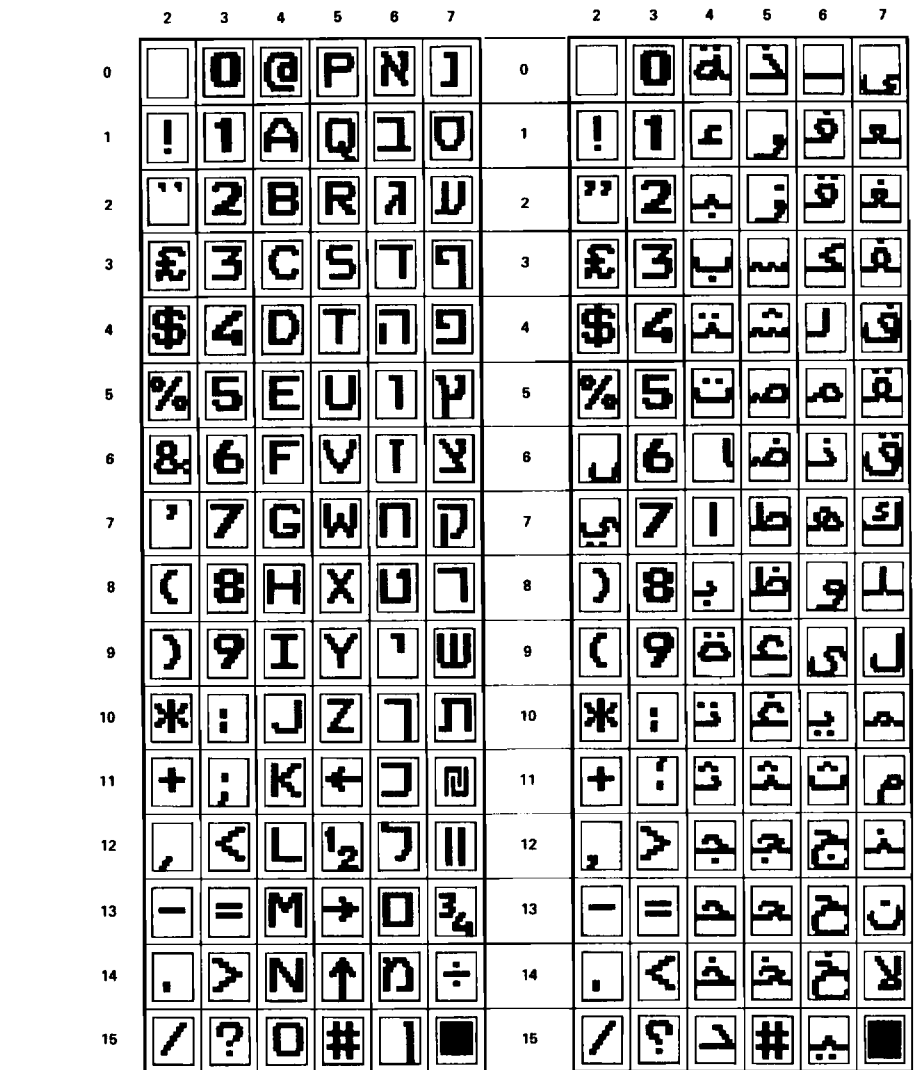


LANGUAGE	ENGLISH		ARABIC
PHCB [1] (C12, C13, C14)	0 0 0		1 1 1

7Z22790

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

Table 6d SAA5243P/L national option character set



(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

APPLICATION INFORMATION (continued)

Table 6e SAA5243P/T national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

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(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6f SAA5243R/L national option character set

LANGUAGE	PHCB [1]			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ESTONIAN	0	1	0	#	Õ	Š	Ä	Ö	Ž	Ü	õ	š	ä	ö	ž	ü
LETTISH / LITHUANIAN	0	1	1	#	$	Š	ė	ę	Ž	Č	ū	š	ą	ų	ž	į
RUSSIAN	1	0	0		О	Ю	П	ю	п							
				!	1	А	Я	а	я							
				"	2	Б	Р	б	р							
				#	3	Ц	С	ц	с							
				$	4	Д	Т	д	т							
				%	5	Е	У	е	у							
				ы	6	Ф	Ж	ф	ж							
				'	7	Г	В	г	в							
				(	8	Х	Ь	х	ь							
				)	9	И	Ь	и	ь							
				ж	:	Й	З	й	з							
				+	;	К	Ш	к	ш							
				,	<	Л	Э	л	э							
				−	=	М	Щ	м	щ							
				.	>	Н	Ч	н	ч							
				/	?	О	Ы	о	■							

MBA647

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.