TV PLL for 62.5 kHz Resolution

SDA 3002

Bipolar IC

Preliminary data

Type	Ordering code	Package
SDA 3002	Q67000-A2267	DIP 18

Combined with a VCO (tuner) and a fast divider (dividing ratio 1:64), the ASBC technology component forms a digitally programmable phase-locked loop for television sets with PLL frequency synthesis tuning. The PLL enables crystal-controlled setting of the tuner oscillator frequency for 125 kHz resolution in the TV band III/IV/V. A serial interface facilitates connection to a microprocessor. The microprocessor loads the divider and the band select outputs with the appropriate information. The PLL provides status information (locked/unlocked) at output LOCK.

Features

- No external integrator required
- Noise-immune message transmission
- Software-controlled integration time constant
- Microprocessor-compatible

Maximum ratings

Supply voltage range	V_S	−0.3 to 7.5	V
Inputs			
Q1, Q2, I_{REF}	V_i	−0.3 to V_S	V
IFO, CPL	V_i	−0.3 to V_S + 0.5	V
PLE	V_i	−0.3 to 7.8	V
F, $\overline{F}$	V_i	−0.3 to V_S + 0.5	V
Outputs			
PD	V_q	−0.3 to V_S	V
V_D	V_q	−0.3 to 33	V
	I_{qL}	−7	mA
BS, $\overline{VHF}$, $\overline{UHF}$, $\overline{Bd\ I/III}$, standard	V_q	−0.3 to 16	V
LOCK	I_q	−1 to 5	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage	V_S	4.5 to 7.15	V
Input frequency	f_F, $f_{\overline{F}}$	16	MHz
Divider factor	N	1024 to 16383	
Resistance for I_{REF}	R_i	80	kΩ
$I_{REF} = (V_S - 0.8)\ R_i$			
Tuning voltage open collector	V_D	0.3 to 33	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_S = 5$ V; $T_A = 25$ °C

		min	typ	max	
Supply current	I_S	15	22	35	mA
Signal inputs F/$\overline{F}$					
Input voltage	V_{16H}			$V_S + 0.2$	V
	V_{16L}	3.8			V
Input current	I_{16}			50	µA
$V_{16} = 5$ V					
Input sensitivity at sine push-pull; $f = 16$ MHz (peak-to-peak)	V_{16pp}	120		1200	mV
Inputs (IFO, CPL, PLE)					
Input voltage	V_{8H}	2.4			V
	V_{8L}			0.8	V
Input current					
$V_{8H} = 5$ V	I_{8H}			8	µA
$V_{8L} = 0.4$ V	I_{8L}			−550	µA
Band select outputs					
Reverse current	I_{3H}			10	µA
$V_{3H} = 15$ V					
Current drain	I_{3H}	0.5		3	mA
$2\text{ V} \leq V_3 \leq 15$ V					
Tuning section PD, V_D, I_{REF}, LOCK					
Charge pump current	I_{13}	±250		±550	µA
$I_{pump} = 10 \times I_{REF}$; $V_S = 5$ V					
Tuning voltage	V_{15L}			0.3	V
$I_{15L} = 1.5$ mA					
Reverse current	I_{15H}			20	µA
$V_{15H} = 33$ V					
Reference current	I_{14}	30		40	µA
ext. $R = 120$ kΩ; $V_S = 5$ V					
Output voltage	V_{12H}	4.5			V
int. $R_L = 3$ kΩ					
$I_{12H} = -100$ µA					
$I_{12L} = 100$ µA	V_{12L}			0.7	V
IFO, PLE					
Set-up time for					
enable	t_{VE}	2			µs
data	t_{VD}	2			µs
Hold time for:					
enable	t_{HE}	2			µs
data	t_{HD}	2			µs
CPL					
H pulse width	t_{CH}	2			µs
L pulse width	t_{CL}	2			µs

Circuit description

Triggered by the ECL inputs F/$\overline{F}$ a switchable 32/33 counter operates as a 14-bit synchronous divider in the dual modulus method when combined with a 5 and 9-bit programmable synchronous counter. In this combination the 5-bit counter controls the switch-over from 32 to 33 (block diagram 1). Dividing ratios of $N = 1024$ to 16383 are possible.

The 18-bit deep shift register with latch is subdivided into 14 bits for storing the dividing ratio N, as well as 1 bit for selecting the pump current and 1 bit for a standard switch-over. The remaining 2 bits control the 4 band selection outputs. The message is inserted over the serial data input IFO with the H-L slope of the shift clock CPL, when the enable input is set at H. Beginning with LSB, the complement of the dividing ratio is inserted in binary code, then the select bit 2^{14} for the pump current and the control bit 2^{15} for standard TV switch-over are added. The band selection control bits 2^{16} and 2^{17} complete this process (refer to table).

An integrated control circuit checks the world length (18 bits) of the data message. The 18-bit latch accepts the data from the shift register during the L state of the enable input PLE.

A 4 MHz crystal controlled clock oscillator has been integrated in the IC. An internal reference divider divides the output signal of the crystal oscillator ($f_{OSC} = 4$ MHz) by 4096 resulting in 0.97656 kHz (reference signal), providing a frequency resolution of 62.5 kHz by means of the asynchronous permanent divider (dividing factor 64).

In a digital phase detector the divided VCO input signal is compared with the reference signal. If the trailing edge of the VCO input signal appears before the trailing edge of the reference signal, the output DOWN of the phase detector will be in the H state for the duration of the phase difference. However, if above signal sequence is reversed, the output UP will be in the H state instead. The outputs UP/DOWN control the two current sources $I+$ and $I-$ (charge pump). In case both outputs are in the L state, the charge pump output will be in the high impedance mode (TRISTATE). Information with respect to either the H or L state will be provided at the LOCK output by the logical "NOR" of the outputs UP/DOWN.

The output current of the charge pump (source current = drain current) is adjusted by an external resistor between pin I_{REF} and V_{CC}. In addition, this output current can be generated by the control bit for the pump current at the same value or at a value increased by a factor of 10 (refer to table).

The current pulses generated by the charge pump are integrated into the tuning voltage by means of an active low pass filter (on-chip loop amplifier and external RC circuit). The dc output signal of the low pass filter is available at V_D and is used as tuning voltage for the VCO. In order to provide tuning voltages higher than $V_{CC} = 5$ V, the output stage of the amplifier consists of a transistor with an open collector. The external collector resistor can be connected to voltage up to 33 V.

To switch voltages higher than $V_{CC} = 5$ V, the band selection outputs (Bd I/III, VHF, UHF, Standard, BS) include current drains with open collectors. It is therefore possible to directly connect transistors operating as band selection switches without the use of current limiting resistors (please refer to application circuit).

Pin description

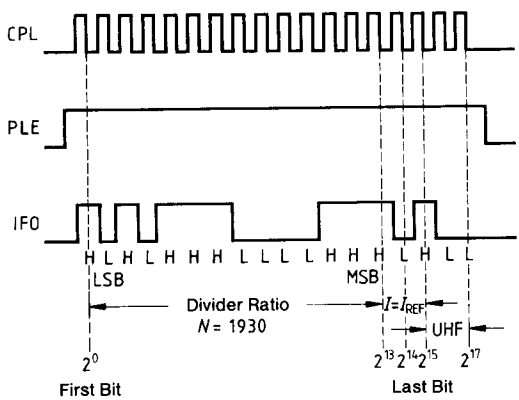
Pin	Symbol	Function
1	Q 1	Crystal
2	Q 2	Crystal
3	Standard	Standard switchover output
4	BS	Band selection output BS
5	VHF	Band selection output VHF
6	UHF	Band selection output UHF
7	Bd I/III	Band selection output I/III
8	PLE	Enable input for shift register
9	GND	Ground
10	CPL	Shift clock pulse input
11	IFO	Data input
12	LOCK	Lock output
13	PD	Amplifier input/charge pump output
14	I_{REF}	Current adjustment for charge pump
15	V_D	Tuning voltage output
16	F	Signal input
17	$\overline{F}$	Signal input
18	V_S	Supply voltage

Truth table

Pump current	IFO-Bit 2^{14}	Bit 2^{15}	Output Standard
$I = I_{REF}$	L		L
$I = 10 \times I_{REF}$	H		H

IFO-Bit 2^{16}	IFO-Bit 2^{17}	Band selection outputs*) Bd I/III	VHF	UHF	BS	Meaning
L	L	H	H	L	H	UHF
L	H	H	L	H	H	VHF/Bd I
H	L	L	L	H	H	VHF/Bd III
H	H	L	L	H	L	BS

Pulse diagram



*) L = conductive; H = blocking

Computation for loop filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\xi = 0.5 \times \omega_R \times R \times C_1$

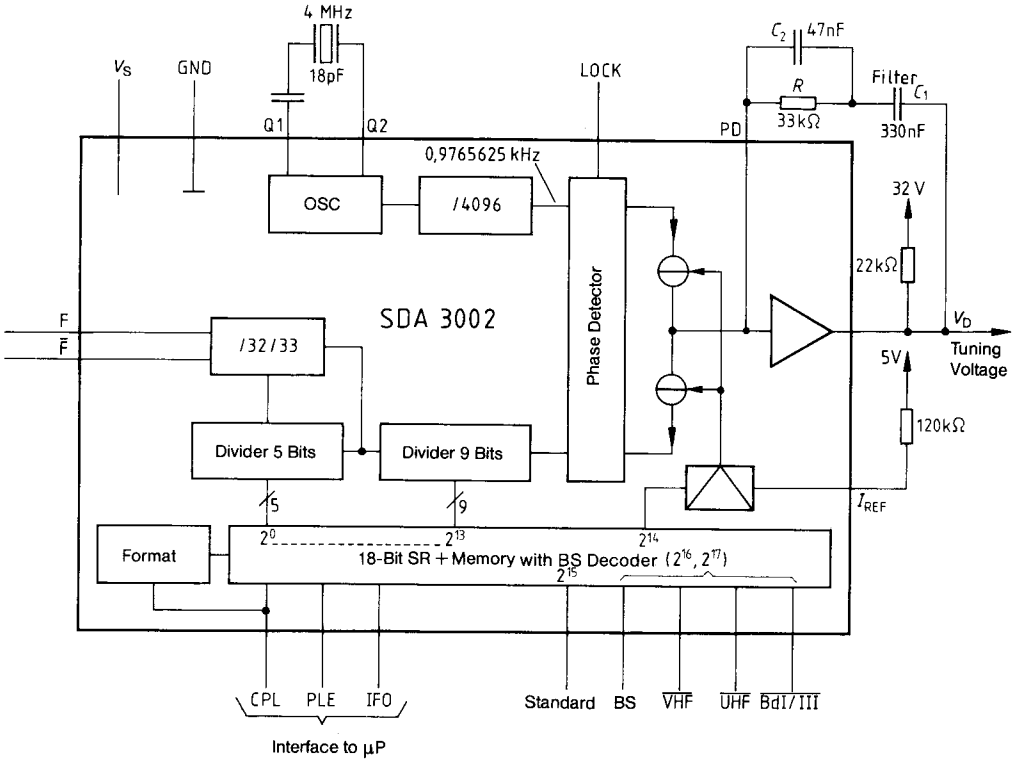
P = Prescaler
N = Progr. divider
I_P = Pump current
K_{VCO} = Tuner slope
R, C_1 = Loop filter

Example for channel 47

$P = 64$; $N = 11520$; $I_p = 200\ \mu A$; $K_{VCO} = 18.7$ MHz/V; $R = 33\ k\Omega$; $C_1 = 330$ nF
$\omega_R = 124$ Hz; $f_R = 20$ Hz; $\xi = 0.675$

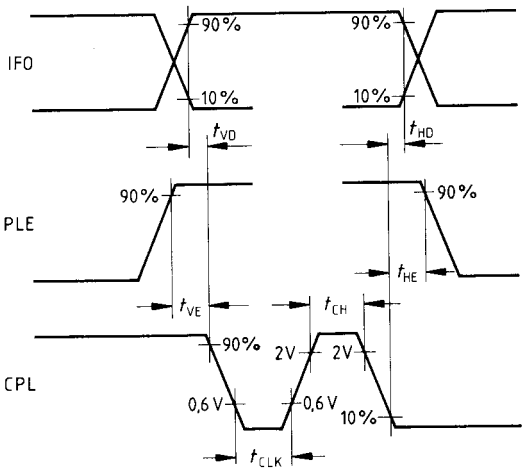
Standard dimensioning: $C_2 \approx C_{1/5}$

Block diagram



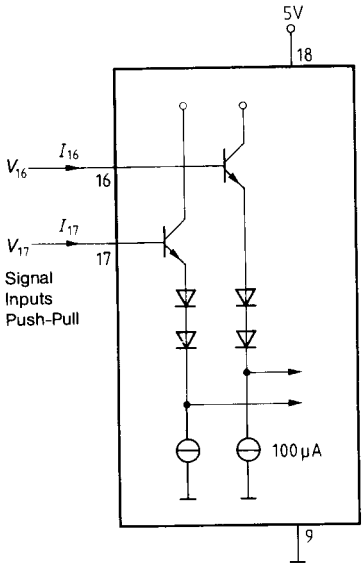
Pulse diagram

Set-up and hold times

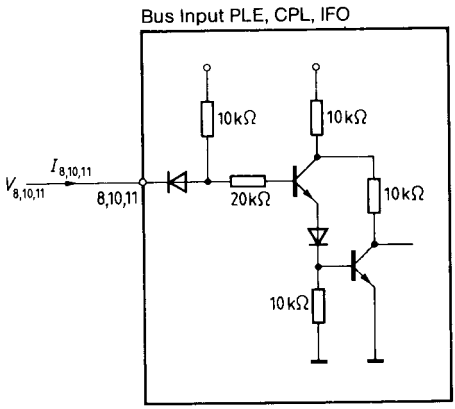


Test and measurement circuits

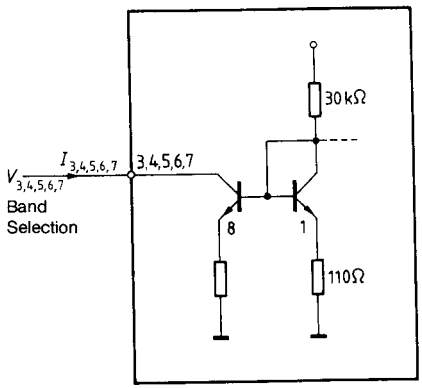
Test circuit 1



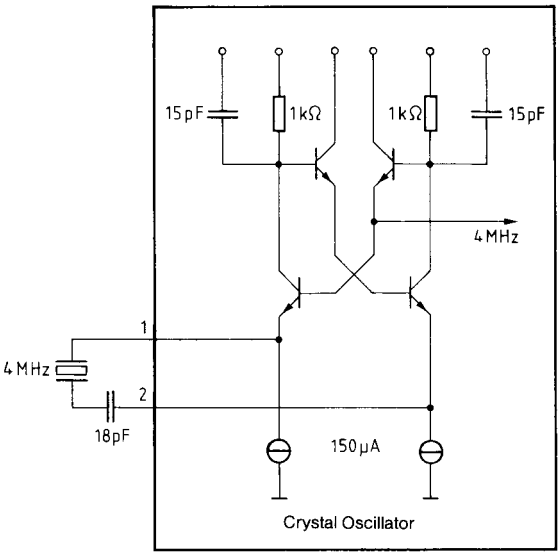
Test circuit 2



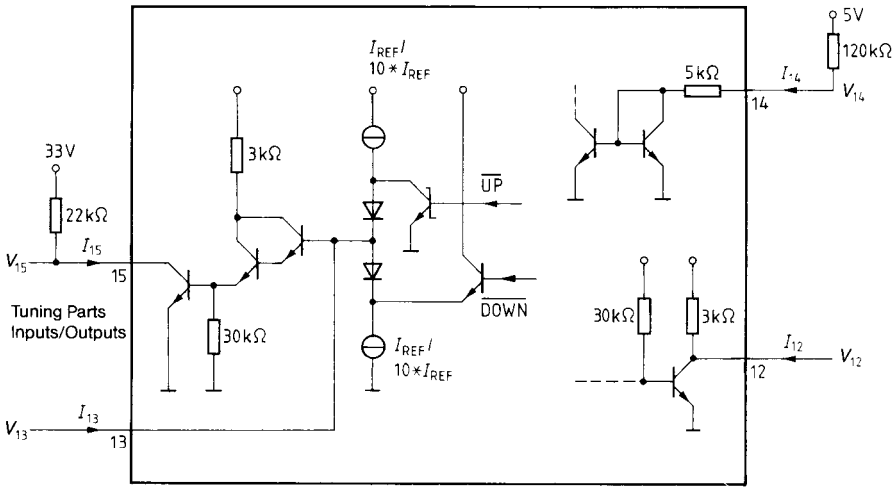
Test circuit 3



Test circuit 4



Test circuit 5



Application circuit

Dimensional proposal: $R_1 = 120\ k\Omega$ ($I_P = 35/350\ \mu A$)
$R_L = 22\ k\Omega$; $R_2 \ldots R_4 = 22\ k\Omega$
Loop filter: $R = 33\ k\Omega$; $C_1 = 330\ nF$; $C_2 = 47\ nF$
Filter (in tuner): $R_T = 10\ k\Omega$; $C_T = 47\ nF$