

HIGH SPEED CURRENT MODE PWM CONTROLLER

DESCRIPTION

The SG1528/30 family of single-ended pulse width modulators are optimized for high frequency, current mode control of switching power supply applications. The control architecture also allows its use as a uni-directional motor speed controller. The circuit features internally preset start-up and run voltage thresholds compatible with power N-channel MOSFETs. A precision low-drift bandgap reference exhibits excellent long-term stability. Both the voltage error amp and current amp are wideband operational amplifiers for high speed performance and maximum applications flexibility. A high peak-current totem-pole output driver permits direct drive of the power switch. The difference between these two series of controllers is the maximum duty cycle range of the output stage. The SG1530 family can operate to duty cycles approaching 100%, where they are mainly used in non-isolated DC-DC converters whereas the 1528 series has a duty cycle range of zero to <50%, optimized for isolated, primary-side control of switching power supplies. The SG1528/1530 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2528/2530 is characterized for the industrial range of -25°C to 85°C, and the SG3528/3530 is designed for the commercial range of 0°C to 70°C.

FEATURES

- Current mode or voltage mode control
- Micropower start-up mode (0.6mA max.)
- ±1% Low-drift reference
- Wideband voltage error amp (6MHz typ.)
- Wideband current differential amp (12MHz typ.)
- Output Frequencies to 2MHz
- Programmable DC Bus O.V. and U.V. sense
- High speed shutdown
- Soft start
- Full fault suppression logic
- 2A peak output current drive
- Output driver rise and fall time less than 30ns
- Ideal for using with SENSFETS

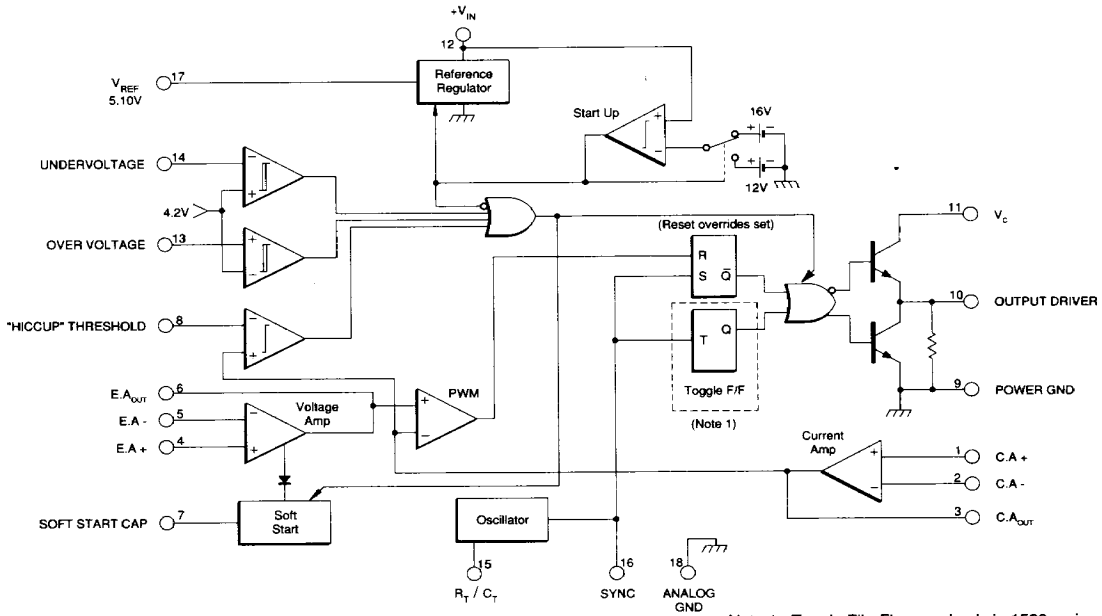
HIGH RELIABILITY FEATURES

- SG1528/SG1530

- ◆ Available to MIL-STD-883
- ◆ SG level "S" processing available

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BLOCK DIAGRAM



Note 1. Toggle Flip-Flop used only in 1528 series.

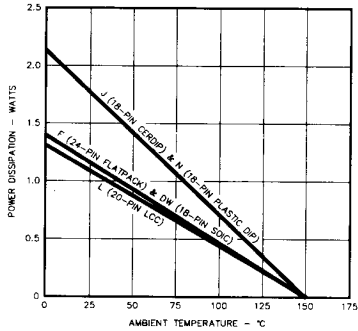
ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage (V_{IN} , V_C)	22V
Analog Inputs (ERR, CUR, OV, UV)	-0.3V to V_{IN}
Logic Inputs (SYNC)	-0.3V to 5.5V
Source / Sink Load Current (continuous)	0.5A
Source / Sink Load Current Peak (200ns)	3A
Reference Load Current	50mA
Soft Start Discharge Current	50mA
Sync Output Source Current	5mA

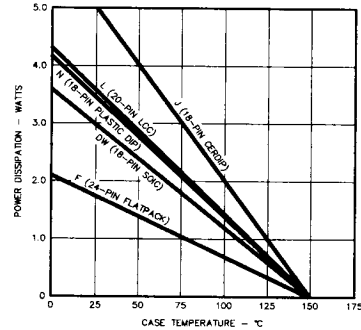
Error Amplifier Output Current	5mA
Current Sense Amplifier Output Current	5mA
Oscillator Discharging Current	5mA
Operating Junction Temperature	
Hermetic (J, F, L Packages)	150°C
Plastic (N, DW Packages)	150°C
Storage Temperature	-65°C to 150°C

Note 2. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3. Range over which the device is functional.)

Collector Voltage	4.5V to 20V
Supply Voltage Range	13V to 20V
Source / Sink Output Current (continuous)	0.3A
Source / Sink Output Current Peak (200ns)	1.5A
Reference Load Current	0 to 10mA
Oscillator Frequency Range	1KHz to 1.5MHz

Oscillator Timing Resistor (R_T)	1K Ω to TBD
Oscillator Timing Capacitor (C_T)	500pF to 0.1 μ F
Operating Ambient Temperature Range	
SG1528	-55°C to 125°C
SG2528	-25°C to 85°C
SG3528	0°C to 70°C

ELECTRICAL SPECIFICATIONS (Note 4)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1528/SG1530 with $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, SG2528/SG2530 with $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, SG3528/SG3530 with $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, and $V_{IN} = V_C = 15\text{V}$ (Note 5). Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1528/2528 SG1530/2530			SG3528 SG3530			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	$T_J = 25^\circ\text{C}$, $I_O = 1\text{mA}$	5.05	5.10	5.15	5.05	5.10	5.15	V
Line Regulation	$V_{IN} = 13\text{V to } 20\text{V}$		3	15		3	15	mV
Load Regulation	$I_L = 1 \text{ to } 10\text{mA}$		2	15		2	15	mV
Temperature Stability (Note 6)			20	40		20	40	mV
Total Output Variation	Line, Load and Temp			5.2	5.0		5.2	V
Output Noise Voltage (Note 6)	$T_J = 25^\circ\text{C}$, 10Hz < f < 10KHz	5.0				100		$\mu\text{V}/\text{rms}$
Long-Term Stability (Note 6, 7)	$T_J = 125^\circ\text{C}$, 1000Hrs		5	25		5	25	mV
Short Circuit Output Current	$V_{REF} = 0\text{V}$	15	50	100	15	50	100	mA
Oscillator Section (Note 8)								
Initial Accuracy	$T_J = 25^\circ\text{C}$, $C_{SYNC} \leq 10\text{pF}$	0.9	1.0	1.1	0.9	1.0	1.1	MHz
Voltage Stability	$V_{IN} = 13\text{V to } 20\text{V}$			± 0.5			± 0.5	%
Temperature Stability	Over Operating Range		± 4	± 8		± 4	± 8	%
Minimum Frequency	$R_T = \text{TBD}$; $C_T = \text{TBD}$		0.5	1.0		0.5	1.0	KHz
Maximum Frequency	$R_T = \text{TBD}$; $C_T = \text{TBD}$	2	3		2	3		MHz
Ramp Peak Voltage				3.8			3.8	V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1528/2528 SG1530/2530			SG3528 SG3530			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 8)								
Ramp Valley Voltage			2.8			2.8		V
Ramp Valley to Peak Amplitude		0.9	1.0	1.1	0.9	1.0	1.1	V
Sync Output High Level	$T_J = 25^\circ\text{C}, I_{\text{SYNC}} = 1\text{mA}$	4.2	4.35	4.5	4.2	4.35	4.5	V
Sync Output Low Level	$T_J = 25^\circ\text{C}, I_{\text{SYNC}} = 1\text{mA}$	3.35	3.55	3.75	3.35	3.55	3.75	V
Sync Input High Level (Note 6)	$T_J = 25^\circ\text{C}$	4.25			4.25			V
Sync Input Low Level (Note 6)	$T_J = 25^\circ\text{C}$			3.6			3.6	V
Sync Input Current, High & Low (Note 6)	(Note 6)		1	2		1	2	mA
Sync Output Pulse	$C_{\text{CLK}} \leq 10\text{pF}, I_{\text{SYNC}} = 0\text{mA}$	200	275	350	200	275	350	ns
Error Amplifier Section (E.A) (Note 9)								
Input Offset Voltage	$R_S \leq 100\Omega, E.A_{\text{OUT}} = 2.5\text{V}$			5			5	mV
Input Bias Current	$V_{\text{CM}} = 2.5\text{V}$			15			15	μA
Input Offset Current	$V_{\text{CM}} = 2.5\text{V}$			2.5			2.5	μA
Common Mode Range		1.7		7	1.7		7	V
Open Loop Gain	$V_{\text{CM}} = 2.5\text{V}, \text{Output Volt. } 1 \text{ to } 2.5\text{V}, R_L = 10\text{K}$	60	64		60	64		dB
Unity Gain Bandwidth (Note 6)	$A_{\text{VOL}} = 0\text{dB}$	4	6		4	6		MHz
Output Voltage Slew Rate (Note 6)	See Figure TBD	5	10		5	10		V/ μs
CMRR	$V_{\text{CM}} = 1.7\text{V to } 7\text{V}$	75	100		75	100		dB
PSRR	$V_{\text{IN}} = 13\text{V to } 20\text{V}$	90			90			dB
Output Sink Current	$E.A_{\text{OUT}} = 2\text{V}, \Delta V = 150\text{mV}$	0.4	0.7		0.4	0.7		mA
Output Source Current	$E.A_{\text{OUT}} = 2\text{V}, \Delta V = 150\text{mV}$	3	6		3	6		mA
Output High Level	$R_L = 10\text{K}$	2.6	2.8	3.8	2.6	2.8	3.8	V
Output Low Level	$R_L = 10\text{K}$		0.1	0.3		0.1	0.3	V
Current Sense Amplifier (C.A) Section (Note 10)								
Input Offset Voltage	$R_S \leq 10\Omega, C.A_{\text{OUT}} = 2.5\text{V}, V_{\text{CM}} = 1.5\text{V}$		2.5	5		2.5	5	mV
Input Bias Current	$V_{\text{CM}} = 0.1\text{V}$		200	500		200	500	μA
Input Offset Current	$V_{\text{CM}} = 0.1\text{V}$			50			50	μA
Common Mode Range		0.1		7	0.1		7	V
Open Loop Gain	$V_{\text{CM}} = 1.5\text{V}, \text{Output Voltage } 1 \text{ to } 2.5\text{V}, R_L = 5\text{K}$	60	64		60	64		dB
Unity Gain Bandwidth (Note 6)	$A_{\text{VOL}} = 0\text{dB}$	8	12		8	12		MHz
Output Voltage Slew Rate (Note 6)	See Figure TBD	10	20		10	20		V/ μs
CMRR	$V_{\text{CM}} = 0.1\text{V to } 7\text{V}, C.A_{\text{OUT}} = 2.5\text{V}$	75	100		75	100		dB
PSRR	$V_{\text{IN}} = 13\text{V to } 20\text{V}, V_{\text{CM}} = 0.1$	90			90			dB
Output Sink Current	$C.A_{\text{OUT}} = 2\text{V}, V_{\text{CM}} = 2.5\text{V}, \Delta V = 75\text{mV}$	0.5	1.33		0.5	1.33		mA
Output Source Current	$C.A_{\text{OUT}} = 2\text{V}, V_{\text{CM}} = 2.5\text{V}, \Delta V = 75\text{mV}$	5	10		5	10		mA
Delay to Output (Note 6)	$C.A_{\text{OUT}} = 0.5\text{V to } 2\text{V}, E.A_{\text{OUT}} = 1.5\text{V}$			80			80	ns
Output High Level	$R_L = 5\text{K}$	2.7	3.5		2.7	3.5		V
Output Low Level	$R_L = 5\text{K}$		0.2	0.4		0.2	0.4	V
"Hiccup" Section								
Input Offset Voltage	$R_S \leq 10\Omega, V_{\text{CM}} = 1.7\text{V to } 2.5\text{V}$			10			10	mV
Input Bias Current	$C.A_{\text{OUT}} = 2.5\text{V}, V_{\text{HICCUP}} = 1.7\text{V to } 3.5\text{V}$			10			10	μA
Common Mode Range		1.7		3.5	1.7		3.5	V
Delay to Output (Note 6)	$C.A_{\text{OUT}} = 2.2\text{V}, V_{\text{HICCUP}} = 2\text{V}, E.A_{\text{OUT}} = 2.5\text{V}$	60	650		60	650		ns
Overvoltage/Undervoltage Section								
Overvoltage Threshold Voltage	$I_{\text{REF}} = 1\text{mA}$	4.0	4.2	4.4	4.0	4.2	4.4	V
Overvoltage Hysteresis	$I_{\text{REF}} = 1\text{mA}$	350	450	550	350	450	550	mV
Undervoltage Threshold Voltage	$I_{\text{REF}} = 1\text{mA}$	4.0	4.2	4.4	4.0	4.2	4.4	V
Undervoltage Hysteresis	$I_{\text{REF}} = 1\text{mA}$	660	830	1000	660	830	1000	mV
Delay to Output (Note 6)	$O.V. = V_{\text{REF}} + 0.2\text{V}$		550	800		550	800	ns
O.V. Input Bias Current	O.V. Input = 10V		2	6		2	6	μA
U.V. Input Bias Current	U.V. Input = 10V		2	6		2	6	μA



ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1528/2528 SG1530/2530			SG3528 SG3530			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Section								
Collector Leakage Current	$V_C = 20V$, Output off			0.5			0.5	mA
Output High Level	$I_{SOURCE} = 50mA$	13	13.5		13	13.5		V
	$I_{SOURCE} = 200mA$	12.5	13.5		12.5	13.5		V
Output Low Level	$I_{SINK} = 50mA$		0.3	0.5		0.3	0.5	V
	$I_{SINK} = 200mA$		1	2		1	2	V
Maximum Duty Cycle (Note 8)	$E.A_{OUT} = 2V$, $C.A_{OUT} = 1.5V$	45	48	51	45	48	51	%
Zero Duty Cycle	$E.A_{OUT} = 0.5V$, $C.A_{OUT} = 0.6V$			0			0	%
Rise Time (Note 6)	$C_L = 1nF$		25	50		25	50	ns
Fall Time (Note 6)	$C_L = 1nF$		20	50		20	50	ns
Bleeding Resistor	Tristate Output, $V_{IN} = 11V$ (Note 6)	10		60	10		60	KΩ
Cross Conduction Current (Note 6)	$C_L = 1nF$		6	60		6	60	nJ/Hz
Start Up Section								
Start Up Voltage		15.5	16	16.5	15.5	16	16.5	V
Start Up Current	$V_{IN} =$ Start-Up Threshold		350	600		350	600	μA
Shut Down Voltage		11.5	12	12.5	11.5	12	12.5	V
Delay to Output on Shut Down	Output Low, $V_{IN} = 11V$ (Note 6)		150	300		150	300	ns
Soft-Start Section								
Soft Start Charging Current	$V_{SOFTSTART} = 0.5V$, $V_{HICCUP} = 4V$	35	45	55	35	45	55	μA
Soft Start Discharge Current	$V_{SOFTSTART} = 11V$, $V_{IN} = 11V$	30			30			mA
Soft Start Discharge Voltage	$I_{DISCHARGE} = 30mA$			2			2	V
Power Consumption Section								
Total Supply Current	$f_o = 200KHz$, $C_L = 1000pF$		35	50		35	50	mA
Standby Current	$V_{UV} = 3.5V$			20			20	mA

Note 4. Performance data described herein represent design goals. Final device specifications are subject to change.
 Note 5. Adjust V_{IN} above the start threshold before setting it to 15V.
 Note 6. This parameter, although guaranteed, is not tested in production.

Note 7. This parameter is non-accumulative, and represents the random fluctuation of the reference voltage within some error band when observed over any 1000 hour period of time.
 Note 8. $F_{OSC} = 1MHz$ ($R_T = TBD$, $C_T = TBD$)
 Note 9. $C.A. - = 1.1V$, $C.A. + = 1V$
 Note 10. $E.A. - = 2.5V$, $E.A. + = 2.4V$

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1528J/883B SG1528J SG2528J SG3528J SG1530J/883B SG1530J SG2530J SG3530J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2528DW SG3528DW SG2530DW SG3530DW	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	

Notes: 1. Contact factory for JAN and DESC product availability.
 2. All parts are viewed from the top.

3. Product is also available in leadless chip carrier (LCC) and 24-pin hermetic flat pack (F). Contact factory for price and availability.