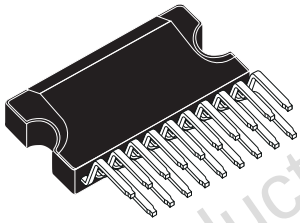
STA540SA

4 x 10-watt dual/quad power amplifier

Features

- High output-power capability:
  - 4 x 9 W / 2 Ω at 12 V, 1 kHz, 10 %
  - 4 x 10 W / 4 Ω at 17 V, 1 kHz, 10 %
  - 2 x 26 W / 4 Ω at 14.4 V, 1 kHz, 10 %
  - 2 x 15 W / 8 Ω at 16 V, 1 kHz, 10 %
- Minimum external components count:
  - No bootstrap capacitors
  - No Boucherot cells
  - Internally fixed gain of 20 dB
- Standby function (CMOS compatible)
- No audible pop during standby operations
- Diagnostic facilities:
  - Clip detector
  - Out to GND short circuit
  - Out to VS short circuit
  - Soft short at turn-on
  - Thermal shutdown proximity
- Protection for
  - Output AC/DC short circuit
  - Soft short circuit at turn-on



Clipwatt19

  - Thermal cut-off limiter to prevent chip from overheating
  - High inductive loads
  - ESD

Description

The amplifier is a class AB audio amplifier assembled in the Clipwatt19 package and designed for high-quality sound applications.

The STA540SA is a 4-channel single-ended amplifier with integrated short-circuit protection, thermal protection and diagnostic functions.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STA540SA	0 to 70 °C	Clipwatt19	Tube

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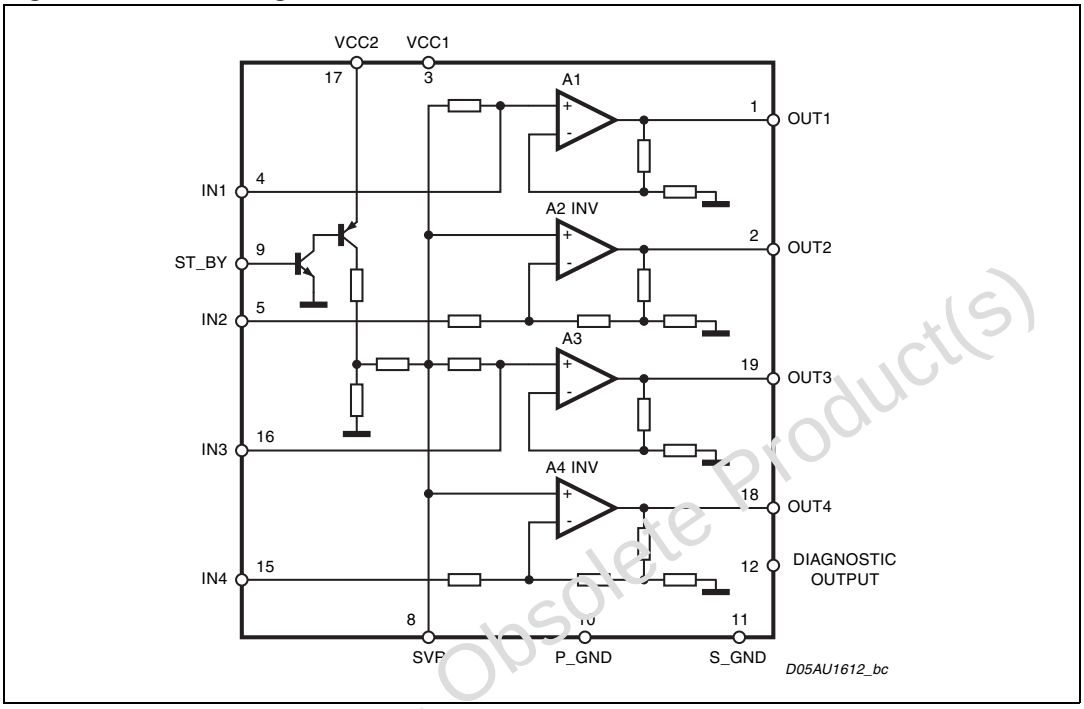
1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection (top view)

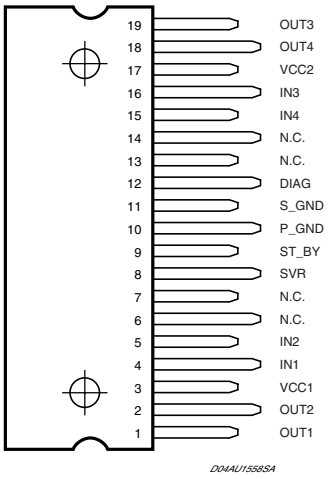


Table 2. Pin description

Pin	Name	Type	Function
1	OUT1	OUTPUT	Channel 1 output
2	OUT2	OUTPUT	Channel 2 output
3	VCC1	POWER	Power supply
4	IN1	INPUT	Channel 1 input
5	IN2	INPUT	Channel 2 input
6	N.C.	-	Not connected
7	N.C.	-	Not connected
8	SVR	INPUT	Supply voltage rejection
9	ST_BY	INPUT	Standby control pin
10	P_GND	POWER	Power ground
11	S_GND	POWER	Signal ground
12	DIAG	OUTPUT	Diagnostics
13	N.C.	-	Not connected
14	N.C.	-	Not connected
15	IN4	INPUT	Channel 4 input
16	IN3	INPUT	Channel 3 input
17	VCC2	POWER	Power supply
18	OUT4	OUTPUT	Channel 4 output
19	OUT3	OUTPUT	Channel 3 output

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_s	Supply voltage idle mode (no signal)	24	V
	Supply voltage operating	22	V
	Supply voltage AC-DC short safe	20	V
P_{tot}	Total power dissipation (T_{case} = 70 °C)	35	W
T_{stg}, T_j	Storage and junction temperature	-40 to150	°C
T_{op}	Operating temperature	0 to 70	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	-	-	2.5	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	-	-	45	°C/W

3.3 Electrical characteristics

Refer to the test circuit, V_S = 15V, R_L = 4 Ω, f = 1 kHz, T_{amb} = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_s	Supply voltage range	-	8	-	22	V
I_d	Total quiescent drain current	-	-	80	150	mA
V_{os}	Output offset voltage	-	-250	-	250	mV
P_o	Output power	THD = 10 %	6.5	7.5	-	W
		THD = 10 %, V_S = 17 V S.E. R_L = 4 Ω	-	10	-	W
		THD = 10 %, V_S = 17 V BTL, R_L = 8 Ω	-	20	-	W
THD	Distortion	R_L = 4 Ω, P_o = 0.1 to 4 W	-	0.02	-	%
I_{SC}	Short-circuit current	-	-	3.5	-	A
C_T	Crosstalk	f = 1 kHz f = 10 kHz	-	70 60	-	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
R_{in}	Input impedance	-	20	30	-	kΩ
G_v	Voltage gain	-	19	20	21	dB
G_v	Voltage gain match	-	-	-	0.5	dB
E_N	Total output noise	Rg = 0, “A” weighted Inverting channels: Non-inverting channels:	 - -	 50 20	 - -	µV
SVR	Supply voltage rejection	Rg = 0, f = 300 Hz, C_{SVR} = 470 µF	50	-	-	dB
A_{SB}	Standby attenuation	-	80	90	-	dB
I_{SB}	ST_BY current consumption	V_{ST_BY} = 0 to 1.5 V	-	-	100	µA
V_{SB}	ST_BY IN threshold voltage	-	-	-	1.5	V
V_{SB}	ST_BY OUT threshold voltage	-	3.5	-	-	V
I_{ST_BY}	ST_BY pin current	Play mode V_{ST_BY} = 5 V	-	-	50	µA
		Driving current under fault	-	-	5	mA
$I_{cd\ off}$	Clipping detector output average current	d = 1 % (1)	-	90	-	µA
$I_{cd\ on}$	Clipping detector output average current	d = 5 % (1)	-	160	-	µA
V_{DIAG}	Voltage saturation on DIAG	Sink current at I_{DIAG} = 1 mA	-	-	0.7	V
T_W	Thermal warning	-	-	140	-	°C
T_M	Thermal muting	-	-	150	-	°C
T_S	Thermal shutdown	-	-	160	-	°C

1. Pin DIAG pulled-up to 5 V with 10 kΩ

4 Test and application board

This section includes information about the test and application board including the test circuit, board layout, and parts list.

Figure 3. Test and application board

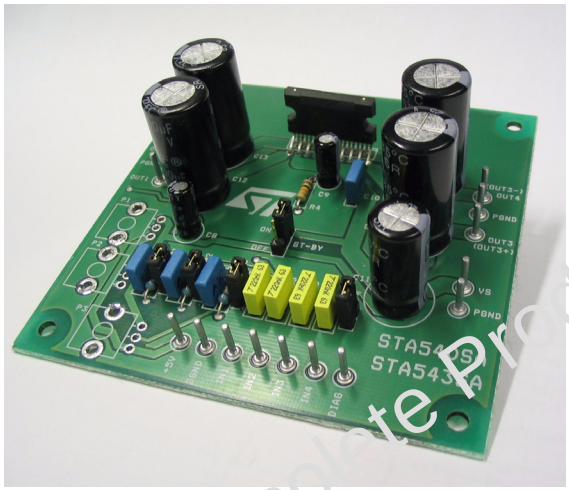
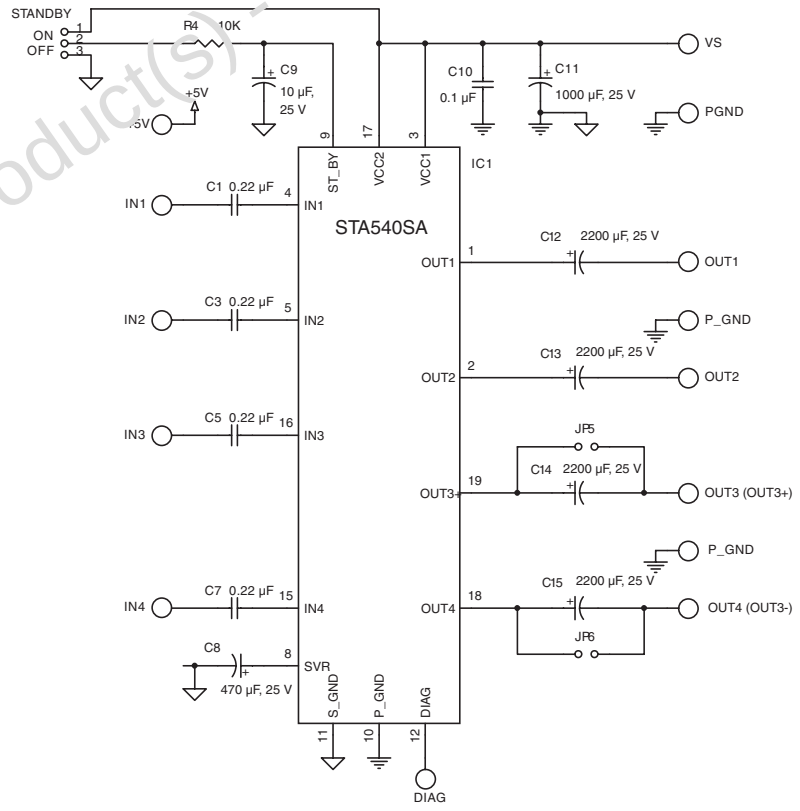


Figure 4. Test circuit



4.1 Board layout

Figure 5. Component layout

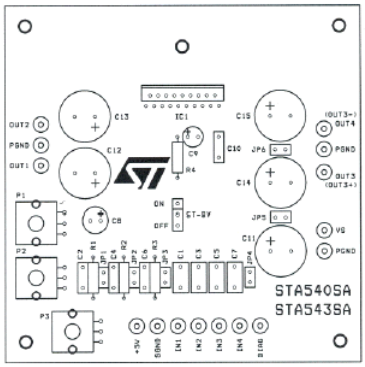


Figure 6. Component side

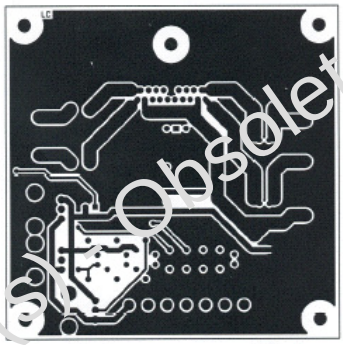
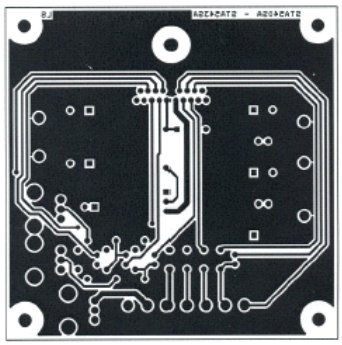


Figure 7. Solder side



4.2 Parts list

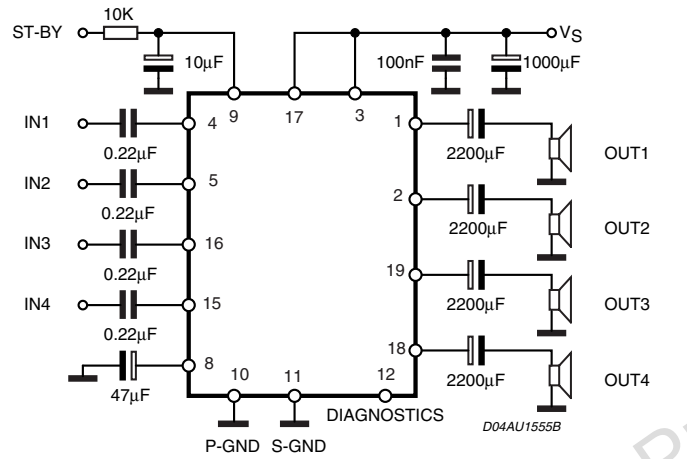
Table 6. Components

Components	Suggested value	Purpose
R4	10 kΩ	Standby time constant
C1, C3, C5, C7	0.22 µF	Input AC coupling
C8	470 µF	Ripple rejection
C9	10 µF	Standby time constant
C10	0.1 µF	Supply voltage bypass
C11	1000 µF	Supply voltage bypass
C12, C13, C14, C15	2200 µF	Output AC coupling

*Note: The application board is designed to also test the STA543SA device. Therefore, the following components must **not** be mounted for the STA540SA: R1, R2, R3, P1, P2, and P3.*

5 Standard applications circuits

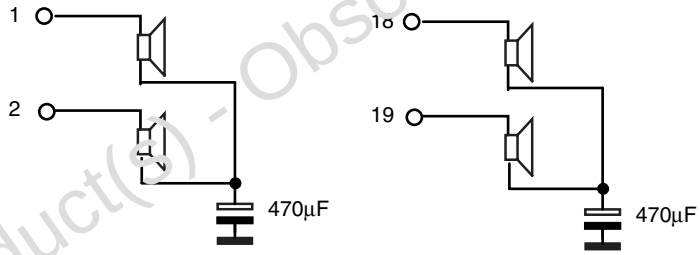
Figure 8. Quad stereo



Suggested applications:

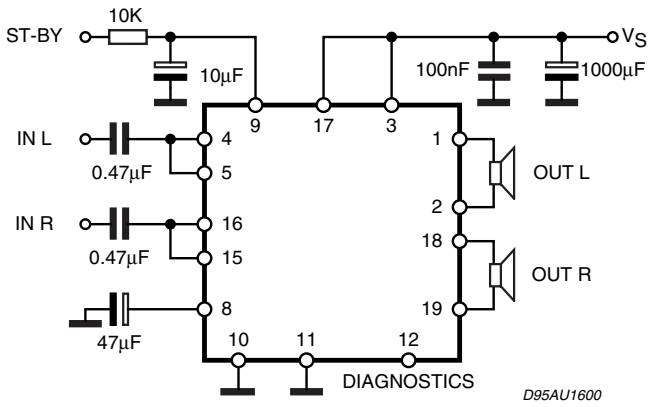
4 x 12 W at 2 Ω, 14.4 V
4 x 10 W at 4 Ω, 17 V
4 x 9 W at 2 Ω, 12 V
4 x 5 W at 4 Ω, 12 V

Figure 9. Audio performance option



The best audio performance is obtained with the configuration where each speaker has its own DC blocking capacitor. If the application allows a little degradation of the spatial image it is possible to connect a couple of speakers with only one low-value DC blocking capacitor.

Figure 10. Double bridge

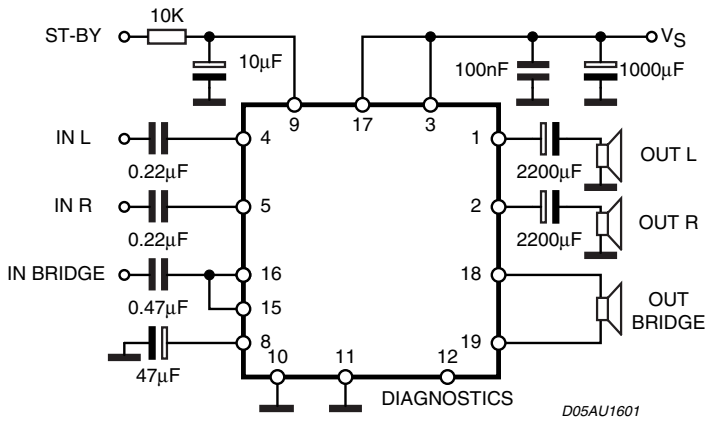


Suggested applications:

2 x 9 W at 8 Ω, 12 V
2 x 18 W at 4 Ω, 12 V
2 x 13 W at 8 Ω, 14 V
2 x 26 W at 8 Ω, 14 V
2 x 15 W at 8 Ω, 16 V

A dedicated evaluation board is available for this application (see *Section 9 on page 24*).

Figure 11. Stereo Bridge



Suggested applications:

2 x 9 W into 2 Ω + 1 x 18 W into 4 Ω, 12 V
2 x 12 W into 2 Ω + 1 x 26 W into 4 Ω, 14.4 V
2 x 8 W into 4 Ω + 1 x 16 W into 8 Ω, 13 V

A dedicated evaluation board is available for this application (see *Section 9 on page 24*).

6 Electrical characteristics curves

Figure 12. Quiescent drain current vs supply voltage (single-ended and bridge)

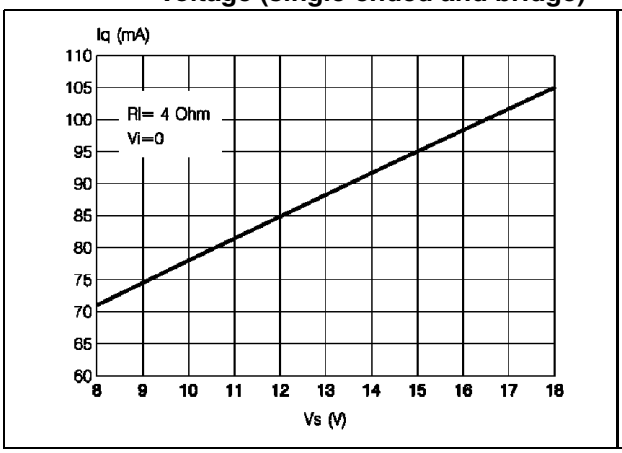


Figure 13. Quiescent output voltage vs supply voltage (single-ended and bridge)

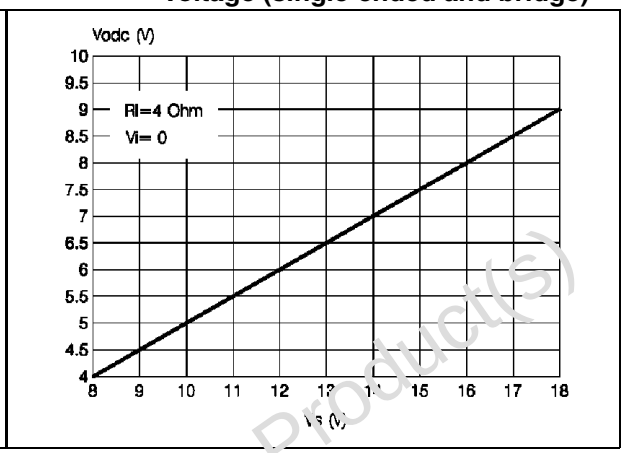


Figure 14. Output power vs supply voltage

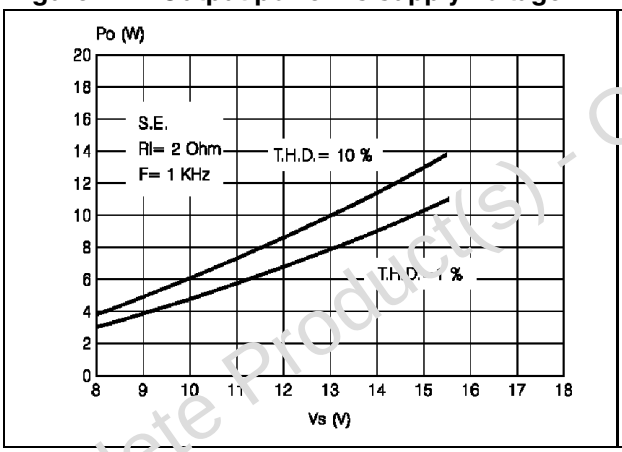


Figure 15. Distortion vs output power

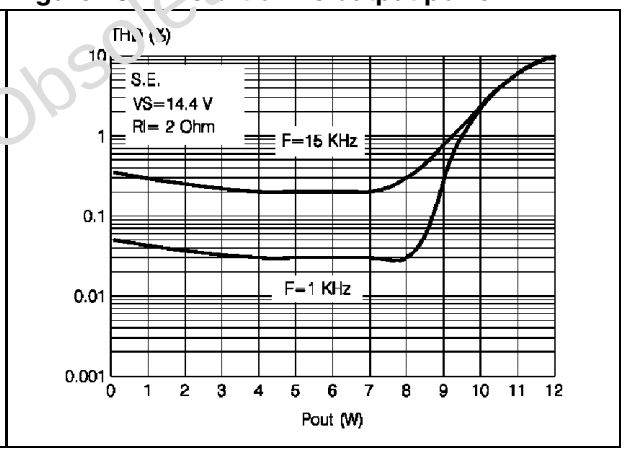


Figure 16. Output power vs supply voltage

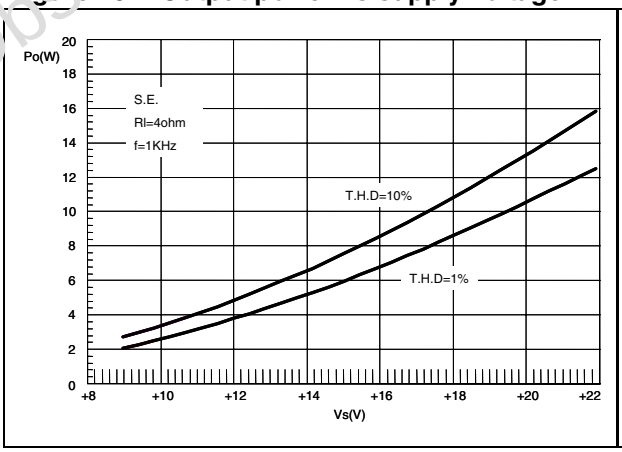


Figure 17. Distortion vs output power

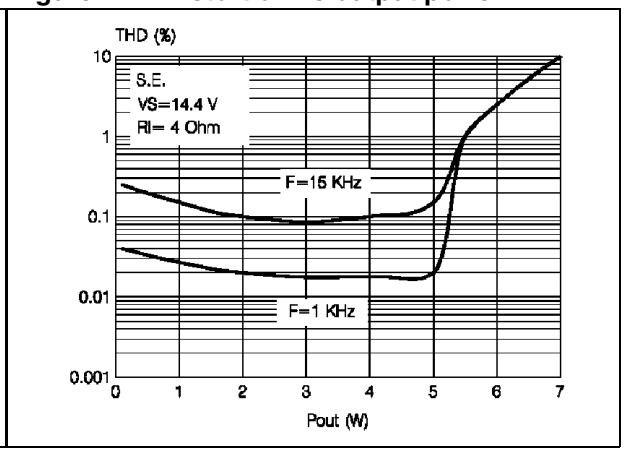


Figure 18. Output power vs supply voltage

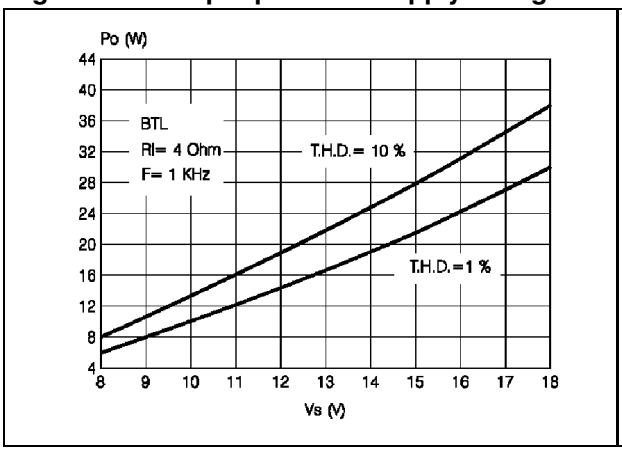


Figure 19. Distortion vs output power

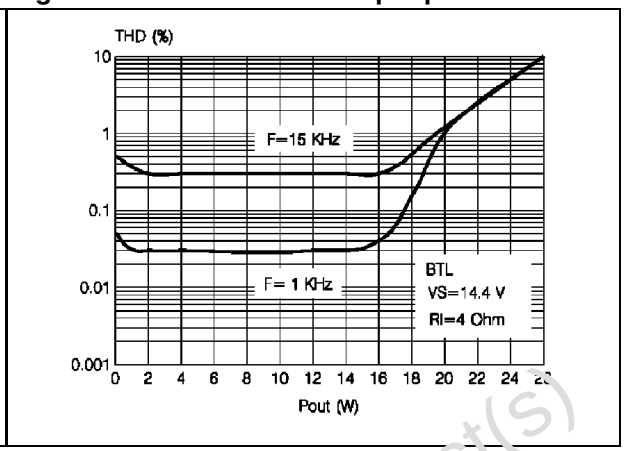


Figure 20. Output power vs supply voltage

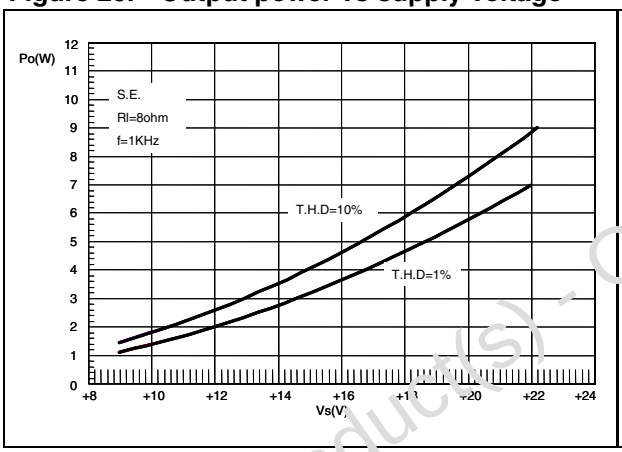


Figure 21. Crosstalk vs frequency

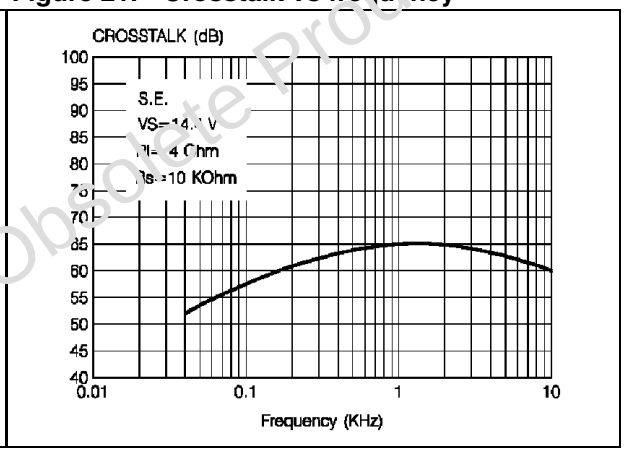


Figure 22. Output power vs voltage

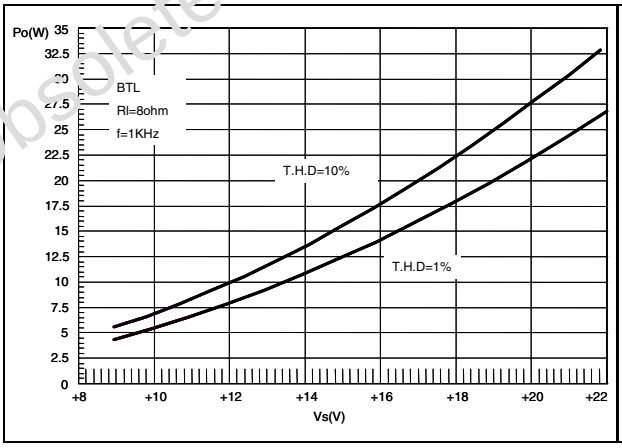


Figure 23. Standby attenuation vs threshold voltage

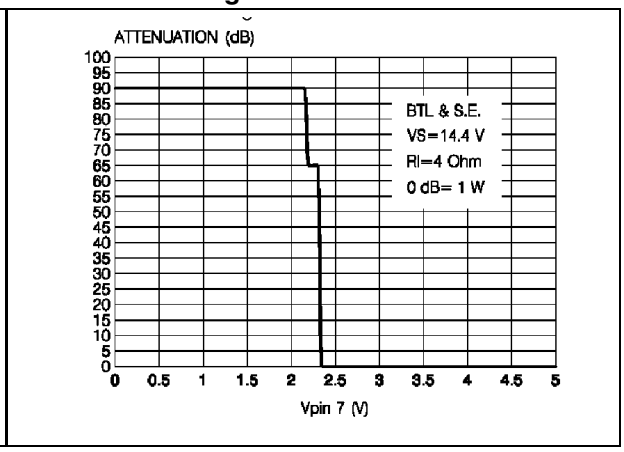


Figure 24. Supply voltage rejection vs frequency

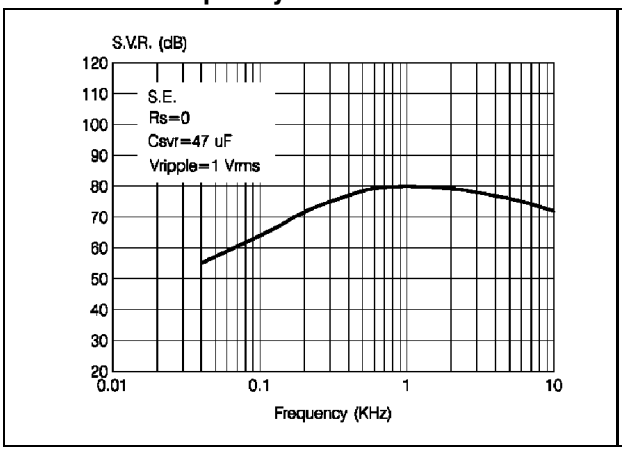


Figure 25. Total power dissipation and efficiency vs output power

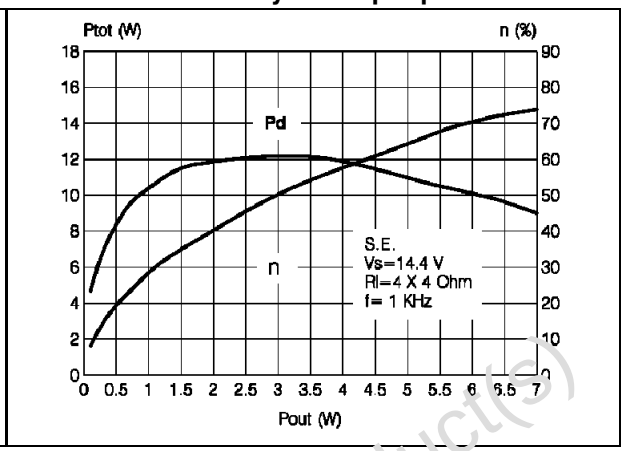
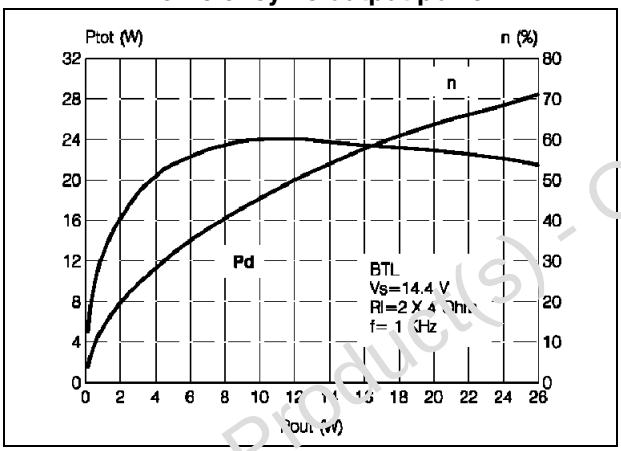


Figure 26. Total power dissipation and efficiency vs output power



7 Thermal information

In order to avoid the thermal protection intervention that is placed at T_j =150 °C (thermal muting) or T_j=160 °C (thermal shutdown), it is important to design the heatsink R_{th} (°C/W) value correctly.

The parameters that influence the design are:

- Maximum dissipated power for the device (P_{dmax})
- Maximum thermal resistance junction to case ($R_{th\_j\text{-}case}$)
- Maximum ambient temperature T_{amb_max}

There is also an additional term that depends on the quiescent current, Iq, but this is negligible in this case.

Example 1: 4-channel single-ended amplifier

V_{CC} =14.4 V, R_L = 4 Ω x 4 channels, $R_{th\_j\text{-}case}$ = 2.5 °C/W, T_{amb_max} = 50 °C, P_{out} = 4 x 7 W

$$P_{dmax} = NChannel \cdot \frac{V_{CC}^2}{2\Pi^2 R_L} = 4 \cdot 2.62 = 10.5W$$

The required thermal resistance for the heatsink is

$$R_{th\_c\text{-}amb} = \frac{150 - T_{amb\_max}}{P_{dmax}} - R_{th\_j\text{-}case} = \frac{150 - 50}{10.5} - 2.5 = 7°C/W$$

Example 2: 2-channel single-ended plus 1-channel (BTL) amplifier

V_{CC} = 14.4 V, R_L = 2 x 2 Ω (SE) + 1 x 4 Ω (BTL), P_{out} = 2 x 12 W + 1 x 26 W

$$P_{dmax} = 2 \cdot \frac{V_{CC}^2}{2\Pi^2 R_L} + \frac{2V_{CC}^2}{\Pi^2 R_L} = 2 \cdot 5.25 + 10.5 = 21W$$

The required thermal resistance for the heatsink is

$$R_{th\_c\text{-}amb} = \frac{150 - T_{amb\_max}}{P_{dmax}} - R_{th\_j\text{-}case} = \frac{150 - 50}{21} - 2.5 = 2.2°C/W$$

Design notes on examples 1 and 2

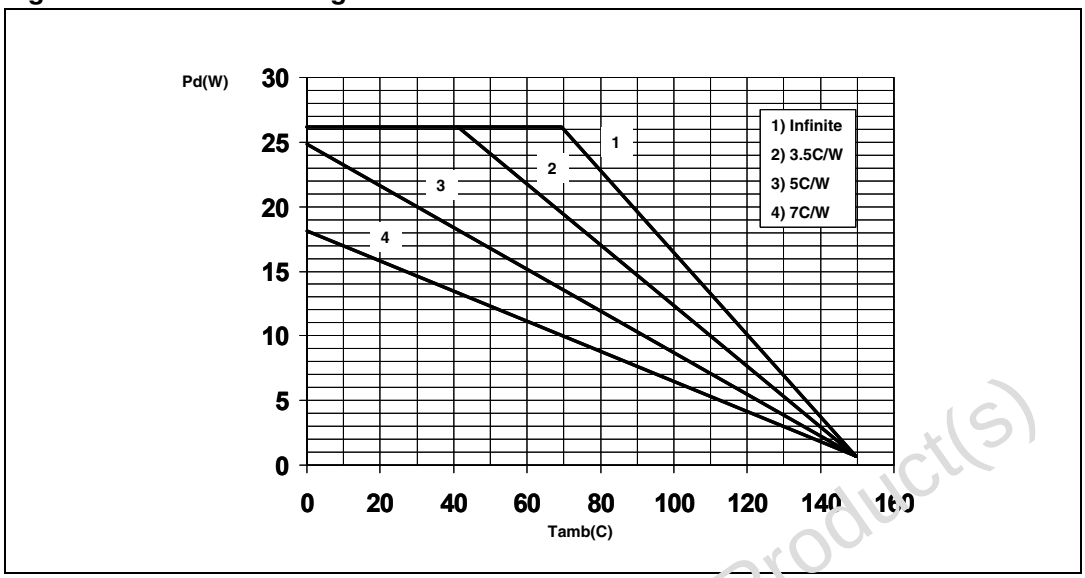
The values found give a heatsink that is designed to sustain the maximum dissipated power. But as explained in the applications note (AN1965) the heatsink can be smaller when a realistic application is considered where a musical program is used.

When the average listening power concept is considered, the dissipated power is about 40% less than the P_{dmax}. Therefore, in examples 1 and 2, the resulting average dissipated power is reduced as follows:

– Example 1: 10.5 W - 40% = 6.3 W giving $R_{th\_c\text{-}amb}$ = 13.4 °C/W
– Example 2: 21 W - 40% = 12.6 W giving $R_{th\_c\text{-}amb}$ = 5.4 °C/W

Figure 27 below shows the power derating curve for the device.

Figure 27. Power derating curve



8 General structure

8.1 High application flexibility

The availability of four independent channels makes it possible to accomplish several kinds of applications ranging from four-speaker stereo (F/R) to two-speaker bridge solutions.

When working with single-ended conditions, the polarity of the speakers driven by the inverting amplifier must be reversed with respect to those driven by non-inverting channels. This is to avoid phase irregularities causing sound alterations especially during the reproduction of low frequencies.

8.2 Easy single-ended to bridge transition

The change from single-ended to bridge configurations is made simple by means of a short circuit across the inputs (resulting in no need of additional external components).

8.3 Internally fixed gain

The gain is internally fixed to 20 dB in single-ended mode and 26 dB in bridge mode.

The advantages of this design choice are in terms of:

- components and space saving
- output noise, supply voltage rejection and distortion optimization.

8.4 Silent turn on/off and muting/standby functions

Standby mode can be easily activated by means of a CMOS logic level applied to pin 9 through a RC filter.

Under standby conditions, the device is turned off completely (supply current = 1 mA typical, output attenuation = 80 dB minimum).

All on/off operations are virtually pop-free. Furthermore, at turn-on the device stays in mute condition for a time determined by the value assigned to the SVR capacitor. In mute mode, the device outputs are insensitive to any kind of signal that may be present at the input terminals. In other words, any transients coming from previous stages produce no unpleasant acoustic effects at the speakers.

8.5 Standby driving (pin 9)

Some precautions need to be taken when defining standby driving networks. Pin 9 cannot be directly driven by a voltage source having a current capability higher than 5 mA. In practical cases a series resistance must be inserted, giving it the double purpose of limiting the current at pin 9 and smoothing down the standby on/off transitions. And, when done in combination with a capacitor, prevents output pop.

A capacitor of at least 100 nF from pin 9 to S_GND, with no resistance in between, is necessary to ensure correct turn-on.

8.6 Output stage

The fully complementary output stage is possible with the power ICV PNP component.

This novel design is based on the connection shown in *Figure 28* and allows the full exploitation of its capabilities. The clear advantages this new approach has over classical output stages are described in the following sections.

8.6.1 Rail-to-rail output voltage swing with no need of bootstrap capacitors

The output swing is limited only by the V_{CEsat} of the output transistors, which are in the range of 0.3 Ω (R_{sat}) each.

Classical solutions adopting composite PNP-NPN for the upper output stage have higher saturation loss on the top side of the waveform.

This unbalanced saturation causes a significant power reduction. The only way to recover power includes the addition of expensive bootstrap capacitors.

8.6.2 Absolute stability without any external compensation

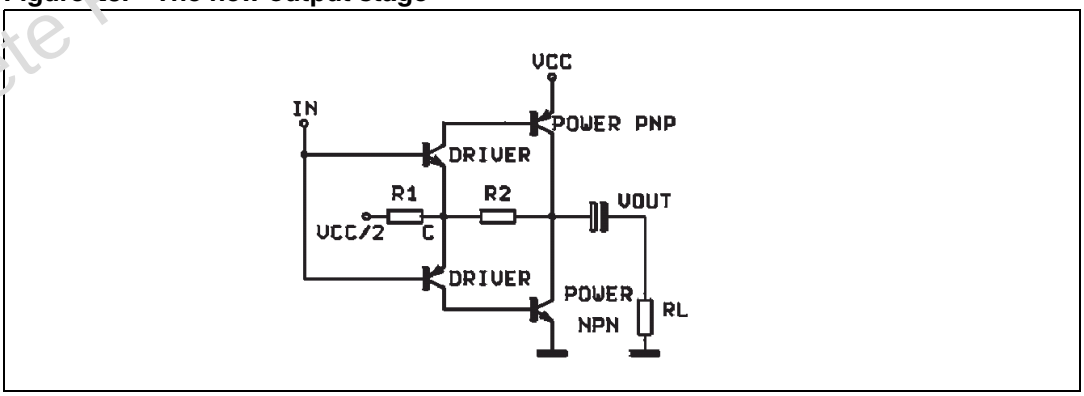
With reference to the circuit shown in *Figure 28*, the gain V_{out}/V_{in} is greater than unity, that is, approximately 1+R2/R1. The DC output ($V_{CC}/2$) is fixed by an auxiliary amplifier common to all the channels.

By controlling the amount of this local feedback, it is possible to force the loop gain (A*β) to less than unity at a frequency where the phase shift is 180 °. This means that the output buffer is intrinsically stable and not prone to oscillation.

The above feature has been achieved even though there is very low closed-loop gain of the amplifier.

This is in contrast with the classical PNP-NPN stage where the solution adopted for reducing the gain at high frequencies makes use of external RC networks, namely the Boucherot cells.

Figure 28. The new output stage



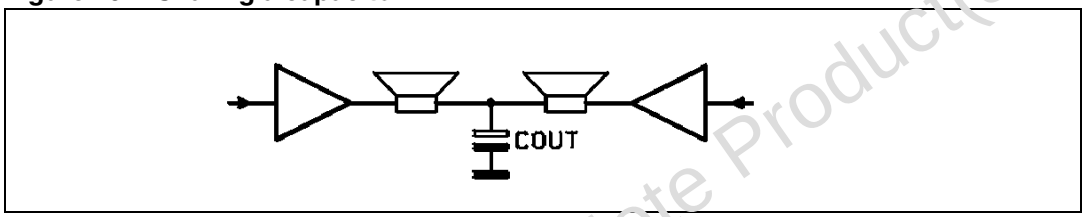
8.7 Built-in short-circuit protection

Reliable and safe operation in the presence of all kinds of short circuits involving the outputs is assured by built-in protection. Additionally, a soft short-condition is signalled out (to the AC/DC short circuit to GND, to VS, and across the speaker) during the turn-on phase to ensure correct operation of the device and the speakers.

This particular kind of protection acts in such a way as to prevent the device being turned on (by ST_BY) when a resistive path (less than 16 Ω) is present between the output and GND. It is important to have the external current source driving the ST_BY pin limited to 5 mA. This is because the associated circuitry is normally disabled with currents >5 mA.

This extra function becomes particularly attractive when, in the single-ended configuration, one capacitor is shared between two outputs as shown in *Figure 29*.

Figure 29. Sharing a capacitor



If the output capacitor C_{out} is shorted for any reason, the loudspeaker is not damaged.

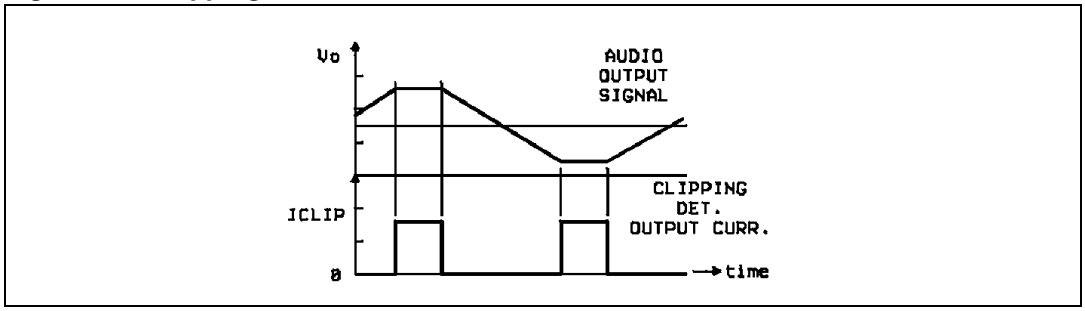
8.7.1 Diagnostic facilities (pin 12)

The STA540SA is equipped with diagnostic circuitry that is able to detect the following events:

- Clipping in the output signal
- Thermal shutdown
- Output fault:
  - short to GND
  - short to VS
  - soft short at turn on

The information is available across an open collector output (pin 12) through a current sinking when the event is detected.

Figure 30. Clipping detection waveforms



A current sinking at pin 12 is provided when a certain distortion level is reached at each output. This function initiates a gain-compression facility whenever the amplifier is overdriven.

8.7.2 Thermal shutdown

With the thermal shutdown feature, the output (pin 12) signals the proximity of the junction temperature to the shutdown threshold. Typically, current sinking at pin 12 starts at approximately 10 °C before the shutdown threshold is reached.

Figure 31. Output fault waveforms

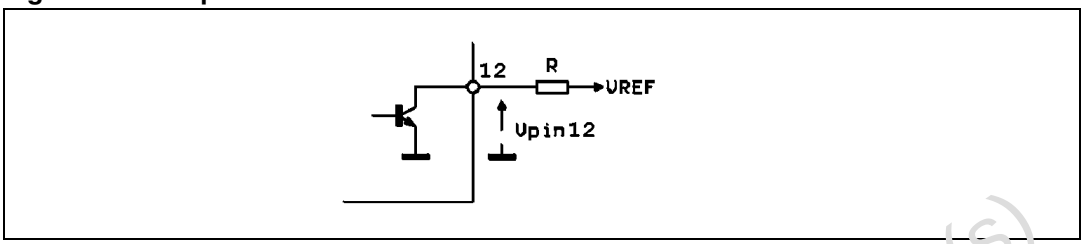
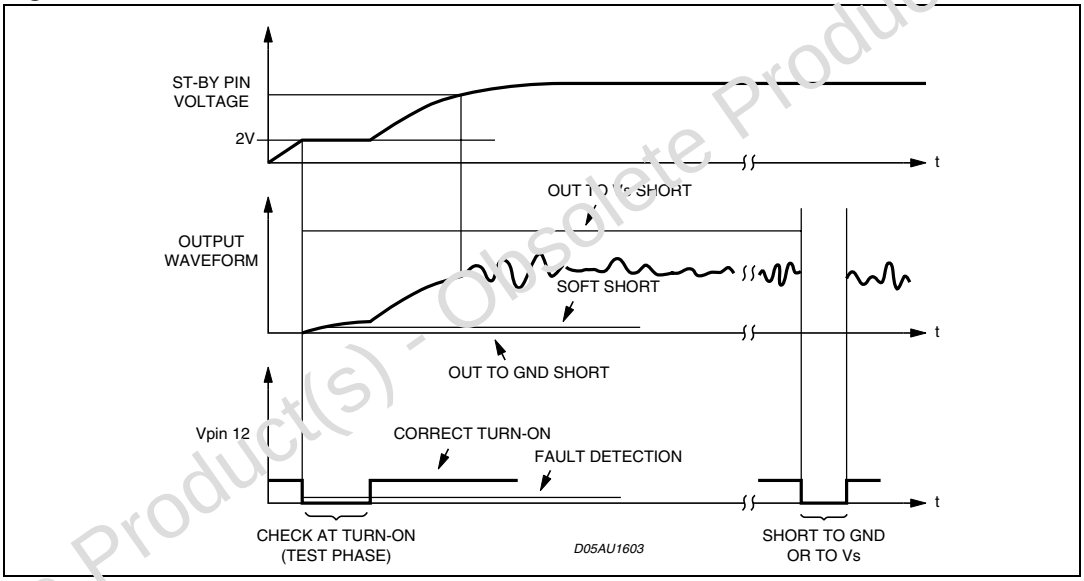


Figure 32. Fault waveforms



8.8 Handling of the diagnostic information

As different diagnostic information is available at the same pin (clipping detection, output fault, thermal proximity), the signal must be handled correctly in order to discriminate the event. This could be done by taking into account the different timing of the diagnostic output during each case.

Normally, clip-detector signalling under faulty conditions produces a low level at pin 12. Based on this assumption, an interface circuitry to differentiate the information is shown in *Figure 34*.

Figure 33. Waveforms

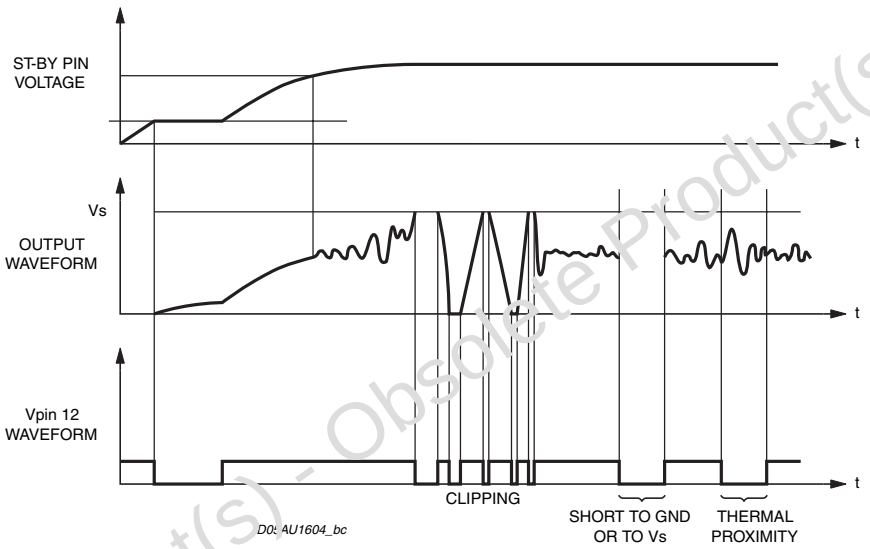
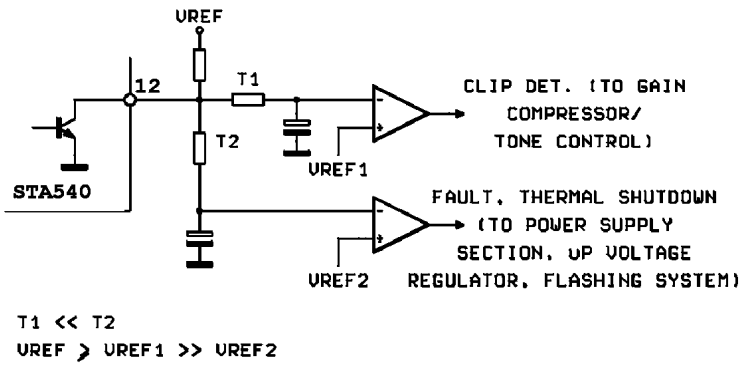


Figure 34. Interface circuit diagram



8.9 PCB-layout grounding (general rules)

The device has two distinct ground leads, P_GND (power ground) and S_GND (signal ground) which are practically disconnected from each other at chip level. Correct operation requires that P_GND and S_GND leads be connected together on the PCB layout by means of reasonably low-resistance tracks.

For the PCB ground configuration a star-like arrangement, where the center is represented by the supply-filtering electrolytic capacitor ground, is recommended. In such context, at least two separate paths must be provided; one for power ground and one for signal ground.

The correct ground assignments are as follows:

- standby capacitor (pin 9, or any other standby driving networks): on signal ground
- SVR capacitor (pin 8): on signal ground and to be placed as close as possible to the device
- input signal ground (from active/passive signal processor stages): on signal ground
- supply filtering capacitors (pins 3 and 17): on power ground. The negative terminal of the electrolytic capacitor must be directly tied to the battery negative line and this should represent the starting point for all the ground paths.

9 Demonstration boards and applications suggestions

In addition to the test and applications board shown in *Figure 3 on page 8*, two demonstration boards are also available:

- STA540SA-2.1CH Eval-Board
- STA540SA-BTL Eval-Board

These two evaluation boards are briefly described in the following section.

Note: The test and application board shown in Figure 3 on page 8 is common to the STA543 amplifier and is intended to verify all the possible application configurations offered by the STA540SA.

9.1 STA540SA-2.1CH evaluation board

This board is intended to debug the 2.1-channel application. The schematic is shown in *Figure 35* and the PCB / components layout is shown in *Figure 36*.

Figure 35. STA540SA-2.1CH evaluation board

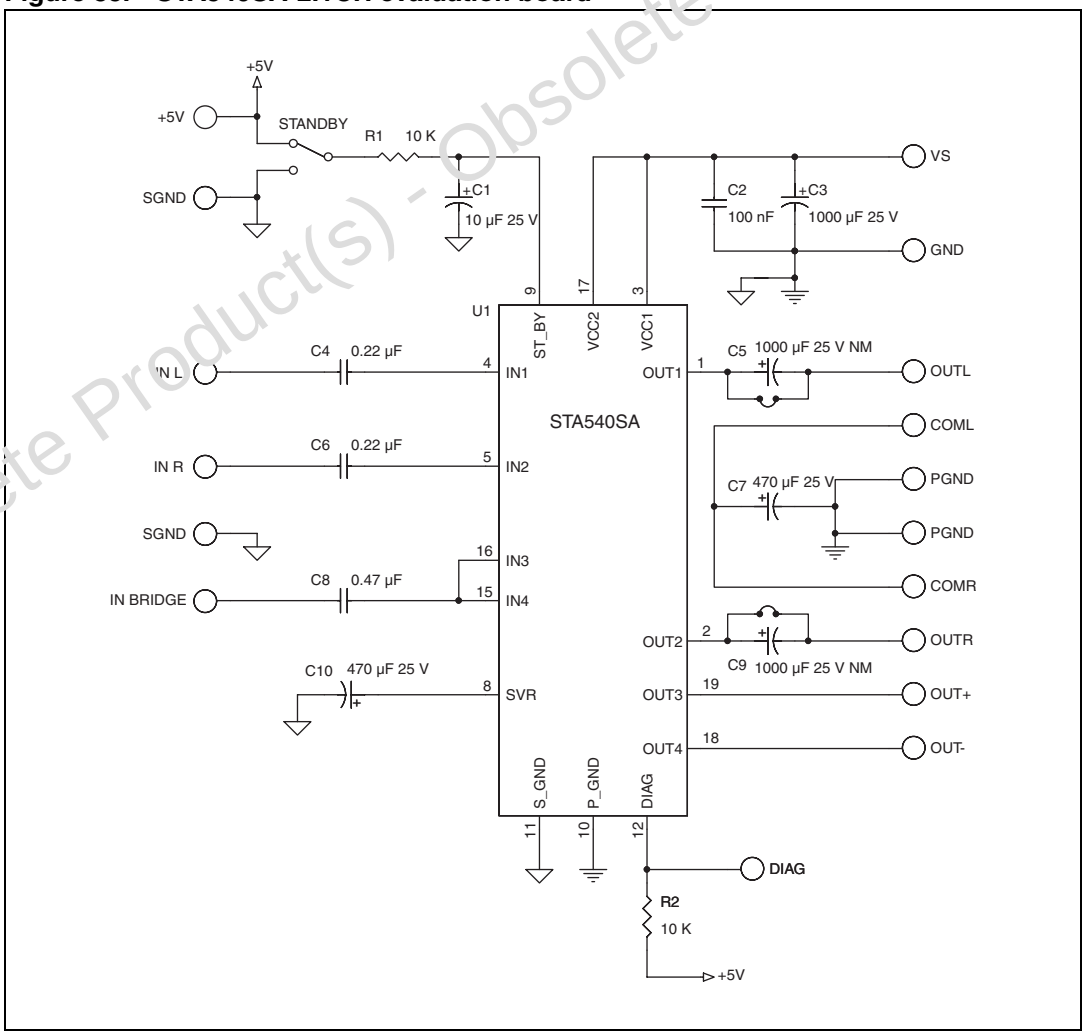
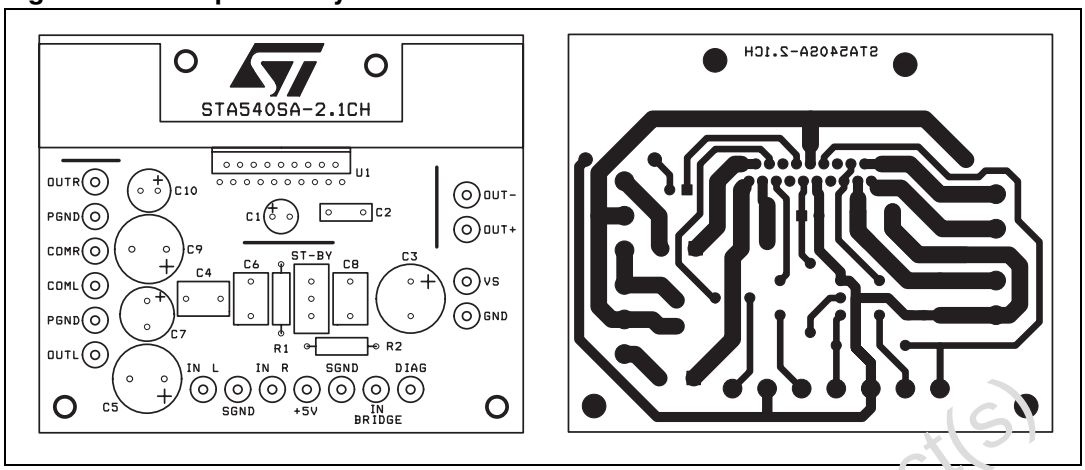


Figure 36. Component layout



With this board, it is possible to connect the left and right speakers in two different ways as shown in *Figure 9 on page 11*.

1. Using the output terminals OUTR / OUTL and P-GND. With this configuration the two jumpers are open and the 1000 µF DC decoupling capacitors (C5, C9) are inserted in series to the load.
2. Using the configuration with one capacitor (470 µF) shared between the two outputs.

For this solution, the jumpers must be closed (C5, C9 are bypassed) and the left and right speakers must be connected between the output terminals OUTR / OUTL and COMR / COML respectively.

Additionally, a switch is available on this board to test the standby function and a test point (DIAG) where it is possible to verify the diagnostic feature (see *Section 8.7 on page 20*).

9.2 STA540SA-BTL evaluation board

This board is intended to debug the double-bridge application. The schematic is shown in *Figure 37* and the PCB / components layout is shown in *Figure 38*.

Figure 37. STA540SA-BT evaluation board

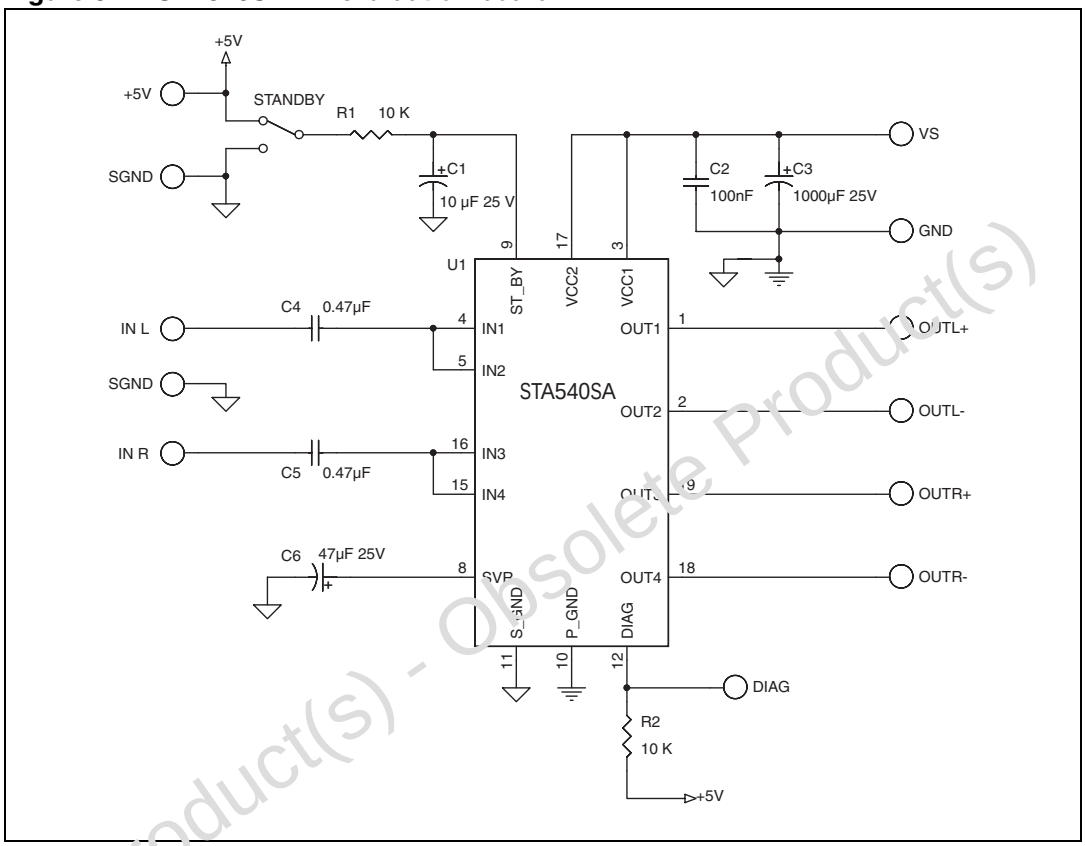
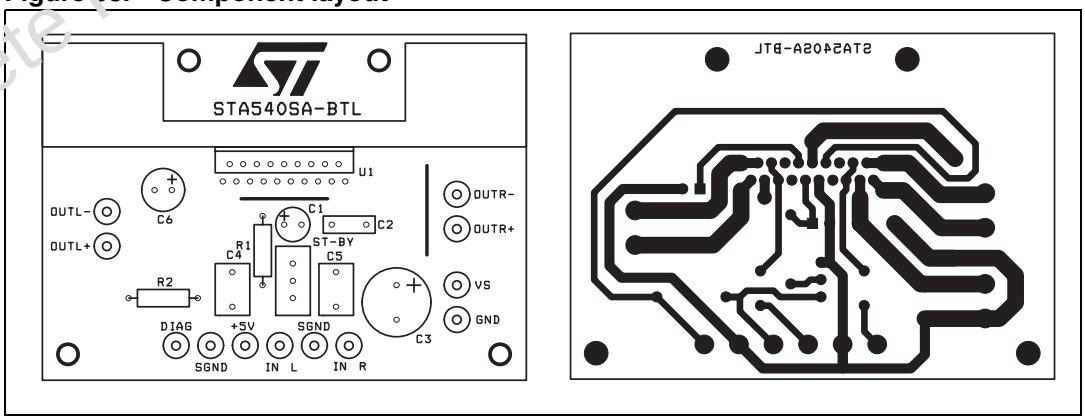


Figure 38. Component layout



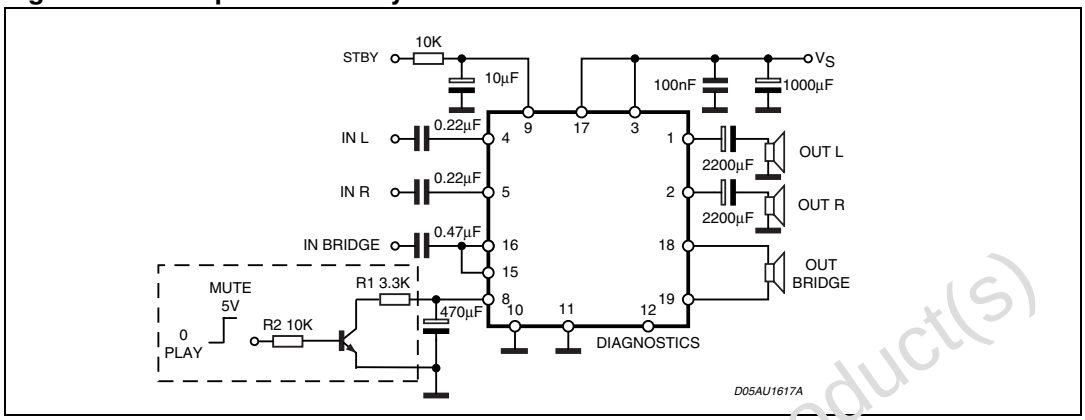
With this board, the left and right speakers are connected in a BTL allowing the implementation of a high-power stereo application with few external components.

Additionally, a switch is available on this board to test the standby function and a test point (DIAG) where it is possible to verify the diagnostic feature (see *Section 8.7 on page 20*).

9.3 Mute function

If the mute function is required, it can be accessed on SVR (pin 8) as shown in *Figure 39*.

Figure 39. Components for layout



V_S = 10 to 16 V, V_{SVR}: mute off ≥ 0.6 to 0.8, mute on ≥ 0.2 V

Using a different value for R1 than the suggested 3.3 kΩ, results in two different situations:

- R1 > 3.3 kΩ:
  - Pop noise improved
  - Lower mute attenuation
- R1 < 3.3 kΩ:
  - Pop noise degradation
  - Higher mute attenuation

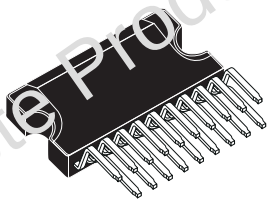
10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

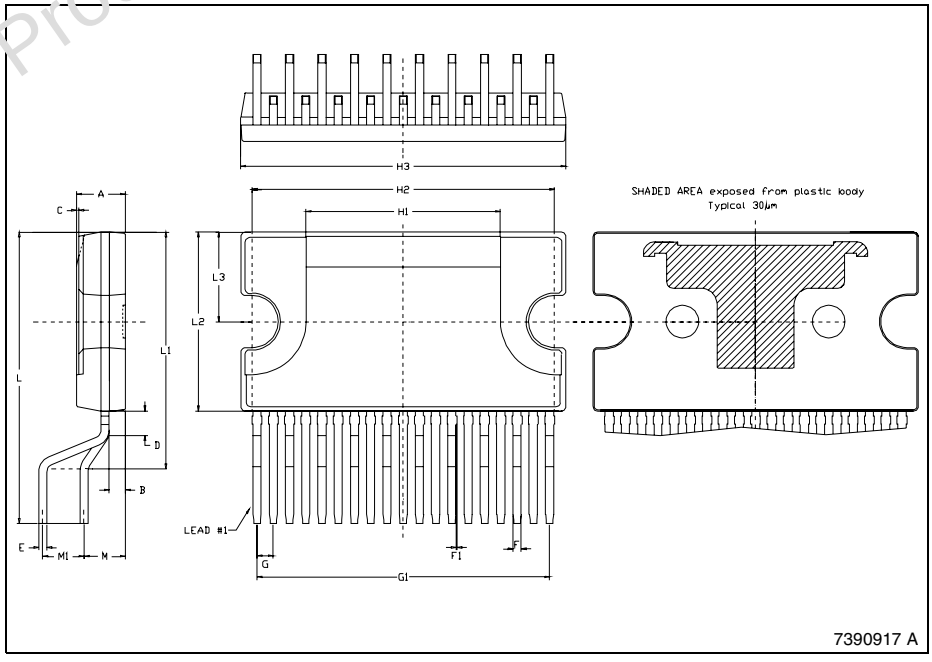
Figure 40. Mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.2			0.126
B			1.05			0.041
C		0.15			0.006	
D		1.50			0.061	
E	0.49		0.55	0.019		0.022
F	0.47	0.50	0.58	0.018		0.020
F1			0.1			0.004
G	0.87	1.00	1.13	0.034	0.039	0.044
G1	17.87	18.0	18.13	0.703	0.708	0.713
H1		12.0			0.480	
H2		18.6			0.732	
H3	19.85			0.781		
L		17.9			0.704	
L1		14.55			0.572	
L2	10.7	11.0	11.2	0.421	0.433	0.441
L3		5.50			0.217	
M		2.54			0.100	
M1		2.54			0.100	

OUTLINE AND MECHANICAL DATA



Clipwatt19



11 Revision history

Table 7. Document revision history

Date	Revision	Changes
Dec-2005	1	Initial release
09-Dec-2010	2	Updated presentation to current template Additional information on cover page

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