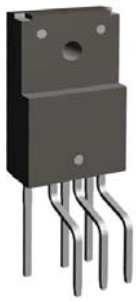
STR-W6000S Series PWM Off-Line Switching Regulator ICs

General Description

The STR-W6000S series are power ICs for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC in one package. To achieve low power consumption, the product includes a startup circuit and a standby function in the controller.

The switching modes are automatically changed according to load conditions so that the PWM mode is in normal operation and the burst mode is in light load condition. The rich set of protection features helps to realize low component counts, and high performance-to-cost power supply.



Not to scale

TO-220F-6L package

Features and Benefits

- Current mode PWM control
- Brown-In and Brown-Out function: auto-restart, prevents excess input current and heat rise at low input voltage
- Auto Standby function: improves efficiency by burst mode operation in light load
  - Normal load operation: PWM mode
  - Light load operation: Burst mode
- No load power consumption < 30 mW
- Random Switching function: reduces EMI noise, and simplifies EMI filters
- Slope Compensation function: avoids subharmonic oscillation
- Leading Edge Blanking function
- Audible Noise Suppression function during Standby mode
- Protection features
  - Overcurrent Protection function (OCP): pulse-by-pulse, with input compensation function
  - Overvoltage Protection function (OVP): auto-restart
  - Overload Protection function (OLP): auto-restart, with timer
  - Thermal shutdown protection (TSD): auto-restart

Applications

Switching power supplies for electronic devices such as:

- Home appliances
- Digital appliances
- Office automation (OA) equipment
- Industrial apparatus
- Communication facilities

The product lineup for the STR-W6000S series provides the following options

Part Number	f_{OSC} (kHz)	Power MOSFET		Output Power*, P_{OUT} (W)	
		V_{DSS}(min) (V)	$R_{DS(ON)}$(max) (Ω)	230 VAC	85 to 265 VAC
STR-W6051S	67	650	3.95	45	30
STR-W6052S			2.8	60	40
STR-W6053S			1.9	90	60

*The listed output power is based on the thermal ratings, and the peak output power can be 120% to 140% of the value stated here. At low output voltage and short duty cycle, the output power may be less than the value stated here.

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Absolute Maximum Ratings

- Refer to the datasheet of each product for these details.
- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.

Absolute Maximum Ratings Unless otherwise specified, T_A = 25°C

Characteristic	Symbol	Conditions		Pins	Rating	Unit
Drain Peak Current	I_{DPEAK}	STR-W6051S	Single pulse	1 − 3	5.0	A
		STR-W6052S			7.0	A
		STR-W6053S			9.5	A
Drain Peak Current[1]	I_{DMAX}	STR-W6051S	Single pulse, T_A= –20°C to 125°C	1 − 3	5.0	A
		STR-W6052S			7.0	A
		STR-W6053S			9.5	A
Avalanche Energy[2]	E_{AS}	STR-W6051S	I_{LPEAK} = 2.0 A	1 − 3	47	mJ
		STR-W6052S	I_{LPEAK} = 2.3 A		62	mJ
		STR-W6053S	I_{LPEAK} = 2.7 A		86	mJ
S/OCP Pin Voltage	V_{OCP}			3 − 5	−2 to 6	V
Control Part Input Voltage	V_{CC}			4 − 5	32	V
FB/OLP Pin Voltage	V_{FB}			6 − 5	−0.3 to 14	V
FB/OLP Pin Sink Current	I_{FB}			6 − 5	1.0	mA
BR Pin Voltage	V_{BR}			7 − 5	−0.3 to 7	V
BR Pin Sink Current	I_{BR}			7 − 5	1.0	mA
Power Dissipation of MOSFET	P_{D1}	STR-W6051S	With infinite heatsink	1 − 3	22.3	W
		STR-W6052S			23.6	W
		STR-W6053S			26.5	W
		Without heatsink			1.3	W
Power Dissipation of Control Part	P_{D2}	$V_{CC} \times I_{CC}$		4 − 5	0.13	W
Internal Frame Temperature in Operation[3]	T_F			–	−20 to 115	°C
Operating Ambient Temperature	T_{OP}			–	−20 to 125	°C
Storage Temperature	T_{stg}			–	−40 to 125	°C
Channel Temperature	T_{ch}			–	150	°C

[1]The maximum switching current is the drain current determined by the drive voltage of the IC and threshold voltage (V_{th}) of the MOSFET.

[2]Single pulse, V_{DD} = 99 V, L = 20 mH.

[3]The recommended internal frame temperature in operation, T_F, is 105°C (max).

Electrical Characteristics

- Refer to the datasheet of each product for these details.
- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.

Electrical Characteristics of Control Part Unless otherwise specified, T_A = 25°C, V_{CC} = 18 V

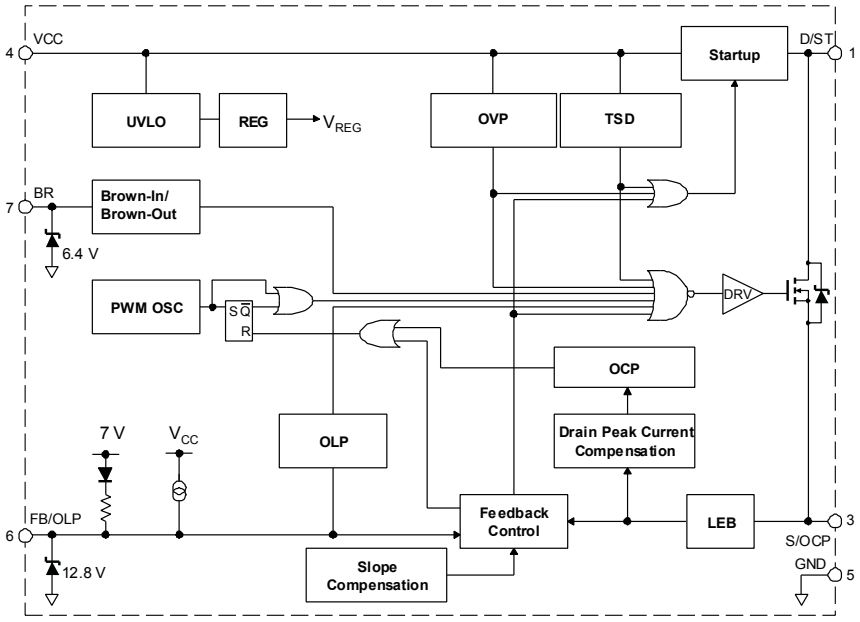
Characteristic	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Operation Start Voltage	$V_{CC(ON)}$		4 – 5	13.8	15.3	16.8	V
Operation Stop Voltage*	$V_{CC(OFF)}$		4 – 5	7.3	8.1	8.9	V
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	4 – 5	–	–	2.5	mA
Minimum Start Voltage	$V_{ST(ON)}$		4 – 5	–	40	–	V
Startup Current	$I_{STARTUP}$	V_{CC} = 13.5 V	4 – 5	−3.9	−2.5	−1.1	mA
Startup Current Threshold Biasing Voltage*	$V_{CC(BIAS)}$	I_{CC} = −100 µA	4 – 5	8.5	9.5	10.5	V
Average Operation Frequency	$f_{OSC(AVG)}$		1 – 5	60	67	74	kHz
Frequency Modulation Deviation	Δf		1 – 5	–	5	–	kHz
Maximum Duty Cycle	D_{MAX}		1 – 5	63	71	79	%
Leading Edge Blanking Time	t_{BW}		–	–	390	–	ns
OCP Compensation Coefficient	DPC		–	–	18	–	mV/µs
OCP Compensation Duty Cycle Limit	D_{DPC}		–	–	36	–	%
OCP Threshold Voltage at Zero Duty Cycle	$V_{OCP(L)}$		3 – 5	0.70	0.78	0.86	V
OCP Threshold Voltage at 36% Duty Cycle	$V_{OCP(H)}$	V_{CC} = 32 V	3 – 5	0.79	0.88	0.97	V
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	6 – 5	−340	−230	−150	µA
Minimum Feedback Current	$I_{FB(MIN)}$		6 – 5	−30	−15	−7	µA
FB/OLP Pin Oscillation Stop Threshold Voltage	$V_{FB(STB)}$		6 – 5	0.85	0.95	1.05	V
OLP Threshold Voltage	$V_{FB(OLP)}$		6 – 5	7.3	8.1	8.9	V
OLP Delay Time	t_{OLP}		6 – 5	54	68	82	ms
OLP Operation Current	$I_{CC(OLP)}$	V_{CC} = 12 V	4 – 5	–	300	–	µA
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		6 – 5	11	12.8	14	V
Brown-In Threshold Voltage	$V_{BR(IN)}$	V_{CC} = 32 V	7 – 5	5.2	5.6	6	V
Brown-Out Threshold Voltage	$V_{BR(OUT)}$	V_{CC} = 32 V	7 – 5	4.45	4.8	5.15	V
BR Pin Clamp Voltage	$V_{BR(CLAMP)}$	V_{CC} = 32 V	7 – 5	6	6.4	7	V
BR Function Disabling Threshold Voltage	$V_{BR(DIS)}$	V_{CC} = 32 V	7 – 5	0.3	0.48	0.7	V
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		4 – 5	26	29	32	V
Thermal Shutdown Temperature	$T_{j(TSD)}$		–	130	–	–	°C

*$V_{CC(BIAS)}$ > $V_{CC(OFF)}$ always.

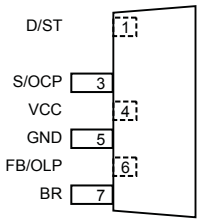
Electrical Characteristics of MOSFET Unless otherwise specified, T_A is 25°C

Characteristic	Symbol	Conditions		Pins	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}			1 – 3	650	–	–	V
Drain Leakage Current	I_{DSS}			1 – 3	–	–	300	μA
On-Resistance	$R_{DS(ON)}$	STR-W6051S		1 – 3	–	–	3.95	Ω
		STR-W6052S			–	–	2.8	Ω
		STR-W6053S			–	–	1.9	Ω
Switching Time	t_f			1 – 3	–	–	250	ns
Thermal Resistance	$R_{\theta ch-C}$	STR-W6051S	The thermal resistance between the channels of the MOSFET and the internal frame.	–	–	–	2.63	°C/W
		STR-W6052S			–	–	2.26	°C/W
		STR-W6053S			–	–	1.95	°C/W

Functional Block Diagram



Pin List Table



(LF2003)

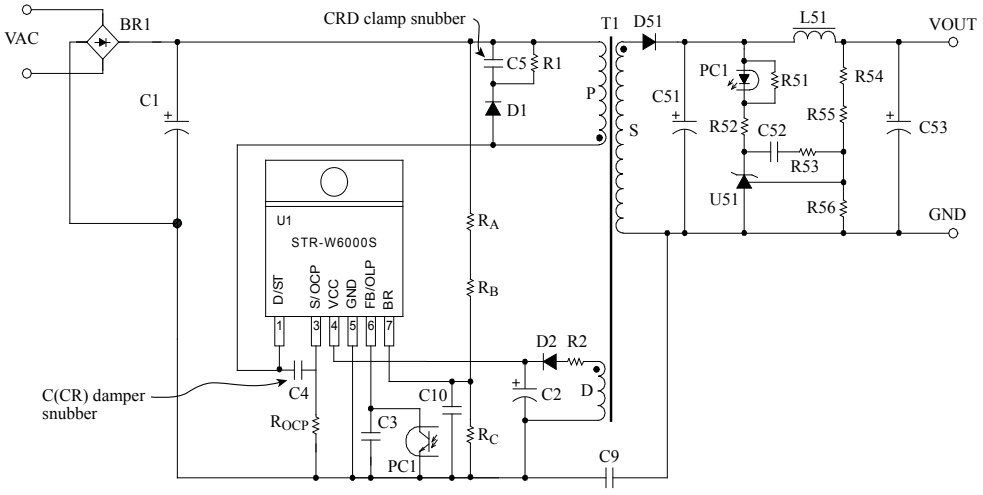
Number	Name	Function
1	D/ST	MOSFET drain, and input of the startup current
2	–	(Pin removed)
3	S/OCP	MOSFET source, and input of Overcurrent Protection (OCP) signal
4	VCC	Power supply voltage input for Control Part, and input of Overvoltage Protection (OVP) signal
5	GND	Ground
6	FB/OLP	Feedback signal input for constant voltage control signal, and input of Overload Protection (OLP) signal
7	BR	Input of Brown-In and Brown-Out detection voltage

Typical Application Circuit

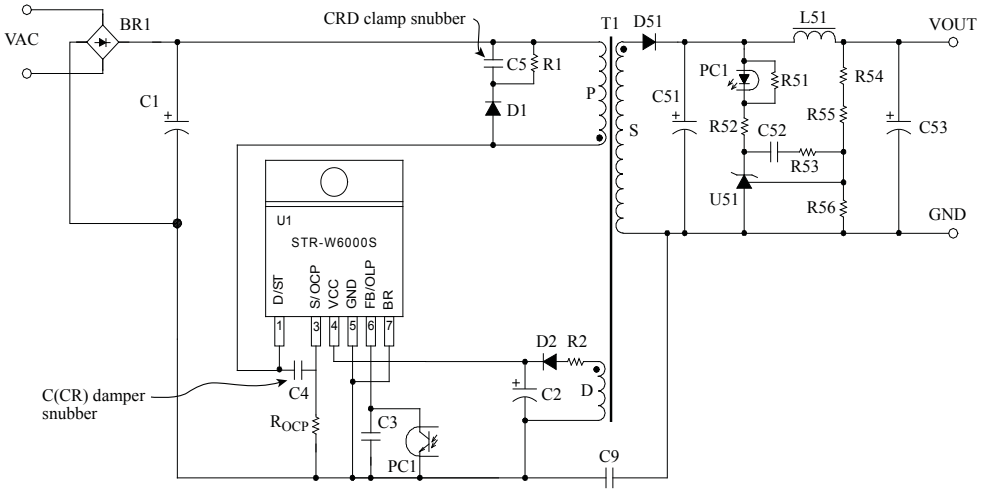
The following drawings show circuits enabled and disabled the Brown-In/Brown-Out function.

The following design features should be observed:

- The PCB traces from the D/ST pins should be as wide as possible, in order to enhance thermal dissipation.
- In applications having a power supply specified such that V_{DS} has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary-side winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.



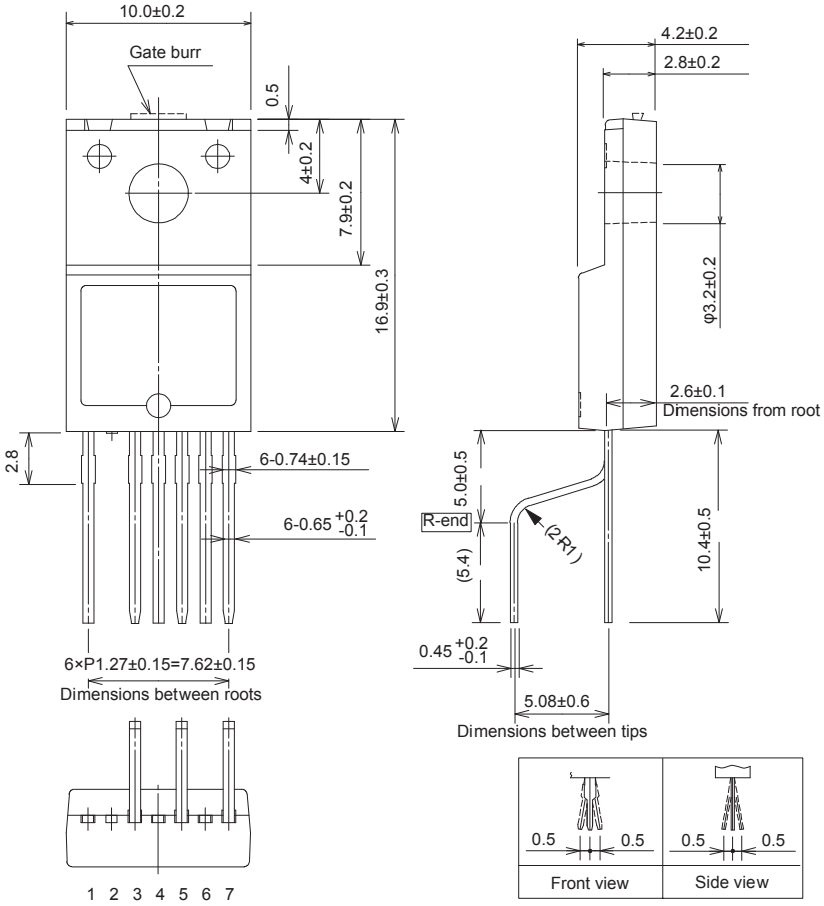
Typical application circuit example, enabled Brown-In/Brown-Out function (DC line detection)



Typical application circuit example, disabled Brown-In/Brown-Out function

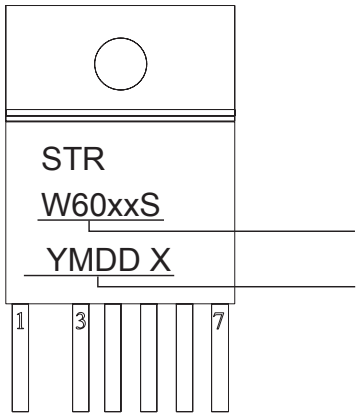
Package Diagram

- TO-220F-6L package
- The pin 2 is removed to provide greater creepage and clearance isolation between the high voltage pin (pin 1: D/ST) and the low voltage pin (pin 3: S/OCP).



Unit: mm
Leadform: LF No.2003
Gate burr indicates protrusion of 0.3 mm (max).
Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Marking Diagram



Part Number

Lot Number
Y is the last digit of the year (0 to 9)
M is the month (1 to 9, O, N, or D)
DD is the day (01 to 31)
X is the Sanken Control Symbol

Functional Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

Startup Operation

Figure 1 shows the VCC pin peripheral circuit, disabled the Brown-In/Brown-Out function by connecting the BR pin trace to the GND pin trace.

The built-in startup circuit is connected to the D/ST pin. When the D/ST pin voltage increases to $V_{ST(ON)}$ = 40 V, the startup circuit starts operation.

In figure 1, the Startup Current, $I_{STARTUP}$, which is a constant current of –2.5 mA, is provided from the IC to capacitor C2 connected to the VCC pin, and it charges C2. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the IC starts operation. After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

During the IC operation, the rectified voltage from the auxiliary winding voltage, V_D, of figure 1 becomes a power source to the VCC pin.

The winding turns of winding D should be adjusted so that the VCC pin voltage is applied to equation (1) within the specifications of the input voltage range and output load range of the power supply. The target voltage of the winding D is about 15 to 20 V.

$$V_{CC(BIAS)}(\max) < V_{CC} < V_{CC(OVP)}(\min) \quad (1)$$

$$\Rightarrow 10.5\ (\text{V}) < V_{CC} < 26.0\ (\text{V})$$

The startup time, t_{START}, is determined by the value of C2, and it is approximately given as below:

$$t_{START} \approx C_2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STARTUP}|} \quad (2)$$

where:

t_{START} is the startup time in s, and

$V_{CC(INT)}$ is the initial voltage of the VCC pin in V.

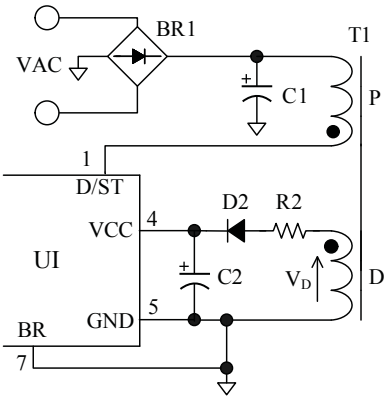


Figure 1. VCC pin peripheral circuit

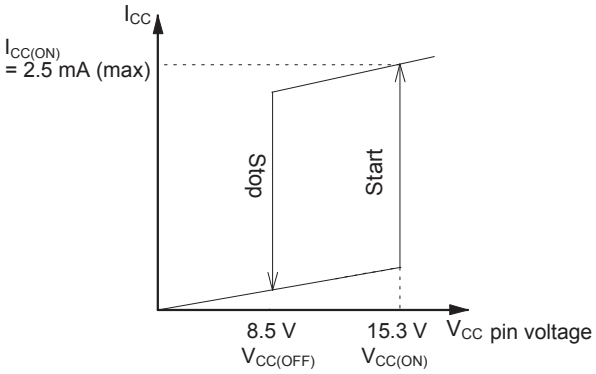


Figure 2. V_{CC} versus I_{CC}

Undervoltage Lockout (UVLO) Circuit

Figure 2 shows the relationship of V_{CC} and I_{CC}. After the IC starts operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the IC stops switching operation by the UVLO (Undervoltage Lockout) circuit and reverts to the state before startup again.

Bias Assist Function

Figure 3 shows the VCC pin voltage behavior during the startup period. When the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the IC starts operation. Thus, the circuit current, I_{CC}, increases, and the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise.

Thus, the VCC pin voltage is set by the balance between dropping due to the increase of I_{CC} and rising due to the increase of the auxiliary winding voltage, V_D.

Just at the turning-off of the power MOSFET, a surge voltage occurs at the output winding. If the feedback control is activated by the surge voltage on light load condition at startup, the output power is restricted and the output voltage decreases.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the IC stops switching operation and a startup failure occurs.

In order to prevent this, the Bias Assist function is activated when the VCC pin voltage decreases to the Startup Current Threshold Biasing Voltage, $V_{CC(BIAS)}$ = 9.5 V, during a state of operating feedback control. While the Bias Assist function is activated, any decrease of the VCC pin voltage is counteracted by providing the Startup Current, $I_{STARTUP}$, from the startup circuit. Thus, the VCC pin voltage is kept almost constant.

By the Bias Assist function, the value of C2 is allowed to be small and the startup time becomes shorter. Furthermore, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function becomes shorter.

It is necessary to check and adjust the startup process based on actual operation in the application, so that the startup failure does not occur.

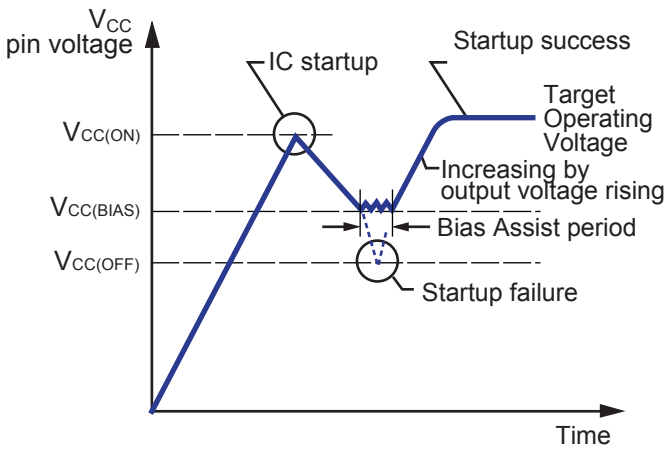


Figure 3. VCC pin voltage during startup period

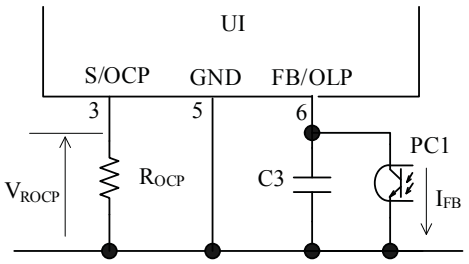


Figure 4. FB/OLP pin peripheral circuit

Constant Voltage Control Operation

The constant output voltage control function uses current mode control (peak current mode), which enhances response speed and provides stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (refer to Function Block Diagram section), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in figures 4 and 5.

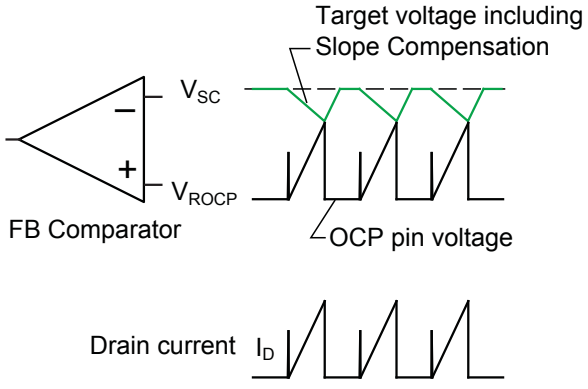


Figure 5. Drain current, I_D, and FB comparator in steady operation

• Light load conditions

When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photocoupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases. This control prevents the output voltage from increasing.

• Heavy load conditions

When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases. This control prevents the output voltage from decreasing.

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in figure 6. This is called the *subharmonics* phenomenon.

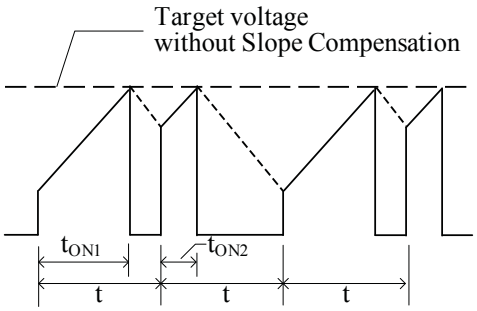


Figure 6. Drain current, I_D, waveform in subharmonic oscillation

In order to avoid this, the IC incorporates the Slope Compensation function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

In the current mode control method, the FB comparator and/or the OCP comparator may respond to the surge voltage resulting from the drain surge current in turning-on the power MOSFET. As a result, the power MOSFET may turn off irregularly. In order to prevent this response to the surge voltage in turning-on the power MOSFET, Leading Edge Blanking, t_{BW} = 390 ns, is built-in.

Auto Standby Mode Function

Auto Standby mode is activated automatically when the drain current, I_D, reduces under light load conditions, at which I_D is less than 15% to 20% of the maximum drain current (it is in the Overcurrent Protection state).

The operation mode becomes burst oscillation, as shown in figure 7. Burst mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

Generally, to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.5 V during the transition to the burst mode, the Bias Assist function is activated and stabilizes the standby mode operation, because $I_{STARTUP}$ is

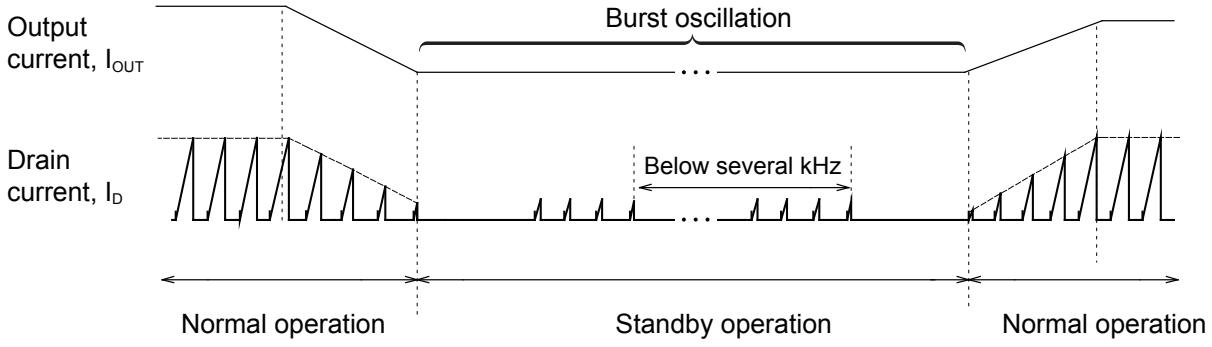


Figure 7. Auto Standby mode timing

provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary-side winding and/or reducing the value of R2 in figure 16 (refer to Peripheral Components section for a detail of R2).

Random Switching Function

The IC modulates its switching frequency randomly within Δf = 5 kHz superposed on the average operation frequency, $f_{OSC(AVG)}$ = 67 kHz. The conduction noise with this function is smaller than that without this function, and this function can simplify noise filtering of the input lines of power supply.

Brown-In and Brown-Out Function

This function stops switching operation when it detects low input line voltage, and thus prevents excessive input current and overheating. During Auto Standby mode, this function is disabled.

Disabled Brown-In and Brown-Out Function

When the Brown-In and Brown-Out function is unnecessary, connect the BR pin trace to the GND pin trace so that the BR pin voltage is $V_{BR(DIS)}$ = 0.48 V or less, as shown in figure 8.

Brown-In and Brown-Out Function by DC Line Detection

The BR pin detects a voltage proportional to the DC input voltage (C1 voltage), with the resistive voltage divider R_A, R_B, and R_C connected between the DC input and GND, plus C10 connected to the BR pin, as shown in figure 8-9.

This method detects peaks of the ripple voltage of the rectified AC input voltage, and thus it minimizes the influence of load conditions on the detecting voltage.

During the input voltage rising from the stopped state of power supply, when the BR pin voltage increases to $V_{BR(DIS)}$ = 0.48 V or more, this function is enabled. After that, when the BR pin voltage increases to $V_{BR(IN)}$ = 5.6 V or more and the VCC pin voltage

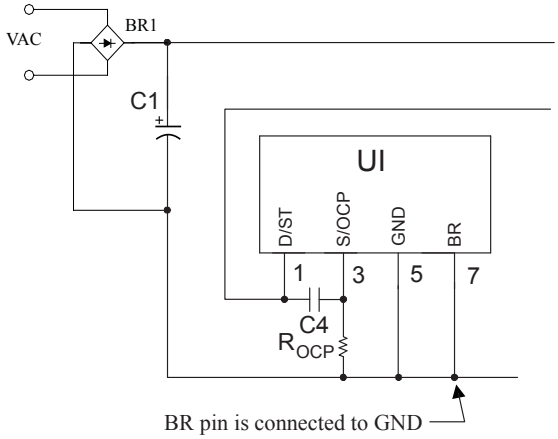


Figure 8. The circuit used to disable the Brown-In and Brown-Out function

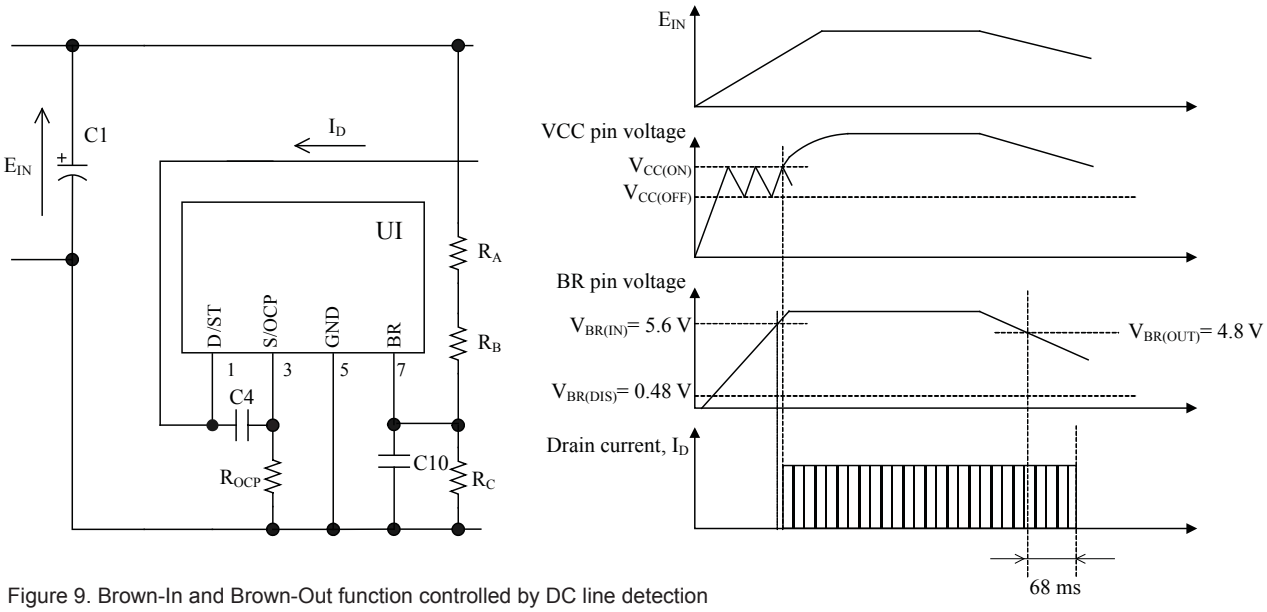


Figure 9. Brown-In and Brown-Out function controlled by DC line detection

increases to $V_{CC(ON)}$ or more, the IC starts switching operation.

During the input voltage falling from the operated state of power supply, when the BR pin voltage decreases to $V_{BR(OUT)}$ = 4.8 V or less for about 68 ms, the IC stops switching operation.

- Component values of the BR pin peripheral circuit:
  - R_A, R_B: A few megohms. Because of high DC voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
  - R_C: A few hundred kilohms
  - C10: 100 to 1000 pF for high frequency noise rejection

Brown-In and Brown-Out Function by AC Line Detection

The BR pin detects a voltage proportional to the AC input voltage, with the resistive voltage divider R_A, R_B, and R_C connected between one side of the AC line and GND, plus C10 connected to the BR pin and R9 connected between the BR pin and the VCC pin, as shown in figure 10.This method detects the AC input voltage, and thus it minimizes the influence from C1 charging and discharging time, or load conditions, on the detecting voltage.

During the input voltage rising from the stopped state of power supply, when the BR pin voltage increases to $V_{BR(DIS)}$ = 0.48 V or more, this function is enabled. After that, when the BR pin voltage increases to $V_{BR(IN)}$ = 5.6 V or more and the VCC pin voltage increases to $V_{CC(ON)}$ or more, the IC starts switching operation.

During the input voltage falling from the operated state of power supply, when the BR pin voltage decreases to $V_{BR(OUT)}$ = 4.8 V or less for about 68 ms, the IC stops switching operation.

- Component values of the BR pin peripheral circuit:
  - R_A, R_B: A few megohms. Because of high DC voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
  - R_C: A few hundred kilohms
  - C10: 0.047 to 0.47 µF for AC ripple rejection. This should be adjusted according to values of R_A, R_B, and R_C.
  - R9: To enable the Brown-In and Brown-Out function, this value must be adjusted so that the BR pin voltage is more than $V_{BR(DIS)}$ = 0.48 V when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V.

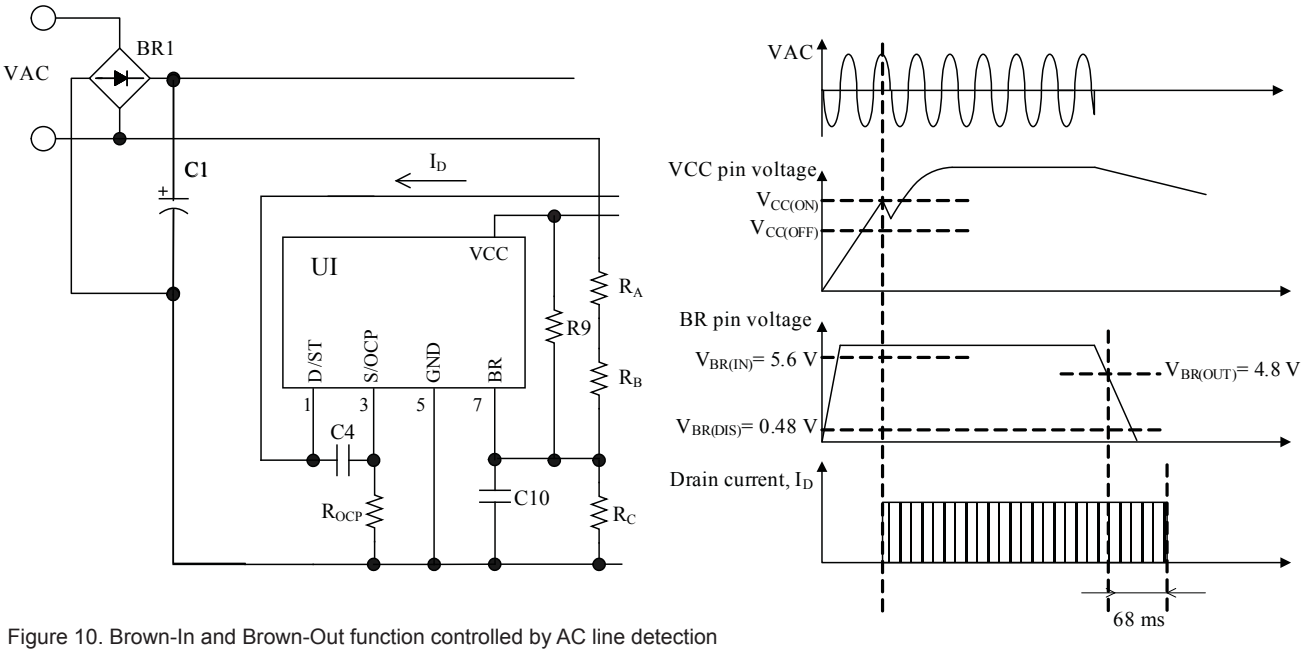


Figure 10. Brown-In and Brown-Out function controlled by AC line detection

Overcurrent Protection Function (OCP)

The OCP function detects each peak drain current level of the power MOSFET by the current detection resistor, R_{OCP}. When the OCP pin voltage increases to the internal OCP threshold voltage, the IC turns off the power MOSFET on pulse-by-pulse basis, and limits the output power.

ICs with PWM control usually have some detection delay time on OCP detection. The steeper the slope of the actual drain current at a high AC input voltage is, the later the actual detection point is, compared to the internal OCP threshold voltage. Thus, the actual OCP point limiting the output current usually has some variation depending on the AC input voltage, as shown in figure 11.

The IC incorporates a built-in Input Compensation function that superposes a signal with a defined slope into the detection signal on the OCP pin as shown in figure 12. When AC input voltage is lower and the duty cycle is longer, the OCP compensation level increases more than that in high AC input voltage. Thus, the OCP point in low AC input voltage increases to minimize the difference of OCP points between low AC input voltage and high AC input voltage, without any additional components.

Because the compensation signal level is designed to depend upon the on-time of the duty cycle, the OCP threshold voltage after compensation, $V_{OCP(ONTime)}$, is given as below. However, when the duty cycle becomes 36% or more, the OCP threshold voltage after compensation remains at $V_{OCP(H)}$ = 0.88 V, constantly

$$V_{OCP(ONTime)}\,(V) = V_{OCP(L)}(V) + DPC\,(mV/\mu s) \times On\ Time\,(\mu s). \quad (3)$$

where:

$V_{OCP(L)}$ is the OCP threshold voltage at zero duty cycle (V), 0.78 V

DPC is the OCP compensation coefficient (mV/µs), 18 mV/µs, and

On Time is the the on-time of the duty cycle (µs):
On Time = On Duty / $f_{OSC(AVG)}$

Overvoltage Protection Function (OVP)

When the voltage between the VCC pin and the GND pin is applied to the OVP threshold voltage, $V_{CC(OVP)}$ = 29 V or more, the Overvoltage Protection function (OVP) is activated and the IC stops switching operation.

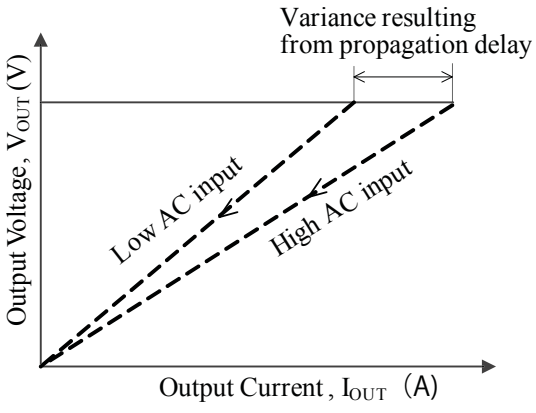


Figure 11. Output current at OCP without input compensation

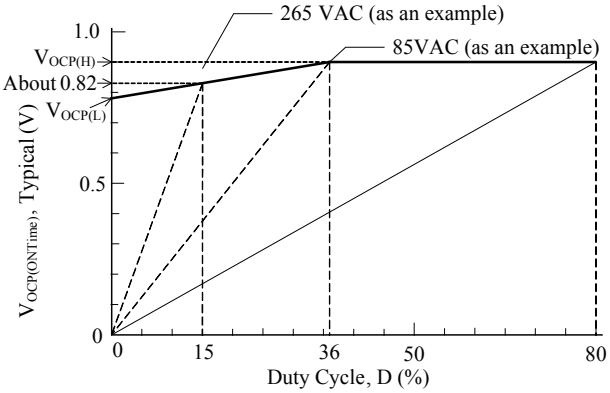


Figure 12. Relationship of duty cycle and OCP threshold voltage after compensation

When the OVP function is activated, the Bias Assist function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V. Thus, the IC stops switching operation by the UVLO (Undervoltage Lockout) circuit and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, and the IC starts switching operation again. In this way, the intermittent operation by UVLO is repeated during OVP state.

This operation reduces power stress on the power MOSFET and secondary-side rectifier diode. Furthermore, this reduces power consumption, because the switching period in this intermittent operation is shorter than non-switching interval. When the fault condition is removed, the IC returns to normal operation automatically.

When the auxiliary winding supplies the VCC pin voltage, the OVP function is able to detect an excessive output voltage, such as when the detection circuit for output control is open on the secondary-side, because the VCC pin voltage is proportional to the output voltage.

The output voltage of the secondary-side at OVP operation, $V_{OUT(OVP)}$, is approximately given as below:

$$V_{OUT(OVP)} = \frac{V_{OUT}(\text{normal operation})}{V_{CC}(\text{normal operation})} \times 29 \text{ (V)} \quad (4)$$

Overload Protection Function (OLP)

Figure 13 shows the FB/OLP pin peripheral circuit, and figure 14 shows each waveform for OLP operation.

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current flowing to the photocoupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin, and the FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 8.1 V or more for the OLP Delay Time, t_{OLP} = 68 ms or more, the OLP function is activated and the IC stops switching operation.

When the OLP function is activated, the Bias Assist function is disabled and the intermittent operation by UVLO is repeated in the same way as described in the Overvoltage Protection Function (OVP) section. When the fault condition is removed, the IC returns to normal operation automatically.

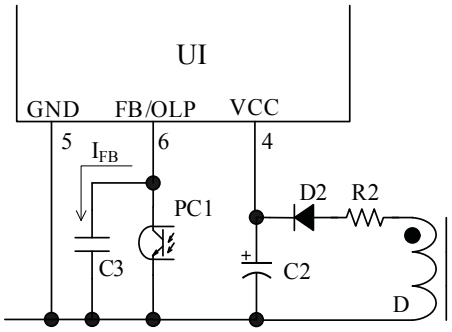


Figure 13. FB/OLP pin peripheral circuit

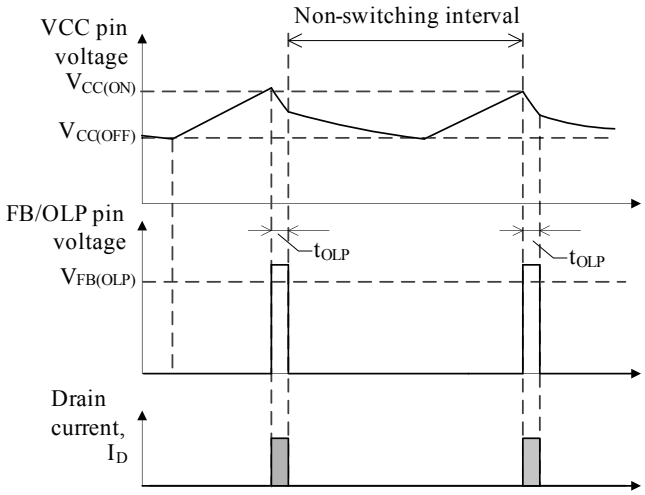


Figure 14. OLP operation waveforms

Thermal Shutdown Function (TSD)

If the temperature of the control part in the IC increases to more than $T_{j(TSD)}$ = 135°C (min), the Thermal Shutdown function (TSD) is activated and the IC stops switching operation. When the TSD function is activated, the Bias Assist function is disabled and the intermittent operation by UVLO is repeated in the same way as described in the Overvoltage Protection Function (OVP) section. If the factor causing the overheating condition is removed, and the temperature of the Control Part decreases to $T_{j(TSD)}$, the IC returns to normal operation automatically.

Design Notes

Peripheral Components

Take care to use the proper rating and proper type of components.

• Input and output electrolytic capacitors

Apply proper design margin to accommodate ripple current, voltage, and temperature rise.

A low ESR type for output smoothing capacitor, designed for switch-mode power supplies, is recommended to reduce output ripple voltage.

• Current detection resistor, R_{OCP}

Choose a low inductance and high surge-tolerant type. Because a high frequency switching current flows to R_{OCP} in figure 15, a high inductance resistor may cause poor operation.

• BR pin peripheral circuit

The Brown-In and Brown-Out function has two types of detection method: AC line or DC line. Refer to Brown-In and Brown-Out Function section for more details.

• FB/OLP pin peripheral circuit

C3, located between the FB/OLP pin and the GND pin in figure 15, performs high frequency noise rejection and phase compensation, C3 should be connected close to these pins. The reference value of C3 is about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

• VCC pin peripheral circuit

Figure 16 shows the VCC pin peripheral circuit. The reference value of C2 is generally 10 to 47 µF (refer to Startup Operation section, because the startup time is determined by the value of C2).

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see figure 17), and the Overvoltage Protection function (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary-side winding when the power MOSFET turns off.

For alleviating C2 peak charging, it is effective to add some

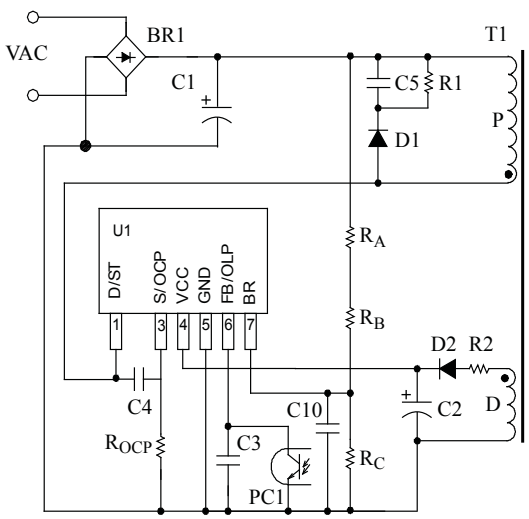


Figure 15. IC peripheral circuit

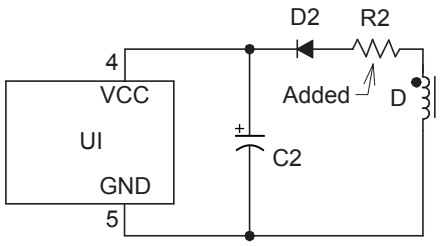


Figure 16. VCC pin peripheral circuit

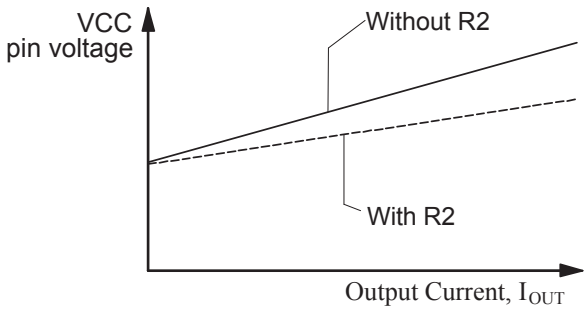


Figure 17. VCC versus I_{OUT} with and without resistor R2

value R2, of several tenths of ohms to several ohms, in series with D2 (see figure 16). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

• Phase Compensation

A typical phase compensation circuit with a secondary-side shunt regulator (U51) is shown in figure 18.

The reference value of C52 for phase compensation is about 0.047 to 0.47 μF, and should be adjusted based on actual operation in the application.

• Transformer

Apply proper design margin to core temperature rise due to core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of about 3 to 4 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

▫ Increase the number of wires in parallel.

▫ Use litz wire.

▫ Thicken the wire gauge.

Fluctuation of the VCC pin voltage by I_{OUT} worsens in the following cases, requiring a transformer designer to pay close attention to the placement of the auxiliary winding D:

▫ Poor coupling between the primary-side and secondary-side windings (this causes high surge voltage and is seen in a design with low output voltage and high output current)

▫ Poor coupling between the auxiliary winding D and the secondary-side stabilized output winding where the output line voltage is controlled constant by the output voltage feedback (this is susceptible to surge voltage)

In order to reduce the influence of surge voltage on the VCC pin, figure 19 shows winding structural examples which take into consideration the placement of the auxiliary winding D:

▫ Winding structural example (a): Separating the auxiliary winding D from the primary-side windings P1 and P2. P1 and P2 are windings divided the primary-side winding into two.

▫ Winding structural example (b): Placing the auxiliary winding D within the secondary-side stabilized output winding, S1, in order to improve the coupling of those windings. S1 is a stabilized output winding of secondary-side windings, controlled to constant voltage.

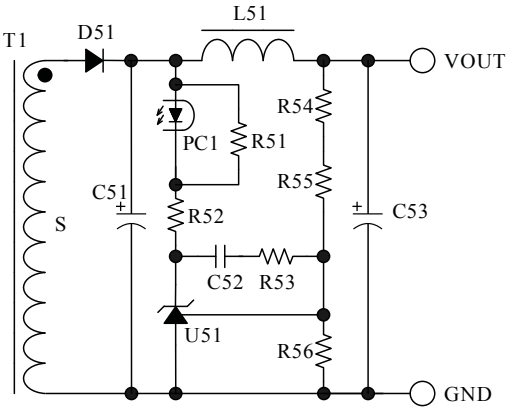
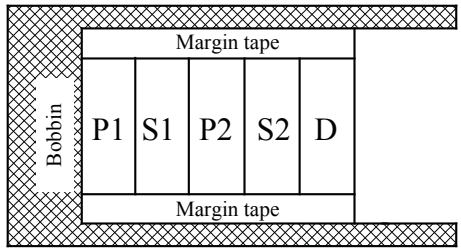
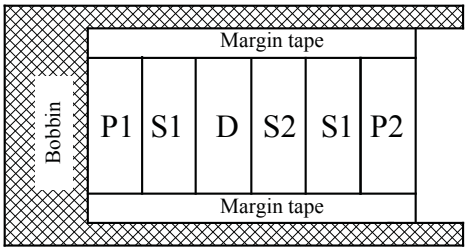


Figure 18. Peripheral circuit around secondary-side shunt regulator (U51)



Winding structural example (a)



Winding structural example (b)

P1, P2: Primary main winding
D: Primary auxiliary winding
S1: Secondary stabilized output winding
S2: Secondary output winding

Figure 19. Winding structural examples

PCB Trace Layout and Component Placement

PCB circuit trace design and component layout significantly affect operation, EMI noise, and power dissipation. Therefore, pay extra attention to these designs. In general, trace loops shown in figure 20 where high frequency currents flow should be wide, short, and small to reduce line impedance. In addition, earth ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Switch -mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines. Furthermore, because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it when preparing a thermal design.

Figure 21 shows a circuit layout design example for the IC peripheral circuit and secondary-side rectifier-smoothing circuit.

• IC Peripheral Circuit

(1) S/OCP pin Trace Layout: S/OCP pin to R_{OCP} to C1 to T1 (winding P) to D/ST pin

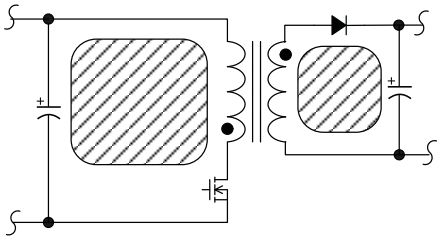


Figure 20. High frequency current loops (hatched areas)

This is the main trace containing switching currents, and thus it should be as wide and short as possible. If the IC and C1 are distant from each other, placing a capacitor such as a film or ceramic capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) GND Trace Layout: GND pin to C2 (negative pin) to T1 (winding D) to R2 to D2 to C2 (positive pin) to VCC pin

This is the trace for supplying power to the IC, and thus it should be as wide and short as possible. If the IC and C2 are distant from each other, placing a capacitor such as a film or ceramic capacitor (about 0.1 to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(3) R_{OCP} Trace Layout

R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in figure 21) which is close to the base of R_{OCP}, to reduce common impedance, and to avoid interference from switching currents to the control part in the IC.

• Secondary-side Rectifier-Smoothing Circuit Trace Layout: T1 (winding S) to D51 to C51

This is the trace of the rectifier-smoothing loop, carrying the switching current, and thus it should be as wide and short as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier-smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

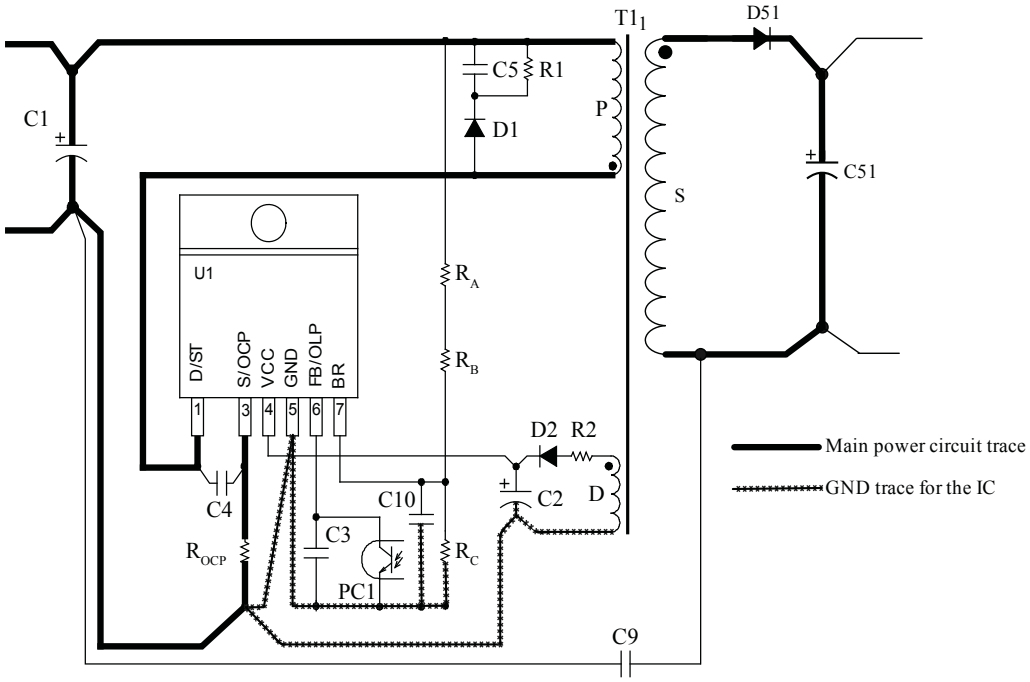


Figure 21. Peripheral circuit example around the IC

Reference Design of Power Supply

As an example, the following show a power supply specification, circuit schematic, bill of materials, and transformer specification.

Power Supply Specification

IC	STR-W6053S
Input Voltage	85 to 265 VAC
Maximum Output Power	56 W (70.4 W_{PEAK})
Output Voltage / Current	8 V / 2.5 A, 12 V / 3 A (4.2 A_{PEAK})

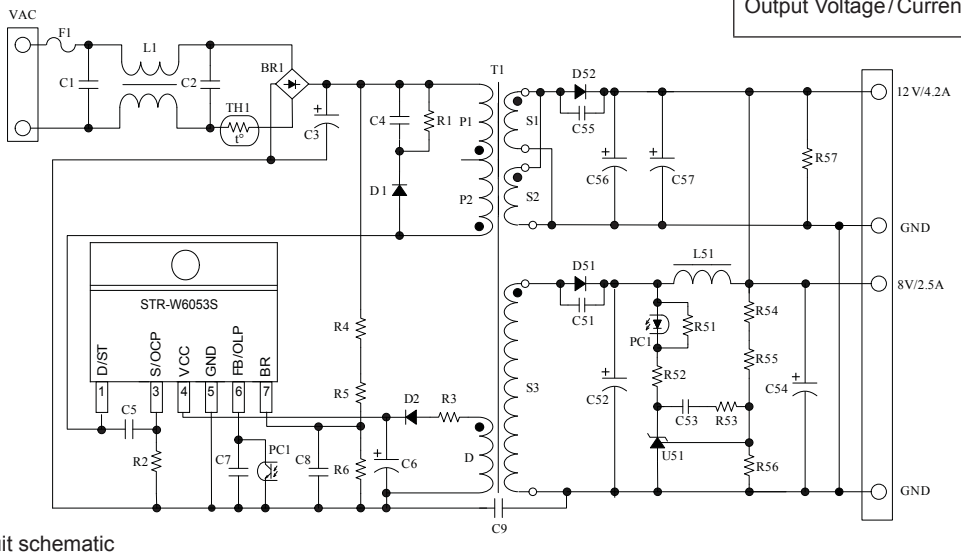


Figure 22. Circuit schematic

Bill of Materials

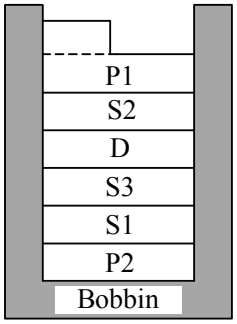
Symbol	Part type	Ratings[a]	Recommended Sanken Parts	Symbol	Part type	Ratings[a]	Recommended Sanken Parts
F1	Fuse	250 VAC, 6 A		PC1	Photo-coupler	PC123 or equiv.	
L1[b]	CM inductor	2.2 mH		U1	IC		STR-W6053S
TH1[b]	NTC thermistor	Short		T1	Transformer	See the specification	
BR1	General	600 V, 6 A		L51	Inductor	5 µH	
D1	Fast recovery	1000 V, 0.5 A	EG01C	D51	Schottky	100 V, 10 A	FMEN-210A
D2	Fast recovery	200 V, 1 A	AL01Z	D52	Fast recovery	150 V, 10 A	FMEN-210B
C1[b]	Film, X2	0.1 µF, 275 V		C51[b]	Ceramic	470 pF, 1 kV	
C2[b]	Film, X2	0.1 µF, 275 V		C52	Electrolytic	1000 µF, 16 V	
C3	Electrolytic	220 µF, 400 V		C53[b]	Ceramic	0.15 µF, 50 V	
C4	Ceramic	3300 pF, 2 kV		C54	Electrolytic	1000 µF, 16 V	
C5	Ceramic	Open		C55	Ceramic	470 pF, 1 kV	
C6	Electrolytic	22 µF, 50 V		C56	Electrolytic	1500 µF, 25 V	
C7[b]	Ceramic	0.01 µF		C57	Electrolytic	1500 µF, 25 V	
C8[b]	Ceramic	1000 pF		R51	General	1.5 kΩ	
C9	Ceramic, Y1	2200 pF, 250 V		R52	General	1 kΩ	
R1[c]	Metal oxide	56 kΩ, 2 W		R53[b]	General	33 kΩ	
R2	General	0.27 Ω, 1 W		R54[b]	General, 1%	3.9 kΩ	
R3	General	5.6 Ω		R55	General, 1%	22 kΩ	
R4[c]	General	2.2 MΩ		R56	General, 1%	6.8 kΩ	
R5[c]	General	2.2 MΩ		R57	General	Open	
R6	General	330 kΩ		U51	Shunt regulator	V_{REF} = 2.5 V TL431 or equiv.	

[a]Unless otherwise specified, the voltage rating of capacitor is 50 V or less, and the power rating of resistor is $^1/_8$ W or less.
[b]It is necessary to be adjusted based on actual operation in the application.
[c]Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

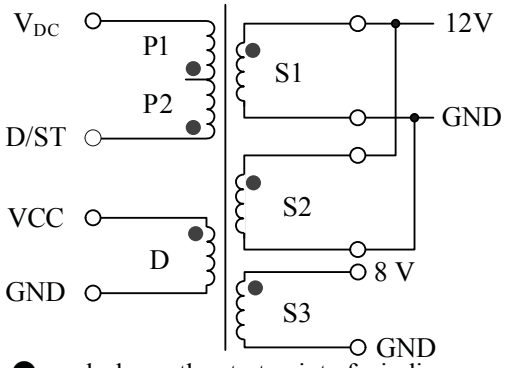
Transformer specification

- Primary inductance, L_P: 315 µH
- Core size: EER28L
- AL-value: 163 nH/N^2 (Center gap of about 0.8 mm)
- Winding specification

Location	Symbol	Number of Turns (T)	Wire (mm)	Configuration
Primary winding	P1	26	TEX-Ø0.35×2	1.5 layers, solenoid winding
Primary winding	P2	18	TEX-Ø0.35×2	Solenoid winding
Auxiliary winding	D	10	TEX-Ø0.23×2	Space winding
Output winding 1	S1	7	Ø0.4×4	Space winding
Output winding 2	S2	7	Ø0.4×4	Space winding
Output winding 3	S3	5	Ø0.4×4	Space winding



Cross-section view



● mark shows the start point of winding

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