SMALL SIGNAL COMBINATION FOR COLOUR TV

GENERAL DESCRIPTION

The integration into a single package of all small signal functions required for colour TV reception is achieved in the TDA4502A. The only additional circuits required for colour TV reception are the deflection output stages, a sound detector and amplifier, and a colour decoder.

The IC includes a vision IF amplifier and video switching circuit, AFC circuit, AGC detector with tuner output, an integral three-level sandcastle pulse generator, fully synchronized vertical and horizontal drive outputs and a mute circuit with external availability. A triggered vertical divider automatically adapts to 50 or 60 Hz operating mode thereby eliminating the need for external vertical frequency control. The sound signal must be demodulated and amplified externally.

Features

- Vision IF amplifier with synchronous demodulator
- AGC detector, suitable for negative modulation
- AGC output to tuner
- AFC circuit with ON/OFF switch
- Video preamplifier
- Video switch to select the internal, or an external, video signal
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generator

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 7)	V_7	9.5	12	13.2	V
Supply current (pin 7)	I_7	–	125	–	mA
Supply current (pin 11)	V_{11}	–	6.0	8.5	mA
Operating ambient temperature range	T_{amb}	−25	–	+ 65	°C
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Total power dissipation	P_{tot}	–	–	2.3	W

PACKAGE OUTLINE

28-lead DIL; plastic with internal heat spreader (SOT117).

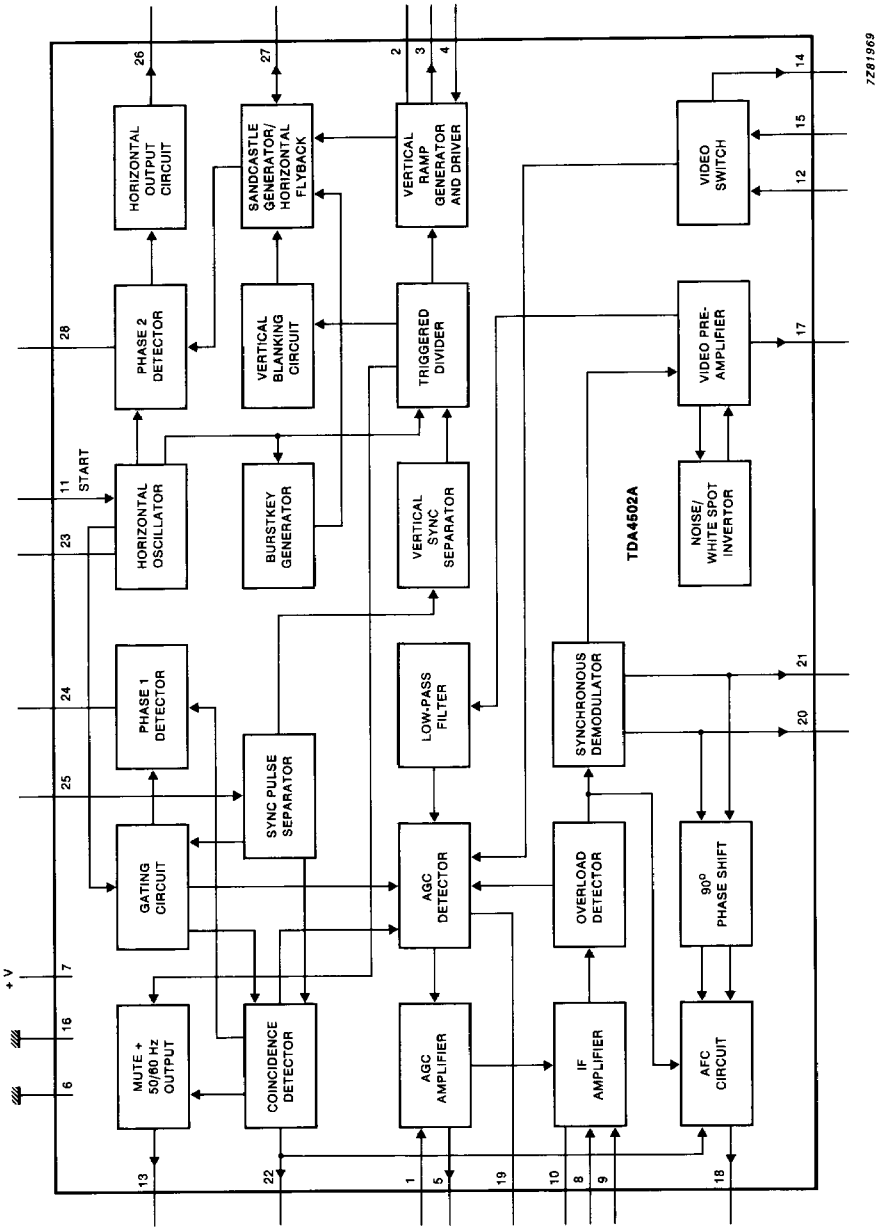


Fig. 1 Block diagram.

PINNING

1. AGC take over input
2. Ramp generator
3. Vertical drive output
4. Vertical feedback input
5. Tuner AGC output
6. Ground
7. Supply
8. IF input
9. IF input
10. Decoupling capacitor
11. Start horizontal oscillator input
12. External video input
13. Mute output
14. Video switch output
15. Internal video and switch input
16. Ground
17. Video output
18. AFC output
19. AGC detection
20. Synchronous demodulator output
21. Synchronous demodulator output
22. Coincidence detector output
23. Horizontal oscillator
24. Phase 1 detector
25. Sync separator
26. Horizontal drive output
27. Sandcastle output/flyback input
28. Phase 2 detector

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

IF amplifier, synchronous demodulator and AFC

The IF amplifier (pins 8 and 9) has a symmetrical input, the impedance of which enables SAW-filtering to be used. The synchronous demodulator and the AFC circuit share an external reference tuned circuit (pins 20 and 21). An internal RC-network provides the necessary phase-shift for AFC operation. The AFC circuit provides a control voltage output with a voltage swing greater than 9 V at pin 18. In the internal and external mode the AFC can be switched OFF when pin 22 is connected to positive supply.

AGC circuit

AGC gating is performed to reduce sensitivity of the IF amplifier to external noise. The AGC time constant is provided by an RC-circuit connected to pin 19. The tuner AGC voltage is supplied from pin 5. The point of tuner take-over is preset by the voltage level at pin 1.

Video switch circuit

The IC has a video switch with two video inputs and one video output. One input is connected to the demodulated IF signal which is also fed to the video output pin of the peritelevision connector. The other input can be switched to an external signal which is applied to the video input of the peritelevision connector. The video output signal of the switch is fed to pin 25 of the IC, which is the synchronization part and, to the colour decoder. When the video switch is in the external mode, the synchronization circuit is switched to the external signal. The vision IF, AGC and AFC circuits will not be affected by the switching action and will, therefore, operate in the normal mode. Gating for the AGC detector is switched OFF when the switch is in the external mode. The first control loop is not switched to a low time constant when weak signals are received.

Horizontal oscillator start function

The horizontal oscillator start function is achieved by applying a current of 8.5 mA to pin 11 during the switch-on period. This current can be taken from the mains rectifier. The main supply, pin 7, can then be obtained from the horizontal output stage. The load current of the driver has to be added to the start current.

Horizontal synchronization

The positive video input signal is applied to pin 25. The horizontal synchronization has two control loops which have been introduced to generate a sandcastle pulse. By using the oscillator sawtooth, an accurate timing of the burst-key pulse can be made. Therefore, the phase of this sawtooth pulse must have a fixed relationship to the sync pulse.

Horizontal phase detector

The circuit has two operating conditions:

(a) Synchronized
The first loop has a fixed time constant and a gated phase detector, this enables optimum performance for co-channel interference. The VCR mode is obtained by an additional load on pin 22.

(b) Non-synchronized
In this condition the time constant is the same as during the VCR mode.

Vertical sync pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of 10 μs and a separation of 22 μs. This type of vertical sync pulse is generated by video tapes with anti-copy guard.

Vertical divider system

A synchronized divider system generates the vertical sawtooth waveforms at pin 2. The system uses an internal frequency doubler circuit to enable the horizontal oscillator to operate at its normal line frequency. One line period equals 2 clock pulses.
Using the divider system avoids the requirement for vertical frequency adjustment. The divider has a discriminator window for automatic switching from 50 Hz to 60 Hz mode. When the trigger pulse arrives before line 576 the 60 Hz mode is selected, if not, the 50 Hz mode is selected.
The divider system operates with two different reset windows to give maximum interference/disturbance protection. The windows are activated via an up/down counter.
The counter is increased by 1 each time the separated vertical sync pulse is within the narrow window. When the sync pulse is not within the narrow window the counter is decreased by 1.
The operation modes of the divider system are as follows:

Mode A

Large (search) window (divider ratio between 488 and 722)

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found – not within the narrow window limits
- A non-standard composite video signal is detected – when a double or enlarged vertical sync pulse is detected after the internally generated anti-top-flutter pulse has ended. This means a vertical sync pulse width > 10 clock pulses (50 Hz); > 12 clock pulses (60 Hz). This mode is normally activated for video tape recorders operating in the feature trick mode
- Up/down counter value of the divider system, operating in the narrow window mode, drops below count 6

Mode B

Narrow window (divider ratio between 522 to 528 (60 Hz) or 622 to 628 (50 Hz))

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and, a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below 6 the divider system switches over to the large window mode.
The divider system also generates an anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. In 'Mode A' the start is generated by resetting the divider. In 'Mode B' the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode.
The vertical blanking pulse is also generated via the divider system. The start is initiated by resetting the divider while the blanking pulse width is at count 34, (17 lines), for the 60 Hz mode and at count 42, (21 lines), for the 50 Hz mode. The vertical blanking pulse, at the sandcastle output (pin 27), is generated by adding the anti-top-flutter pulse to the blanking pulse. When the divider operates in 'Mode B', the vertical blanking pulse starts at the beginning of the first equalizing pulse. The length of the vertical blanking in this condition is 21 lines in the 60 Hz mode and 25 lines in the 50 Hz mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{7-6}$	–	13.2	V
Total power dissipation	P_{tot}	–	2.3	W
Operating ambient temperature range	T_{amb}	−25	+ 65	°C
Storage temperature range	T_{stg}	−25	+ 150	°C

CHARACTERISTICS

$V_P = V_7 = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified; all voltages are referenced to ground (pin 6) unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 7)		V_7	9.5	12.0	13.2	V
Supply current (pin 7)		I_7	–	125	–	mA
Supply current (pin 11)	note 1	I_{11}	–	6	8.5	mA
Vision IF amplifier (pins 8 and 9)						
Input sensitivity at 38.9 MHz	note 2	V_8	40	80	120	μV
Input sensitivity at 45.75 MHz	note 2	V_8	–	100	–	μV
Differential input resistance (pin 8 to pin 9)	note 3	R_{8-9}	0.8	1.3	1.8	kΩ
Differential input capacitance (pin 8 to pin 9)	note 3	C_{8-9}	–	5	–	pF
Gain control range		G_{8-9}	–	62	–	dB
Maximum input signal		V_{8-9}	50	100	–	mV
Expansion of output signal for 50 dB variation of input signal	note 4	ΔV_{17}	–	1	–	dB
Video amplifier	note 5					
Output level for zero signal input	note 6	V_{17}	3.3	3.7	4.1	V
Output signal top sync level		V_{17}	1.5	1.7	1.9	V
Amplitude of video output signal (peak-to-peak value)	note 7	$V_{17(p-p)}$	1.4	1.8	2.2	V
Internal bias current of output transistor (npn emitter follower)		$I_{17(int)}$	1.4	2.0	–	mA
Bandwidth of demodulated output signal		B	4.0	5.0	–	MHz
Differential gain	note 8	G_{17}	–	5	10	%
Differential phase	note 8	φ	–	5	10	%

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Video non-linearity	note 9	NL	–	5	12	%
Intermodulation	note 10					
f = 1.1 MHz; blue			47	50	–	dB
f = 1.1 MHz; yellow			45	47	–	dB
f = 3.3 MHz; blue			50	55	–	dB
f = 3.3 MHz; yellow			48	52	–	dB
Signal-to-noise ratio	note 11					
input signal = 10 mV		S/N	45	50	–	dB
end of gain control range as		S/N	50	55	–	dB
a function of input voltage	see Fig. 5					
Residual carrier signal			–	7	30	mV
Residual 2nd harmonic of carrier signal			–	15	30	mV
Video switching circuit	note 12					
External video input (positive video; pin 12)						
Input signal (peak-to-peak value)	V_O = 2.4 $V_{(p\text{-}p)}$	$V_{12\ (p\text{-}p)}$	–	0.9	–	V
Input current		I_{12}	–	3.5	–	μA
Top sync clamping level		V_{12}	–	3.4	–	V
Video output (positive video; pin 14)						
Output signal		V_{14}	2.2	2.4	2.6	V
Top sync level		V_{14}	2.4	3.0	3.6	V
Internal bias current npn output transistor		I_{14}	0.8	–	–	mA
Crosstalk of video signal	measured at 4.4 MHz					
external to internal		α	50	55	–	dB
internal to external		α	42	46	–	dB
Internal video and switch input (pin 15)						
Amplitude of input signal (peak-to-peak value)	V_O = 2.4 $V_{(p\text{-}p)}$	$V_{15\ (p\text{-}p)}$	–	1.8	–	V
Input current		I_{15}	–	7	–	μA
Top sync clamping level (via 100 kΩ to ground)		V_{15}	–	4.2	–	V
Condition for internal signal	note 12					
Condition for external signal (via 100 kΩ to positive supply)		V_{15}	–	10	12	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Tuner AGC						
Minimum starting point take over* (RMS value)	I = 0.2 mA	$V_{1(rms)}$	–	–	0.5	mV
Maximum starting point take over* (RMS value)	I = 0.2 mA	$V_{1(rms)}$	50	100	–	mV
Maximum output swing		I_{5max}	6	8	–	mA
Output saturation voltage	I = 2 mA	$V_{5(sat)}$	–	100	300	mV
Leakage current		I_5	–	0.7	1.0	μA
Input signal variation complete tuner control	ΔI_5 = 2 mA	ΔV_i	0.1	2.0	5.0	dB
Minimum voltage take over (pin 1)		V_1	–	–	1	V
AFC circuit (pin 18)	note 13					
AFC output voltage swing (peak-to-peak value)		$V_{18(p-p)}$	9.5	10.2	11.5	V
Available output current		I_{18}	–	± 2.2	–	mA
Control steepness			70	100	150	mV/kHz
Output voltage at nominal tuning of the reference tuned circuit		V_{18}	–	6	–	V
Offset current AFC output (pins 20 and 21 short-circuited)		I_{18}	–	0	± 220	μA
Horizontal synchronization	Fig. 7					
Sync separator and first control loop (pin 25)						
Sync pulse amplitude	note 14	V_{25}	200	–	–	mV
Input current	V_{25} = > 5 V	I_{25}	–	10	–	μA
Input current	V_{25} = 0 V	I_{25}	–	−10	–	mA
Holding range PLL		Δf	–	± 1.1	± 1.5	kHz
Catching range PLL		Δf	+ 0.6	± 1.0	–	kHz
Control sensitivity	note 15					
in sync condition		Δ_{td}	–	2.5	–	kHz/μs
in non-sync condition		Δ_{td}	–	7.5	–	kHz/μs
Second control loop (positive edge)						
Control sensitivity	note 16	$\Delta t_d/\Delta to$	–	50	–	
Control range		t_d	–	25	–	μs

* Take over to be adjusted by a potentiometer with a value of 47 kΩ.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Phase adjustment (via second control loop)						
Control sensitivity			–	25	–	μA/μs
Maximum allowed phase shift		α	–	± 2	–	μs
Horizontal oscillator (pin 23)						
Free running frequency	R = *; C = 2.7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		Δ_f	–	–	4	%
Frequency variation due to change of supply voltage from 9.5 to 13.2 V		Δf_{fr}	–	0	0.5	%
Frequency variation with temperature		TC	–	–	1.6	Hz/°C
Maximum frequency shift		Δf_{fr}	–	4	10	%
Maximum frequency deviation at start horizontal out		Δf_{fr}	0	+ 8	+ 10	%
Horizontal output (pin 26)						
Output voltage high		V_{26}	–	–	13.2	V
Output voltage at which protection commences		V_{26}	–	–	15.8	V
Output voltage low	I_{26} = 10 mA	V_{26}	–	0.3	0.5	V
Duty factor of horizontal output signal	t_p = 10 μs	d	–	45	–	%
Duty factor during start-up		d	–	52	–	%
Rise time of output pulse		t_r	–	260	–	ns
Fall time of output pulse		t_f	–	100	–	ns
Horizontal flyback input and sandcastle output	note 17					
Input current required during flyback pulse		I_{27}	0.1	–	2.0	mA
Output voltage						
during burst-key pulse		V_{27}	8.4	9.0	–	V
during horizontal blanking		V_{27}	4.1	4.35	5.0	V
during vertical blanking		V_{27}	2.1	2.4	2.7	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Horizontal flyback input and sandcastle output (continued)						
Pulse width						
burst-key pulse	60 Hz	t_w	3.1	3.45	3.9	μs
burst-key pulse	50 Hz	t_w	3.5	3.8	4.4	μs
horizontal blanking pulse			flyback pulse width			
vertical blanking pulse						
50 Hz divider in search window			–	21	–	lines
60 Hz divider in search window			–	17	–	lines
50 Hz divider in narrow window			–	25	–	lines
60 Hz divider in narrow window			–	21	–	lines
Delay between start of sync pulse at video output and trailing edge of burst-key pulse			–	–	9.2	μs
Coincidence detector mute output (pin 22)	Fig 6; note 18					
Voltage for in-sync condition		V_{22}	8.5	10.0	10.5	V
Voltage for no-sync condition	no signal	V_{22}	0	0.3	0.6	V
Switching level to switch phase detector from slow to fast		V_{22}	4.9	5.3	5.8	V
Hysteresis		V_{22}	–	0.6	–	V
Voltage for AFC switch-off		V_{22}	–	10.5	11.0	V
Switching level to activate mute function		V_{22}	2.25	2.5	2.75	V
Hysteresis mute function		V_{22}	–	0.6	–	V
Output current (peak-to-peak value)	in-sync	$I_{22(p-p)}$	0.7	1.0	–	mA
Discharge current (peak-to-peak value)		$I_{22(p-p)}$	–	0.5	–	mA
Video transmitter identification output (pin 13)						
Output voltage active	no-sync; $I = 5$ mA	V_{13}	–	0.3	0.5	V
Output current active		I_{13}	–	–	5	mA
Output current inactive	sync	I_{13}	–	–	1	μA

parameter	conditions	symbol	min.	typ.	max.	unit
50/60 Hz identification (pin 13)						
Output voltage						
50 Hz		V_{13}	9	12	–	V
60 Hz		V_{13}	4.7	6.0	6.4	V
Vertical ramp generator (pin 2)	note 19					
Input current during scan		I_2	–	1	2	μA
Discharge current during retrace		I_2	0.3	0.35	–	mA
Sawtooth amplitude (peak-to-peak value)		$V_{2(p-p)}$	–	0.8	1.1	V
Vertical drive output (pin 3)						
Maximum available output current		I_3	1.5	3.5	–	mA
Maximum output voltage		V_3	–	4	–	V
Vertical feedback input (pin 4)						
Input voltage DC component		V_4	2.4	3.0	4.1	V
AC component (peak-to-peak value)		$V_{4(p-p)}$	–	1.2	–	V
Input current		I_4	–	–	12	μA
Internal precorrection to sawtooth		Δt_p	–	6	–	%
Deviation amplitude	50/60 Hz		–	–	2	%
Vertical guard	note 20					
Active at a deviation with respect to the DC feedback level	V_{27} = 2.5 V					
switching voltage level LOW		ΔV_4	0.6	0.9	–	V
switching voltage level HIGH		ΔV_4	–	2	–	V

DEVELOPMENT DATA

Notes to the characteristics

1. The horizontal oscillator can be started when a current of 8.5 mA is applied to pin 11; this current can be taken from the mains rectifier. The main supply (pin 7) can then be derived from the horizontal output stage. The load current of the driver must be added to the start current (8.5 mA).
2. On set AGC.
3. Input impedance selected so that a SAW-filter can be applied.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(rms) top sync input signal.
6. Projected zero point with switched demodulator.
7. Signal with negative going sync top white level 10% of the top sync amplitude.
8. Measured in accordance with the test line given in Fig. 2.
   The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   The differential phase is defined as the difference in degrees between the largest and smallest phase angle.

Notes to the characteristics (continued)

9. This figure is valid for the complete video signal amplitude (peak white to black) and measured with a 6.6 kΩ damping resistor connected between pins 20 and 21 (see Fig. 3).
10. The test set-up and input conditions are given in Fig. 4. The figures are measured at an input signal of 10 mV(rms).
11. Measured with a source impedance of 75 Ω, where:

$$S/N = 20 \log \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

12. The internal video and video switch inputs are applied to pin 15. By externally connecting the internal video signal to the video switch enables the sound trap to be connected between pins 15 and 17. When the video signal is applied internally to the switch then sound traps are required at two outputs. The switch is activated via a 100 kΩ resistor. When the resistor is connected to ground or left open-circuit the internal video signal is available at pin 14. When the resistor is connected to + V_S the external video signal is available at pin 14. When the video switch is in the external mode the AFC can still be switched off when pin 22 is connected to the supply voltage.
13. The measured figures are obtained at an input signal of 10 mV(rms) and the AFC output loaded with 2 x 100 kΩ between the supply voltage and ground. The unloaded Q-factor of the reference tune circuit is 70. The AFC is switched off when pin 22 is connected to the supply voltage.
14. The minimum value is obtained by connecting a 1.8 kΩ series resistor between pins 14 and 25. The slicing level can be varied by changing the value of this resistor (a higher resistor value will result in a higher value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
15. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor between pins 23 and 24. The oscillator can be adjusted to the correct frequency using either of the following methods:

    (a) Interrupt the resistor between pins 23 and 24.
    (b) Short-circuit the sync separator bias network (pin 25 to supply voltage).

    The device uses a long time constant for the first phase detector. The phase detector is gated to obtain optimal performance for co-channel interference. The VCR mode must be switched on via pin 22.
16. This figure is valid for an external load impedance of 82 kΩ connected between pin 28 and the shift-adjustment potentiometer.
17. The flyback input and sandcastle output are combined at pin 27. The flyback pulse is clamped to a level of 4.35 V. The minimum current required to drive the second control loop is 0.1 mA.
18. The functions in-sync/out-of-sync and transmitter identification are combined at pin 22. The 22 nF capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
19. Because the vertical scan is synchronized via a divider system, no adjustment is required for the ramp generator. The divider system detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and subsequently corrects the vertical amplitude.
20. To avoid screenburn, due to a collapse of the vertical deflection, a continuous blanking level is inserted in the sandcastle pulse when the feedback voltage from the vertical deflection is not within the specified limits.

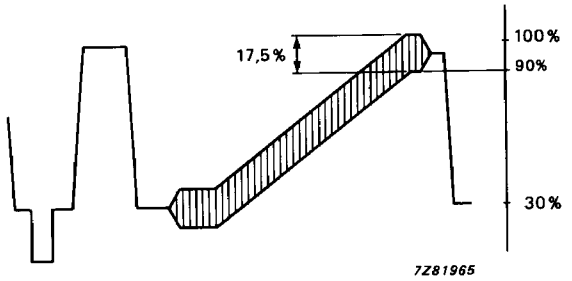


Fig. 2 Video output signal.

DEVELOPMENT DATA

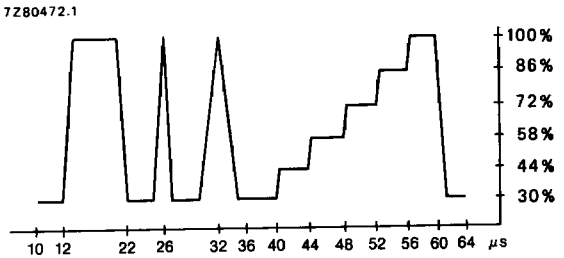
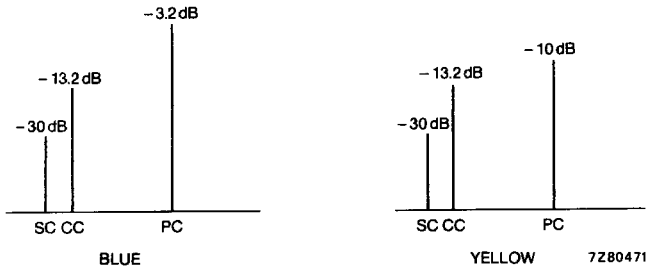


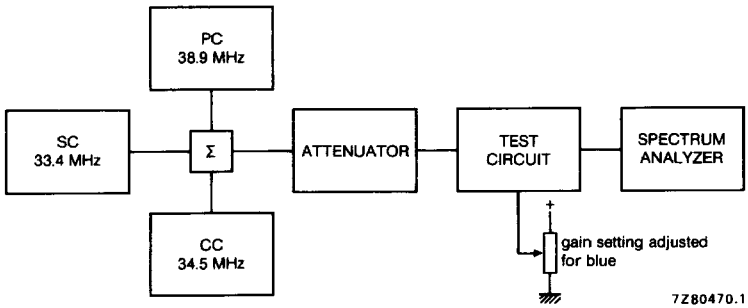
Fig. 3 EBU test signal waveform (line 330).



Input signal conditions:

SC = sound carrier
CC = chrominance carrier
PC = picture carrier

all with respect to top sync level.



Where:

$$\text{Value at 1.1 MHz: } 20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$$

$$\text{Value at 3.3 MHz: } 20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$$

Fig. 4 Test set-up intermodulation.

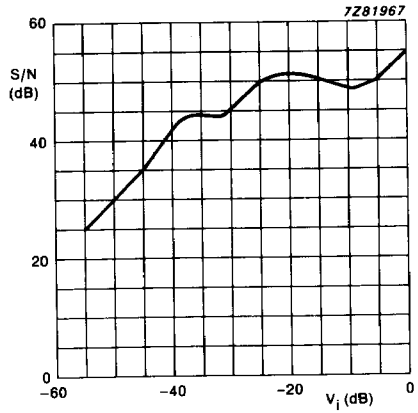
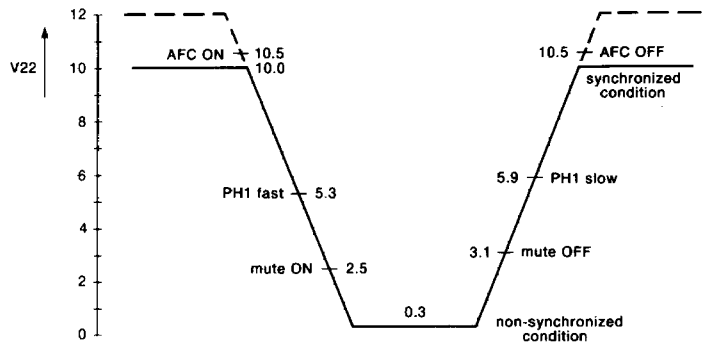


Fig. 5 S/N ratio as a function of the input voltage (0 dB = 100 mV).

DEVELOPMENT DATA



condition	control sensitivity horizontal oscillator kHz/μs		vertical sync separator pulse after
	T2 – T1	T3 = scan	
V22 > 5.9 and			
strong signal	2.5	2.5	16 μs
weak signal	2.5	2.5	9 μs
V22 < 5.3 and			
strong signal	7.5	7.5	16 μs
weak signal	7.5	7.5	9 μs

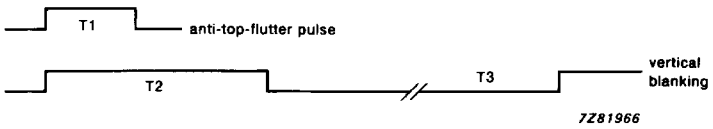
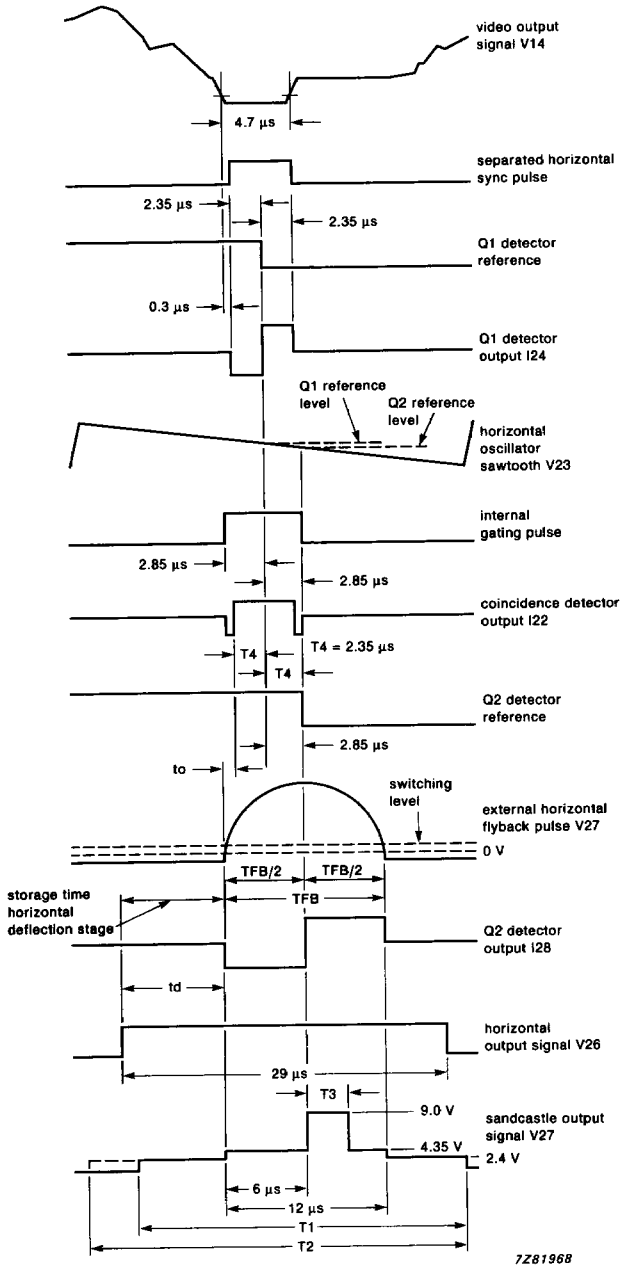


Fig. 6 Switching levels coincidence detector.

DEVELOPMENT DATA



	50 Hz	60 Hz
T1 – Search window	42P	34P
T2 – Narrow window	50P	42P
T3	3.8 µs	3.45 µs

Where: $P = \frac{1}{2 F_H}$

Fig. 7 Timing diagram.

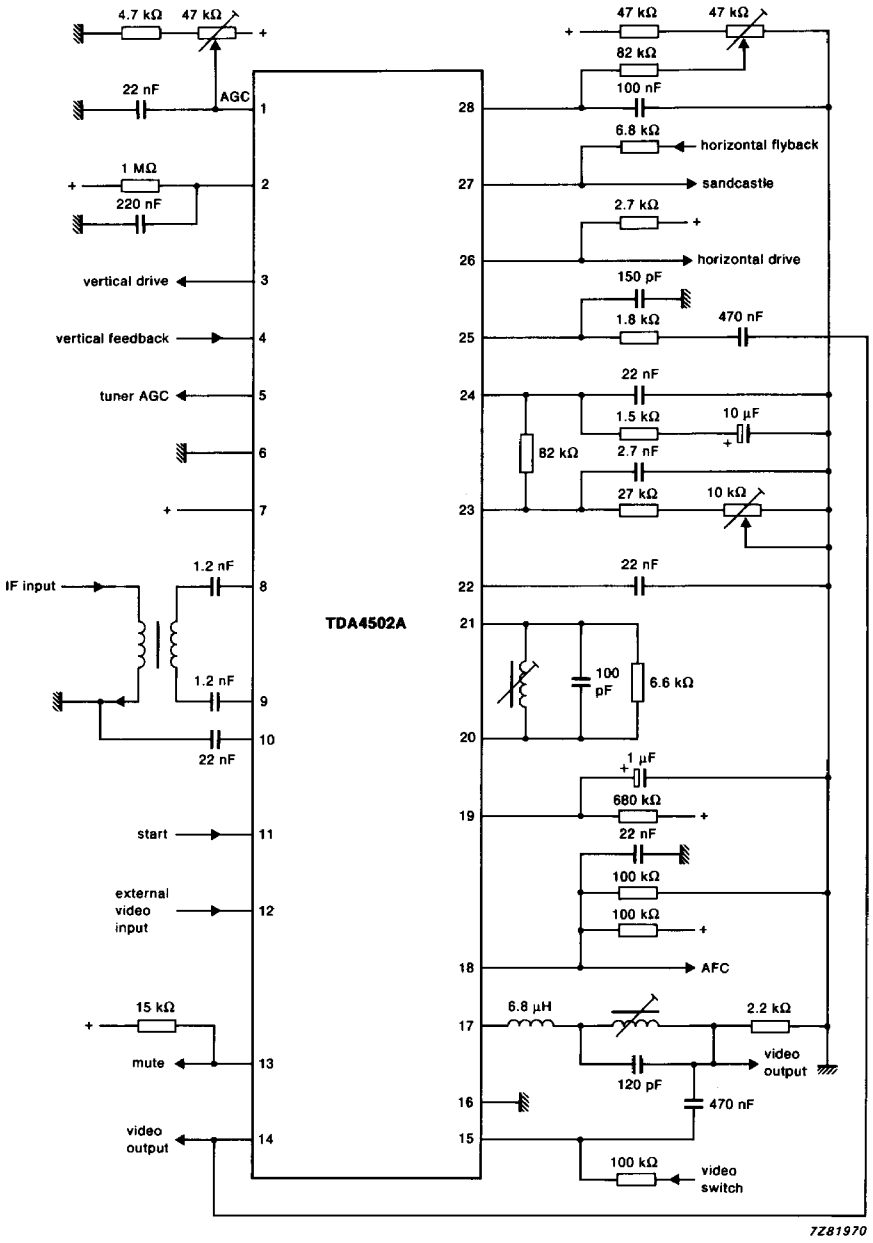


Fig. 8 Application diagram.