AN_8024C_067 December 2009

Teridian 73S8024C versus NXP TDA8024T

Introduction

This application note highlights the advantages of the Teridian 73S8024C compared with the NXP TDA8024T Smart Card Interface IC.

The Teridian 73S8024C is a single Smart Card Interface IC that provides all input and output signal interfaces as well as the power supply to the smart card. The Teridian 73S8024C implements an inductor-based DC-DC converter for the smart card power supply (V_{CC}). This DC-DC converter provides higher current capability, lower noise and higher efficiency than the charge pump based DC-DC converter of the similar NXP part. The 73S8024C requires only a single 3.3 V nominal power supply to comply with applicable standards for both 5 V or 3 V smart cards.

Package

The Teridian 73S8024C IC is available in a SO28 package, which is the same as and is pin compatible with the NXP TDA8024T. The only exception is the inductor input pin 5 (LIN). For applications that require a smaller PCB footprint than the SO28, Teridian offers the 73S8023C part in a tiny QFN32 package (5 mm x 5 mm), which consists of a super-set of the Teridian 73S8024C (extra pins for a Chip Select function, as well as for synchronous card support). Performance highlighted in this document for the Teridian 73S8024C device is applicable to the Teridian 73S8023C IC. Refer to the Teridian *73S8023C Data Sheet* for usage of the additional functions offered by this circuit. Note the pin numbers mentioned in this document are references to the Teridian 73S8024C SO28 package.

Replacement of the NXP TDA8024T

The Teridian 73S8024C easily replaces the TDA8024T with only a few minor modifications. New designs that use the Teridian IC allows operation with only a single 2.7 V to 3.6 V power supply while supporting any 3 V or 5 V card up to 100 mA. This permits removing the 5 V power supply from systems. Particular attention to the three technical points detailed below is all that is necessary to ensure a successful replacement. Refer to the next section of this document to learn more about other technical differences that may marginally affect the behavior of the application.

Required Changes

The Teridian 73S8024C uses an inductor based DC-DC converter, which requires a 10 μH inductor connected between the V_{PC} and Lin pins (6 and 5 respectively). This inductor must be capable of handling at least 400 mA of peak current.

The 220 nF low ESR capacitor, that is located on the PCB in close proximity to the card connector (connected to the pin 17) is replaced by a 1 μF low ESR cap when using the 73S8024C in ISO7816 or NDS environments. The capacitor should be placed close to the card connector.

Potential Cost Reduction Differences

The capacitor between pins 5 and 6 (the 100 nF low ESR charge pump capacitor of the TDA80x4 parts), and the capacitor connected to pin 8 (100 nF low ESR) can be removed.

The 100 nF capacitor between pins 17 and 14 is not necessary with the 73S8024C and can be removed, however the 1 μF capacitor should remain.

Note about the Use of Pin 18

Existing applications that utilize a NXP TDA8024T may implement an optional resistor bridge connected to pin 18. This allows matching of the operating voltage range of the smart card interface IC (V_{DD} digital power supply IN) to the supply voltage range of the system controller. In other words, when the power supply of the system drops, the card interface is deactivated at higher voltage than the system controller is. This feature is called "V_{DD} Fault Adjust" in the Teridian *73S8024C Data Sheet*.

To meet the exact voltage range (or V_{DD} fault value), the two resistor values must be slightly modified. Refer to the respective data sheets for exact calculation of these resistors.

Advantages

1. **Improved Noise Performance.** The Teridian 73S8024C Smart Card Interface chip uses an inductor based DC/DC converter for the smart card power supply (V_{CC}), while the NXP TDA8024T device use a capacitor based DC/DC converter which generates higher levels of switching-noise. The advantages of the Teridian 73S8024C can easily be seen when monitoring and comparing the noise on the ground (pins 4, 14, and 22) and supply (pins 6 and 21) pins against those of the NXP parts.

   The comparisons shown below between the Teridian 73S8024C and NXP TDA8024T were measured on the same reference PCB. The Teridian 73S8024C had as much as nine times less noise on the supply and ground pins. Table 1 shows the actual measurements and the oscilloscope captures (on pages 3 and 4) clearly show the superior performance of the Teridian 73S8024C IC.

Table 1: Noise Comparison

	Inductor Base DC-DC Converter Teridian 73S8024C	**Charge Pump Based DC/DC Converter NXP TDA8024T**	**Figure #**
	Peak-to-Peak [mVpp]	Peak-to-Peak [mVpp]	
GND (Pin 4)	75	125	**Fig. 1, 2**
GND (Pin 14)	45	100	**Fig. 3.4**
GND (Pin 22)	55	125	**Fig. 5,6**
VPC/VDDp (Pin 6)	88	808	**Fig. 7,8**
VDD (Pin 21)	98	121	**Fig. 9,10**

Test Conditions

V_{PC}/V_{DDP} (Pin 6) = 5.0 / 3.3 [V] (for the NXP TDA8024T and Teridian 73S8024C respectively)
V_{DD} (Pin 21) = 3.3 [V]
I_{CC} (@V_{CC})~ 55 mA
Ta: Room temperature

All signals are measured with respect to a pre-defined reference point (GND on test PCB).

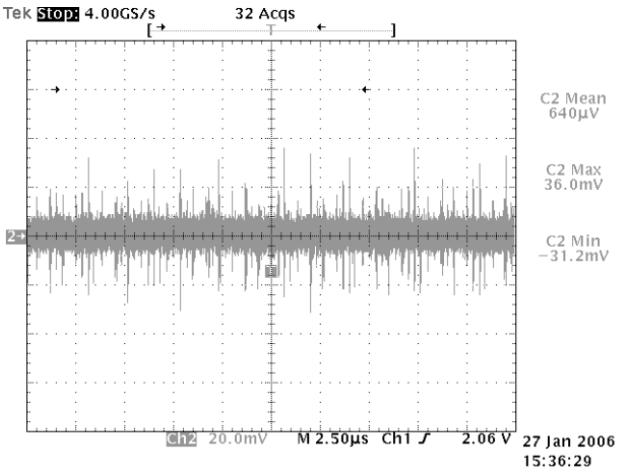


Figure 1: Teridian 73S8024C, GND (Pin 4)

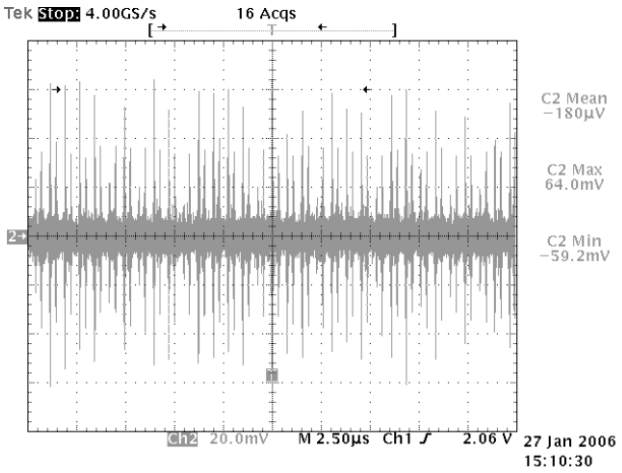


Figure 2: NXP TDA8024T, GND (Pin 4)

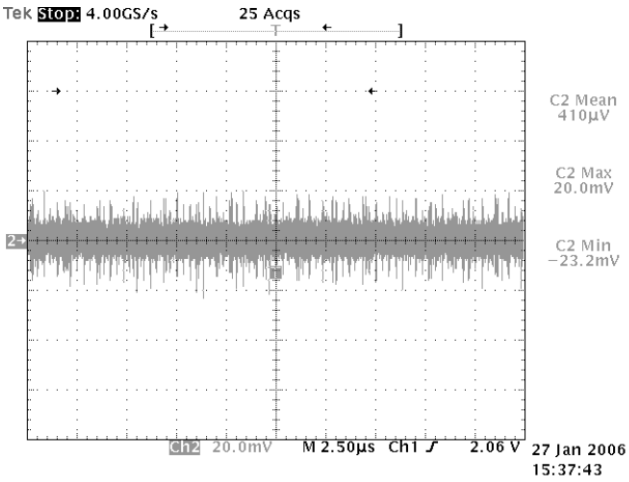


Figure 3: Teridian 73S8024C, GND (Pin 14)

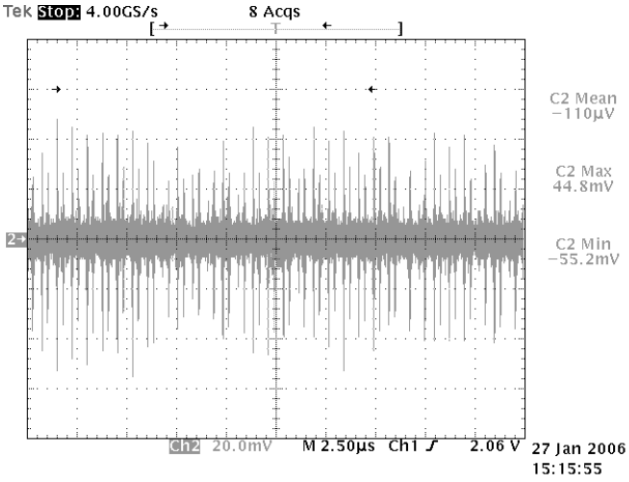


Figure 4: NXP TDA8024T, GND (Pin 14)

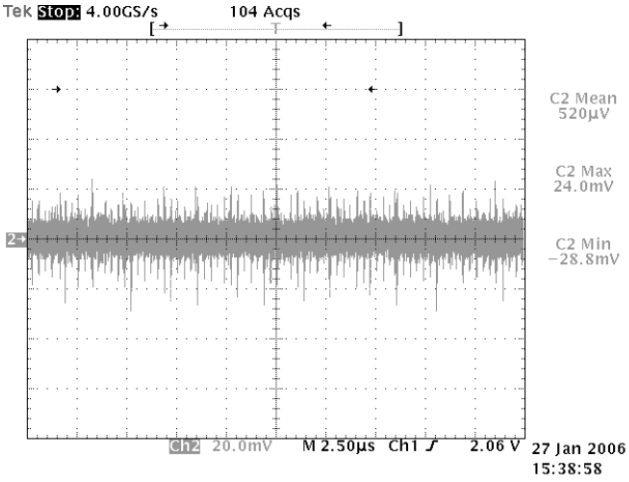


Figure 5: Teridian 73S8024C, GND (Pin 22)

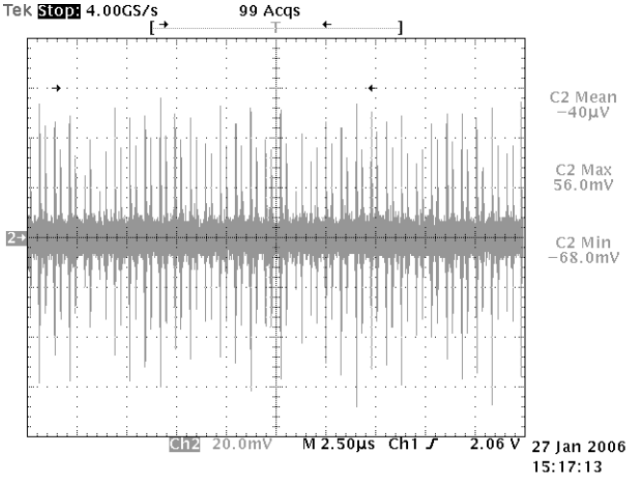
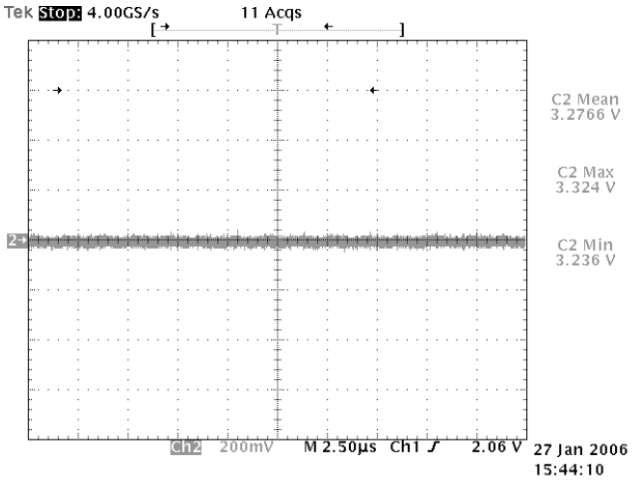


Figure 6: NXP TDA8024T, GND (Pin 22)



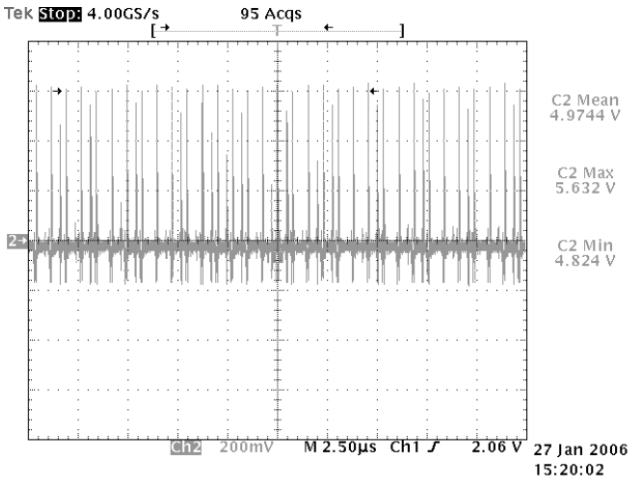
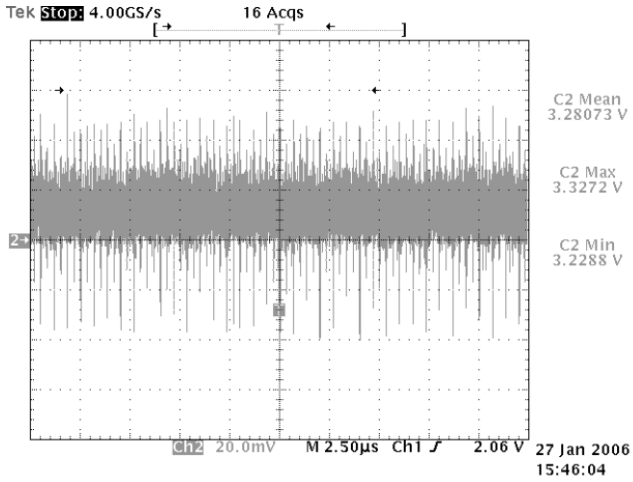


Figure 7: 73S8024C VPC, Regulator Supply (Pin 6) **Figure 8: TDA8024T V_{DDP}, DC/DC Converter Power Supply (Pin 6)**



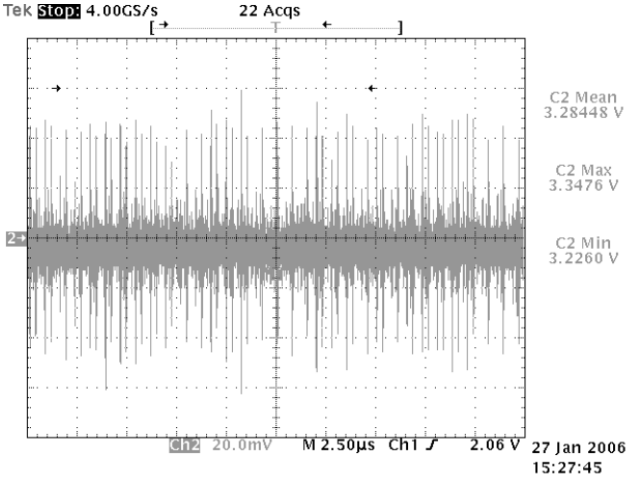


Figure 9: 73S8024C V_{DD} Digital Power Supply (Pin 21) **Figure 10: TDA8024T, V_{DD} Digital Power Supply (Pin 21)**

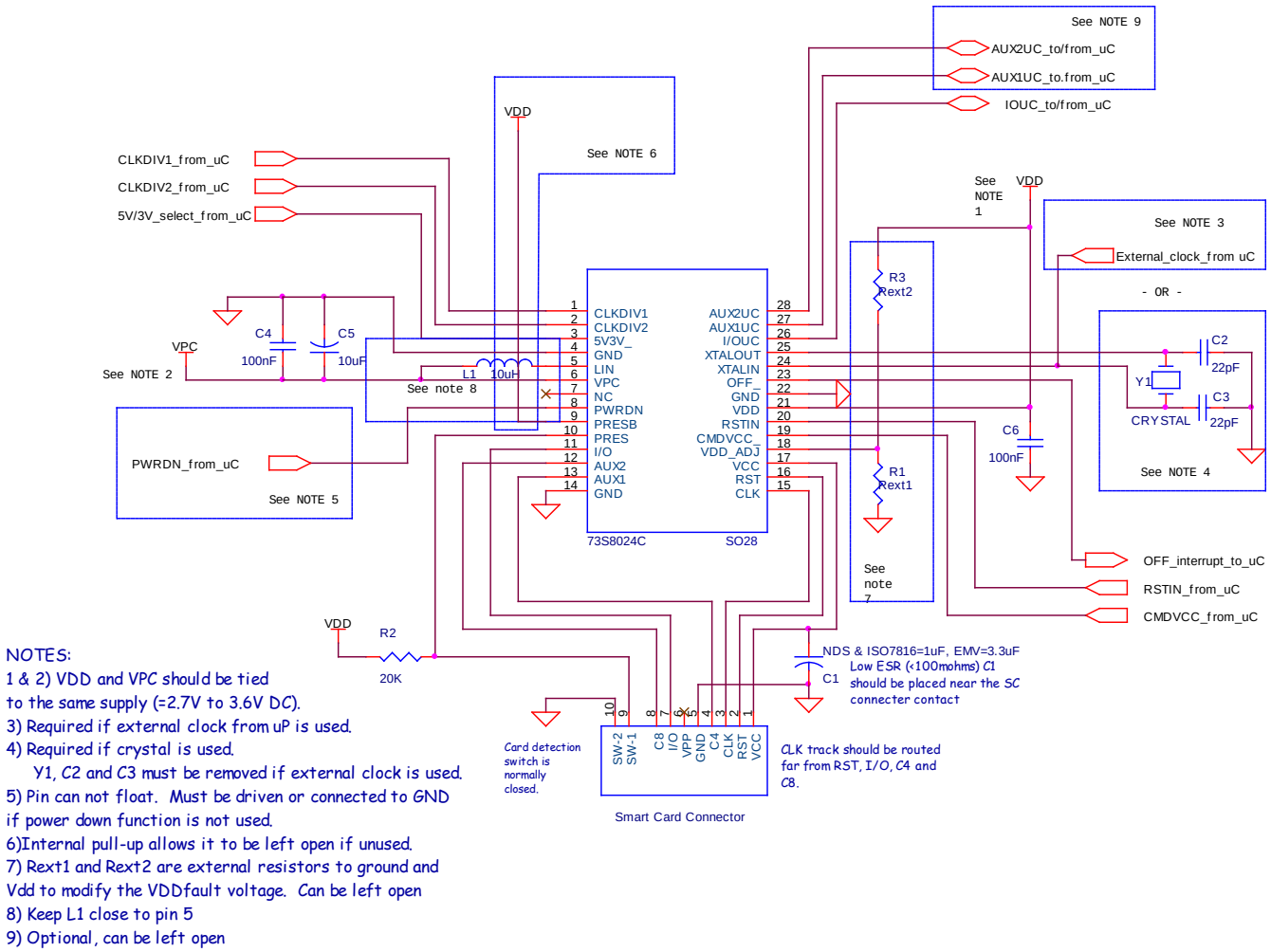
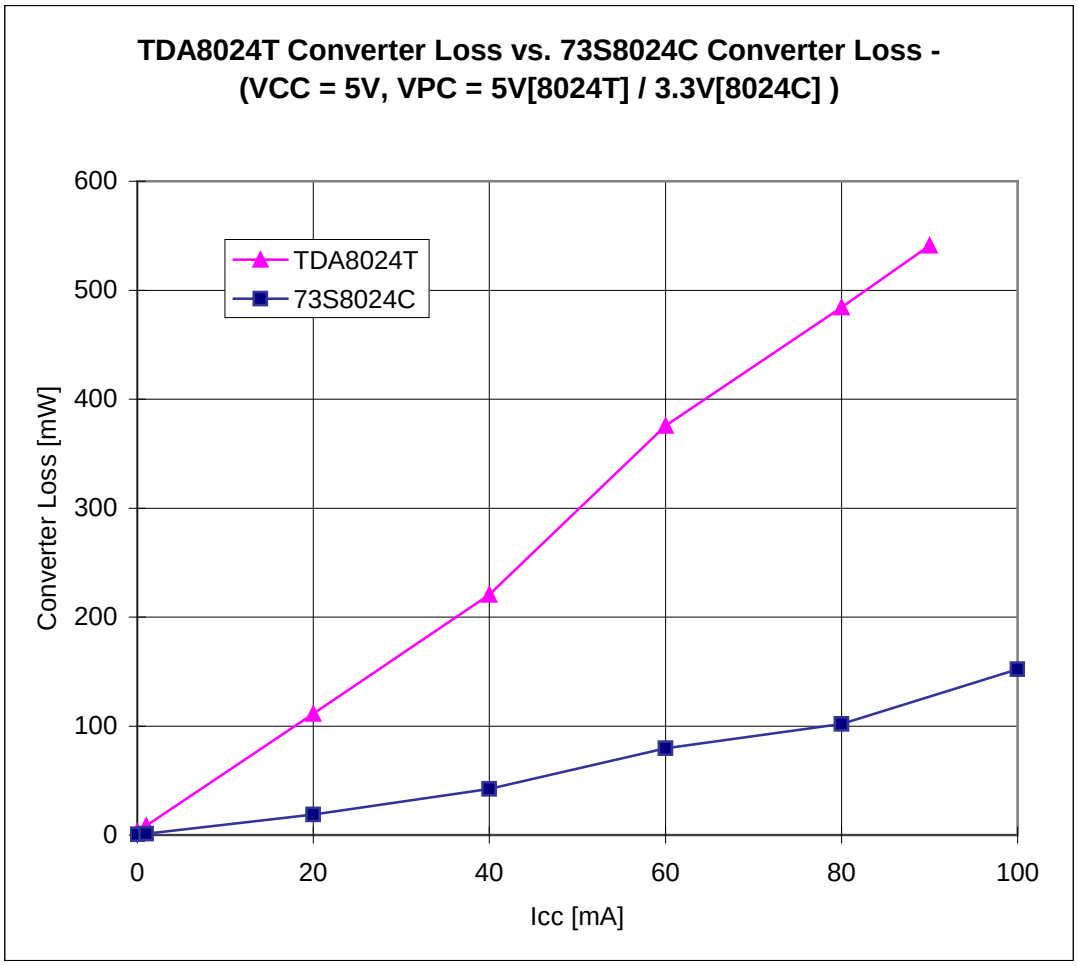


Figure 11: Teridian 73S8024C Application Schematic

2. **Improved Card Power Supply Efficiency.** The following graph shows the converter loss difference between the NXP TDA8024T and the Teridian 73S8024C. It is obvious that the 73S8024C is much more efficient than the TDA8024T over the load range.



3. **3.3 Volt Only Operation**. The Teridian 73S8024C Smart Card Interface IC allows true 3.3 V only operation (down to 2.7 V minimum) for all Vcc loads to 100 mA. This eliminates the 5 V supply in many applications. The NXP TDA8024T needs a 5 V supply for the DC/DC converter for those applications that require Vcc supply current over 20 mA and thus cannot operate as a 3.3 V only device. The NXP TDA8024T specifies that V_{DDP} (V_{PC} on the Teridian 73S8024C) must be greater than 3.0V for Icc < 20 mA and greater than 4V for 20 mA < Icc < 80 mA.

4. **Feature Enhancements.**

   a. **Smart Card Power Down Mode**

   The Teridian 73S8024C has a smart card power-down mode that is controlled by pin 8 (PWRDN) of the SO28 package. This pin is used to connect the DC/DC converter capacitor in the NXP TDA8024T. A logic high signal on this pin will place the 73S8024C into a power saving mode. This mode is only available outside of a card session and consumes less than 5 μA on Vdd and V_{PC} . This pin must be connected to ground if the Power Down Mode is not required.

b. Adjustment of the V_{DD} Fault Threshold Voltage

By default, the Teridian 73S8024C, in common with the NXP TDA8024T, begins an automatic deactivation sequence of the smart card when the digital power supply (V_{DD}) drops below a threshold value. This value is trimmed at the factory to be 2.3 V ±0.1 V. In some applications, it might be desirable to have a different voltage threshold (to deactivate the card earlier for instance). The Teridian 73S8024C provides the option to modify this threshold value by connecting an external resistor to the V_{DDF_ADJ} pin. Either a single resistor from the V_{DDF_ADJ} pin to ground or two resistors, one from the V_{DDF_ADJ} pin to ground and the other from V_{DDF_ADJ} to V_{DD}, can be used to adjust the V_{DD} fault level. This single resistor option is simpler, but the trigger threshold is less accurate than the two resistor option. Refer to the Teridian *73S8024C Data Sheet* for further detail. This feature is supported by the NXP TDA8024T, but requires different resistor value(s) for the same threshold voltage. When unused, pin 18 on the Teridian 73S8024C must be left unconnected.

c. Sequencer (Activation)

Unlike the NXP TDA8024T, the Teridian 73S8024C IC internally generates the EMV 4.0 compliant CLK to RST delay at activation. The related timing differences between 73S8024C and NXP TDA8024T are:

- With the Teridian 73S8024C, the CLK doesn't start unless RSTIN goes low. There is no timeout for this event. In this manner, the host processor easily controls the CLK start. The NXP TDA8024T has a small window between 50 and 220 μs where the falling edge of RSTIN can start CLK. After 220 μs the CLK will start regardless of the state of RSTIN.
- The Teridian 73S8024C automatically asserts 42,000 CLK cycles of RST delay at activation. Negative pulse width on RSTIN can be shorter than this delay. The NXP TDA8024T does not provide any delay; RST is active immediately after the CLK starts.
- Activation is invoked by negating $\overline{\text{CMDVCC}}$. CLK start timing depends on RSTIN fall timing. Three cases for CLK starts are illustrated in Figure 12.

    - Case 1:RSTIN goes low when $t < T_0$
      Teridian 73S8024C – CLK starts at T_1 (approximately 600 μs after $\overline{\text{CMDVCC}}$ goes low).
      NXP TDA8024T – CLK starts between 50.2 and 130.2 μs.

    - Case 2: RSTIN goes low when $T_0 < t < T_1$
      Teridian 73S8024C – CLK starts at T_1. If RSTIN is de-asserted (rises) before T_1, it is ignored and CLK and I/O stay low until next RSTIN de-assertion (same as case 3).
      NXP TDA8024T – There is a window between 50 and 220 μs where the falling edge of RSTIN can start CLK.

    - Case 3: RSTIN goes low when $t > T_1$
      Teridian 73S8024C – CLK starts at RSTIN fall timing.
      NXP TDA8024T – CLK starts 220μs from falling edge of $\overline{\text{CMDVCC}}$.

RST de-assertion (RST rising)
Teridian 73S8024C – RST is de-asserted at 42,000 CLK cycles (T_2) after CLK start if RSTIN becomes high before T_2 (A). If RSTIN goes high after T_2, RST is de-asserted at RSTIN rising as demonstrated in (B). In this manner, the 42,000 clock-cycle delay, as per EMV 4.0 and ISO7816-3 is ensured by the Teridian 73S8024C, and longer delay can also be CLK to RST delay can be controlled by the system controller.
NXP TDA8024T – After CLK has started, RST will track RSTIN.

The Teridian 73S8024C activation sequence and its controlling host firmware are fully compatible with the TDA8024T (as long as the RSTIN line is asserted and de-asserted by the host after time T_2).

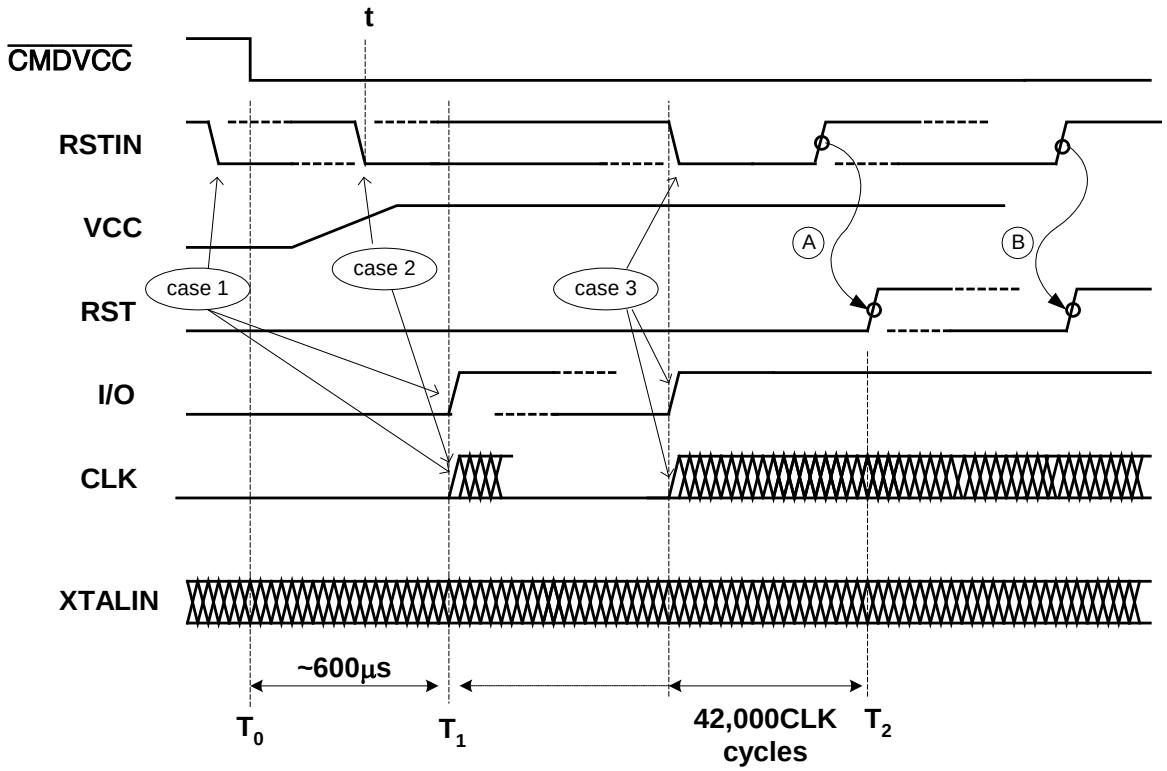


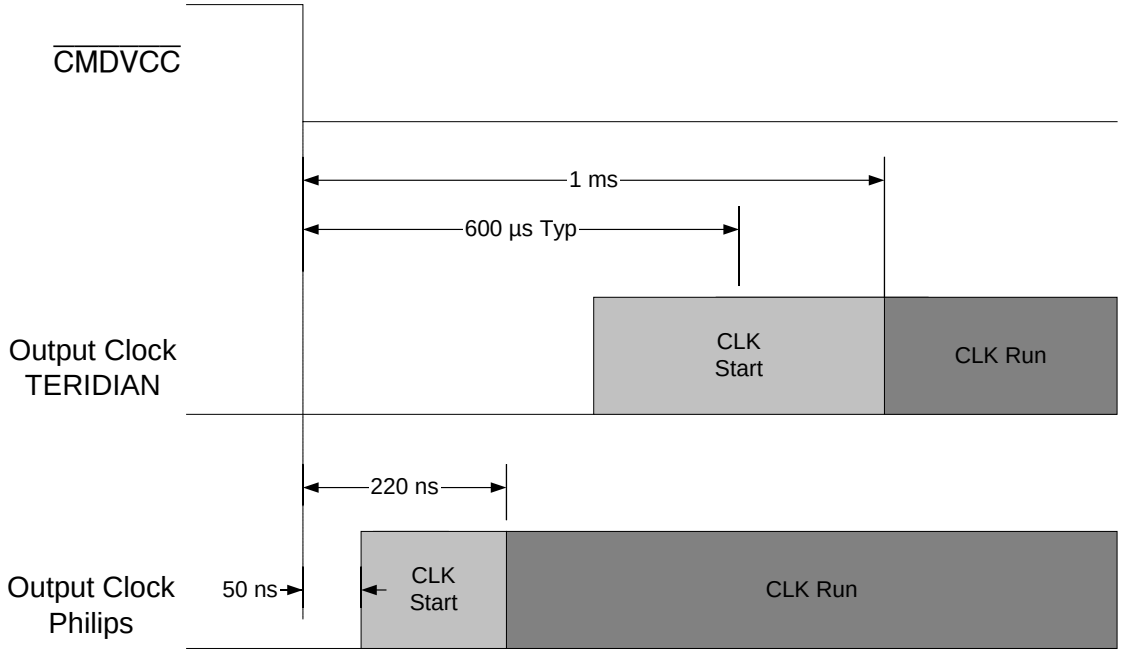
Figure 12: Teridian 73S8024C Activation Sequence

Reset Signal Precautions

Due to activation sequence timing differences between the NXP TDA8024T and the Teridian 73S8024C, there is a possibility of an ATR timeout error occurring with the Teridian 73S8024C when it replaces the NXP TDA8024T in an application. This potential error can be eliminated by simply by extending the ATR timeout by a small amount. This extension is legal under EMV, ISO and NDS specifications. The following sections will describe these differences and the necessary modifications in detail.

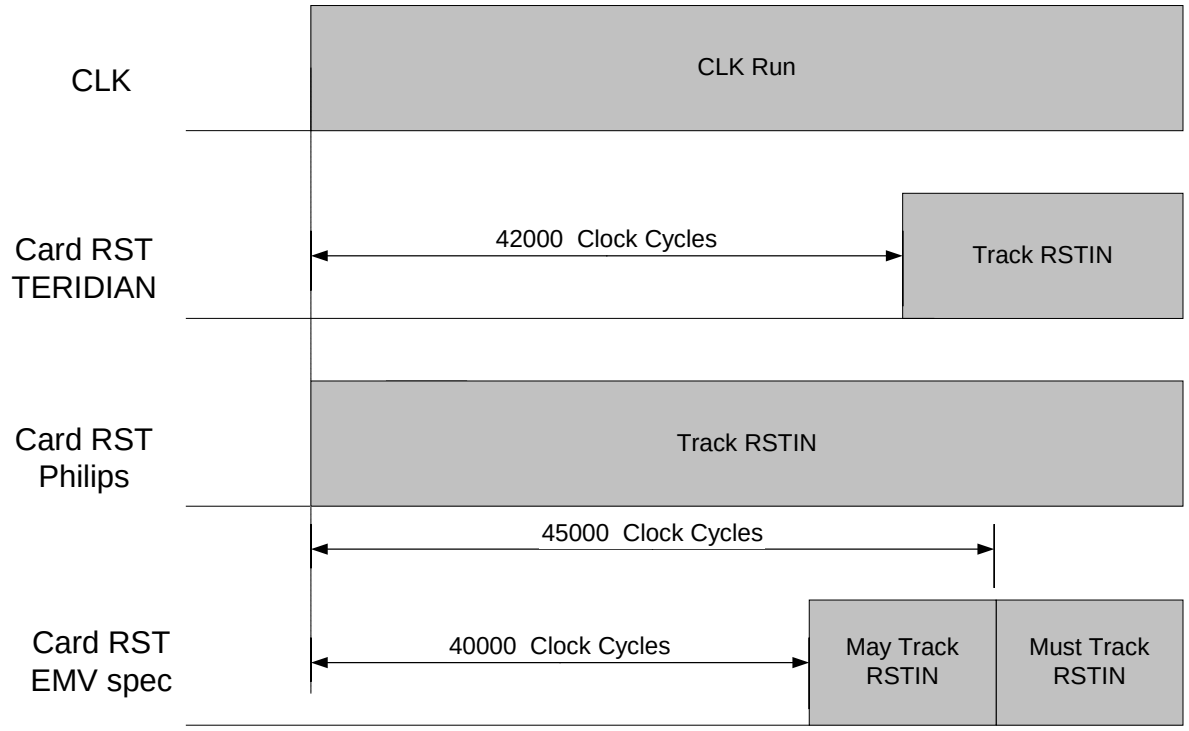
Clock Start Timing Differences

The NXP TDA8024T will start the card CLK between 50 ns and 200 ns after the falling edge of $\overline{\text{CMDVCC}}$, whereas the Teridian 73S8024C will start the CLK around 600 µs after. The specification for the Teridian 73S8024C is 1 ms maximum. As a result, the Teridian 73S8024C CLK signal can start as much as 1 ms – 50 ns = **999.95 µs** (worst case maximum) after the NXP TDA8024T.



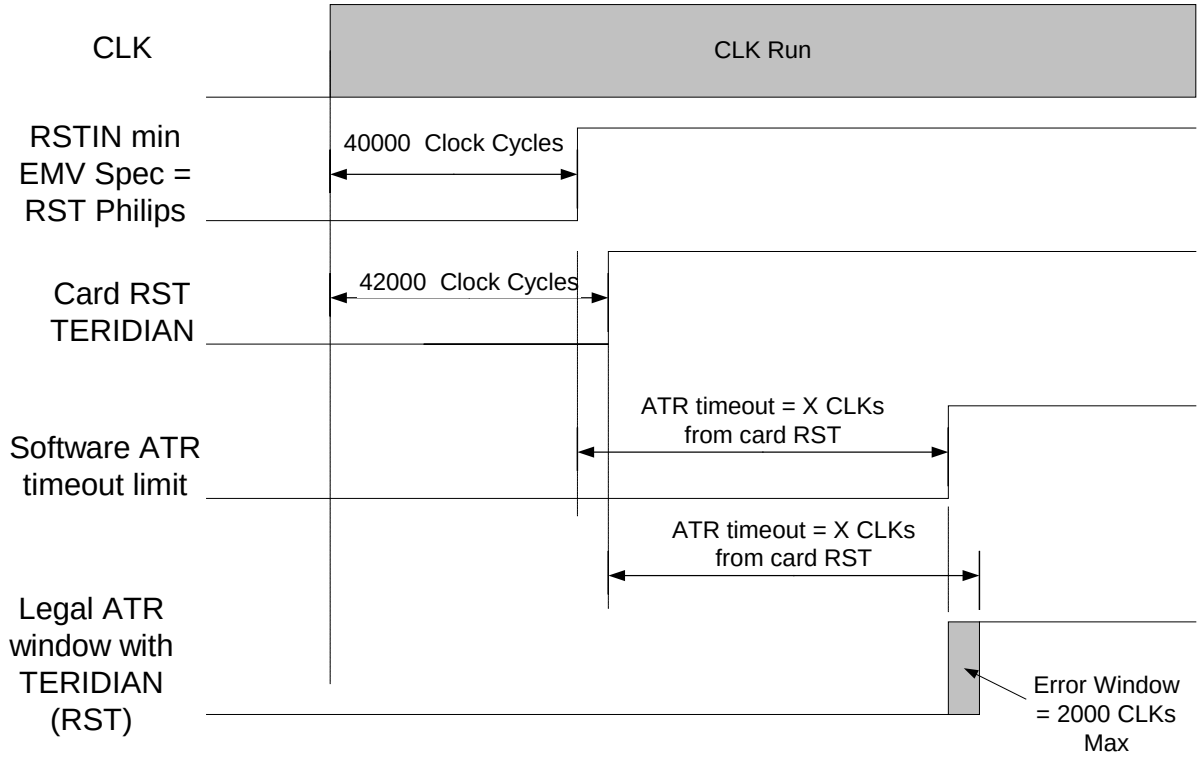
RST Timing Differences

The NXP TDA8024T doesn't have any built-in RST out delay with respect to CLK. As a result, the system controller must generate the RSTIN signal somewhere between 40000 and 45000 clock cycles after the CLK signal starts (EMV specification). The Teridian 73S8024C will delay the RST signal at least 42000 clock cycles after CLK starts. If the system controller de-asserts RSTIN after 42000 clock cycles, the timing of the rising edge of RST is the same between the NXP TDA8024T and the Teridian 73S8024C.



Once card RST is de-asserted, the system controller expects an ATR response from the card within a certain window of time. If the ATR is not properly received before the end of this window an ATR timeout error will occur.

With the NXP TDA8024T, this timeout starts at the rising edge of RSTIN. If the system controller de-asserts RSTIN between 40000 and 42000 clock cycles after CLK starts, the card RST signal timing will be different between the NXP TDA8024T and the Teridian 73S8024C.



Due to the timing difference between the devices in the case of RSTIN being de-asserted between 40000 and 42000 clock cycles after CLK, there is a delay between RSTIN and card RST up to 2000 clock cycles. This means that a card can respond with a valid ATR response (with respect to card RST) and still generate an ATR timeout error (with respect to RSTIN)

This 2000 clock cycle difference in addition to the maximum 950 us clock start timing differential need to be added to the ATR timeout to insure the ATR timeout error will not be generated when the card responds with a valid ATR response.

Pin Comparison

Table 2 lists the 28 pins of the Teridian 73S8024C device (SO28) and of the NXP TDA8024T device. The Comments column describes the system-level differences that should be taken into account when the Teridian 73S8024C is used as a replacement or for dual-source designs.

Table 2: Pin Comparison

Pin No.	Interface	Pin Name		Comments
		73S8024C	TDA8024T	
11	Smart-Card	I/O	I/O	Internal Pull-up to VCC: 11 kΩ.
13		AUX1	AUX1	
12		AUX2	AUX2	
16		RST	RST	
15		CLK	CLK	
10		PRES	PRES	All devices include static high-impedance pull-down/up resistors to allow No-Connect when unused
9		$\overline{\text{PRES}}$	$\overline{\text{PRES}}$	
17		VCC	VCC	73S8024C: Decouple to GND with a 1 μF low ESR capacitor. TDA8024T: Requires 220 nF + 100 nF decoupling capacitor.
14		GND	CGND	
19	System Controller	$\overline{\text{CMDVCC}}$	$\overline{\text{CMDVCC}}$	
3		5V/$\overline{\text{3V}}$	5V/$\overline{\text{3V}}$	73S8024C: Can be left open for 5 V card operation TDA8024T: Must pulled-up for 5 V card operation
7		NC	S1	73S8024C: No Connect TDA8024T / TDA8024T: Return connection for charge pump capacitor.
8		PWRDN	VUP	73S8024C: Power-Down mode when pulled high. This mode is allowed only out of a card session. Must be tied low when power-down mode not used. TDA8024T: Requires 1 x 100 nF low ESR decoupling capacitor to PGND.
1		CKDIV1	CLKDIV1	Teridian 73S8024C has high impedance pull-down
2		CKDIV2	CLKDIV2	Teridian 73S8024C has high impedance pull-down
23		$\overline{\text{OFF}}$	$\overline{\text{OFF}}$	Interrupt output Internal Pull-up to Vdd: 20 kΩ.
20		RSTIN	RSTIN	
26		I/OUC	I/OUC	Internal Pull-up to VDD: 11 kΩ.
27		AUX1UC	AUX1UC	
28		AUX2UC	AUX2UC	

Table 2: Pin Comparison (continued)

Pin No.	Interface	Pin Name		Comments
		73S8024C	TDA8024T	
24	Power Supply and Misc.	XTALIN	XTAL1	
25		XTALOUT	XTAL2	
18		V_{DDF_ADJ}	PORADJ	This pin can optionally be used in 73S8024C and TDA8024T to modify the voltage threshold level of the internal voltage supervisor to deactivate the card interface. With both parts, this pin can be left open to retrieve the default threshold level: 73S8024C: 2.3 V TDA8024T: 2.45 V Connecting an external resistor network to pin 18 allows modification of the V_{DD} fault threshold level. Refer to respective data sheets for determination of the resistor value (different values between 73S8024C and TDA8024T).
5		LIN	S2	73S8024C: 10 µH inductor connecter between this pin and VPC. TDA8024T: Requires 1 x 100 nF low ESR Charge Pump capacitor.
21		V_{DD}	V_{DD}	73S8024C: V_{DD} = 2.7 V to 3.6 V. TDA8024T: V_{DD} = 2.7 V to 6.5 V.
6		V_{PC}	V_{DDP}	73S8024C: V_{PC} = 2.7 V to 3.6 V TDA8024T: V_{DDP} =4.0 V to 6.5 for Icc < 80 mA Both devices require 1 x 100 nF decoupling capacitor.
4		GND	PGND	
22		GND	GND	

Revision History

Revision	Date	Description
1.0	2/14/2006	First publication.
1.1	12/4/2009	Formatted to the Teridian documentation style. Replaced all instances of “Philips” with “NXP”. Assigned document number AN_8024C_067. Miscellaneous editorial changes.