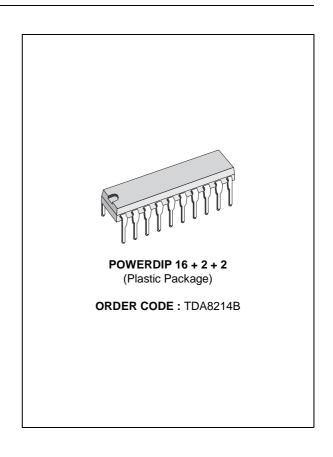


TDA8214B

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

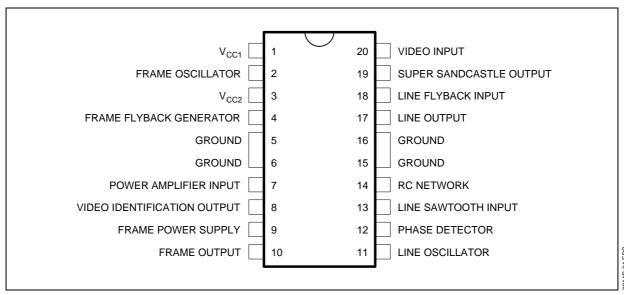
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPA-BILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VIDEO IDENTIFICATION CIRCUIT
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE



DESCRIPTION

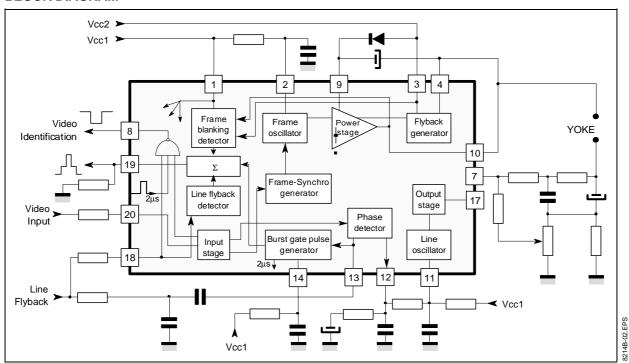
The TDA8214B is an horizontal and vertical deflection circuit with super sandcastle generator and video identification output. Used with TDA8213 (Video & Sound IF system) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS



September 1993 1/9

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC} 1	Supply Voltage	30	V
V _{CC} 2	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
I10 _{NR}	Frame Output Current (non repetitive)	± 1.5	Α
I10	Frame Output Current (continuous)	± 1	Α
V17	Line Output Voltage (external)	60	V
I _P 17	Line Output Peak Current	0.8	Α
Ic17	Line Output Continuous Current	0.4	Α
T_{STG}	Storage Temperature	-40 to + 150	°C
TJ	Max Operating Junction Temperature	+ 150	°C
T _{AMB}	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{TH(j-c)}	Max Junction-case Thermal Resistance	10	°C/W
R _{TH(j-a)}	Typical Junction-ambient Thermal Resistance (Soldered on a 35μm thick 45cm² PC Board copper area)	40	°C/W
TJ	Max Recommended Junction Temperature	120	°C

TBL



ELECTRICAL CHARACTERISTICS

 $V_{CC1} = 10V$, $T_{AMB} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit
SUPPLY (I	Pin 1)	-		Į.	
I _{CC1}	Supply Current		15		mA
V _{CC1}	Supply Voltage	9	10	10.5	V
	PUT (Pin 20)				
V20	Reference Voltage (I20 = -1μA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (When synchronized with TTL signal)	50	1.75		μs
	ILLATOR (Pin 11)	- 50			μο
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current	0.4	100	7.0	nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period	62	64	66	μs
1 = 1	(R = 34.9kΩ Tied to V _{CC1} , C = 2.2nF Tied to Ground)	02	01	00	μο
FLP2	Free Running Line Period (R = $13.7K\Omega$, C = $2.2nF$)		27		μs
OT11	Oscillator Threshold for Line Output, Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUT	PUT (Pin 17)	·			
LV17	Saturation Voltage (I ₁₇ = 200mA)		1.1	1.6	V
OPW	Output Pulse width (line period = 64µs)	27	29	31	μs
LINE SAW	TOOTH INPUT (Pin 13)				
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DE	TECTOR (Pin 12)	-			
l12	Output Current During Synchro Pulse	250	350	500	μΑ
RI12	Current Ratio (positive/negative)	0.95	1	1.05	P
LI12	Leakage Current	-2		+2	μΑ
CV12	Control RangeVoltage	2.60		7.10	·V
VIDEO IDE	ENTIFICATION (Pin 8)		1	l .	
	Low Level Output when the line syn. tip is centered in the line retrace				
V _{H8}	Without video signal (I ₈ = -500μA)	4.5	6.3		V
V _{L8}	With video signal ($I_8 = 50\mu A$)		0.6	0.9	V
	SCILLATOR (Pin 2)				
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = $845k\Omega$ Tied to V_{CC1} , C = $180nF$ Tied to Ground	20.5	23	25	ms
MFP	Minimum Frame Period (I20 = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period (R = $408k\Omega$, C = $220nF$)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10 ⁻³		Hz/°C

ELECTRICAL CHARACTERISTICS (continued)

 $V_{CC1} = 10V$, $T_{AMB} = 25^{\circ}C$ (unless otherwise specified)

FRAME POWER SUPPLY (Pin 9) V9 Operating Voltage (with flyback Generator) 10 1 58 V 19 Supply Current (V9 = 30V) Vcc2 Operating Voltage 10 30 V FRAME OUTPUT (Pin 10) Saturation Voltage to Ground (V9 = 30V) LV10A 110 = 0.1A LV10B 110 = 0.1A HV10B 110 = -1A Saturation Voltage to V9 (V9 = 30V) HV10B 110 = -1A Saturation Voltage to V9 (V9 = 30V) HV10A 110 = 0.1A FV10B 110 = 0.1A FV10B 110 = 0.1A FV10B 110 = 1A Saturation Voltage to V9 in Flyback Mode (V10 > V9) FV10B 110 = 1A Saturation Voltage to V9 in Flyback Mode (V10 > V9) FV10B 110 = 1A Saturation Voltage to V9 in Flyback Mode (V10 > V9) FV10B 110 = 1A FV10B 110 = 1A Saturation Voltage to V9 in Flyback Mode (V10 > V9) FV2BACK GENERATOR (Pin 3 and Pin 4) Flyback Transistor on (output = high state), Vcc2 = 30V V4/3 with FZDA I _A → 3 = 0.1A FZDA I _A → 3 = 0.1A FSVB I ₃ → 4 = 1A SUPER SANDCA STILE OUTPUT (Pin 19) Output Voltages (R load = 2.2kΩ) SANDT2 Frame blanking pulse level SANDT2 Frame blanking pulse level BGS Delay between middle of sync pulse and leading edge of burst key pulse Vertical blanking pulse level SANDCA Line blanking pulse level SCS Delay between middle of sync pulse and leading edge of burst key pulse Vertical blanking pulse width Line FLYBACK INPUT (Pin 18) Switching level Switching level Switching level A CR network time constant (Note 2) F RO Rever time constant (Note 2)	Symbol	Parameter	Min.	Тур.	Max.	Unit
19	FRAME PO	WER SUPPLY (Pin 9)			1	
19	V9	Operating Voltage (with flyback Generator)	10		58	V
FLYBACK GENERATOR SUPPLY (Pin 3) V _{CC2} Operating Voltage 10 30 V FRAME OUTPUT (Pin 10) Saturation Voltage to Ground (V9 = 30V) LV10B I10 = 0.1A 0.06 0.6 V LV10B I10 = 1A 0.37 1 V Saturation Voltage to V9 (V9 = 30V) HV10A I10 = -0.1A 1.3 1.6 V HV10B I10 = -0.1A 1.6 2.1 V FV10B I10 = 0.1A 1.6 2.1 V FV10B I10 = 1A 1.6 2.1 V FV10B I10 = 1A 1.6 2.1 V FV10B I10 = 1A 1.5 2.1 V FV10B I10 = 1A 1.5 2.1 V FV24BCK GENERATOR (Pin 3 and Pin 4) 1.5 2.1 V FIYBBCK Transistor on (output = high state), V _{CC2} = 30V V4/3 with 1.5 2.1 V FYPABCK Transistor on (outp	19			11		mA
FRAME OUTPUT (Pin 10)	FLYBACK (1	1	
Saturation Voltage to Ground (V9 = 30V)	V _{CC2}	Operating Voltage	10		30	V
LV10A I10 = 0.1A 0.06 0.6 V LV10B I10 = 1A 0.37 1 V Saturation Voltage to V9 (V9 = 30V)	FRAME OU	TPUT (Pin 10)				
LV10A I10 = 0.1A 0.06 0.6 V LV10B I10 = 1A 0.37 1 V Saturation Voltage to V9 (V9 = 30V)		Saturation Voltage to Ground (V9 = 30V)				
Saturation Voltage to V9 (V9 = 30V) HV10A 110 = -0.1A	LV10A			0.06	0.6	V
HV10A I10 = -0.1A 1.3 1.6 V HV10B I10 = -1A 1.7 2.4 V Saturation Voltage to V9 in Flyback Mode (V10 > V9) FV10A I10 = 0.1A 1.6 2.1 V FV10B I10 = 1A 2.5 4.5 V FLYBACK GENERATOR (Pin 3 and Pin 4) Flyback Transistor on (output = high state), V _{CC2} = 30V V4/3 with F2DA I ₄ → 3 = 0.1A 1.5 2.1 V F2DB Is 1 → 3 = 1A 3.0 4.5 V Flyback Transistor on (output = high state), V _{CC2} = 30V V3/4 with FSVA I ₃ → 4 = 0.1A 0.8 1.1 V FSVA I ₃ → 4 = 0.1A 0.8 1.1 V FSVA I ₃ → 4 = 0.1A 0.8 1.1 V FSVA I ₃ → 4 = 1A 0.8 1.1 V FSVA I ₃ → 4 = 1A 0.8 1.1 V FISHBACK Transistor of (output = V9 - 8V), V9 - V _{CC2} = 30V FOLIC Leakage Current Pin 3 <t< td=""><td>LV10B</td><td>I10 = 1A</td><td></td><td>0.37</td><td>1</td><td>V</td></t<>	LV10B	I10 = 1A		0.37	1	V
HV10A I10 = -0.1A 1.3 1.6 V HV10B I10 = -1A 1.7 2.4 V Saturation Voltage to V9 in Flyback Mode (V10 > V9) FV10A I10 = 0.1A 1.6 2.1 V FV10B I10 = 1A 2.5 4.5 V FLYBACK GENERATOR (Pin 3 and Pin 4) Flyback Transistor on (output = high state), V _{CC2} = 30V V4/3 with F2DA I ₄ → 3 = 0.1A 1.5 2.1 V F2DB Is 1 → 3 = 1A 3.0 4.5 V Flyback Transistor on (output = high state), V _{CC2} = 30V V3/4 with FSVA I ₃ → 4 = 0.1A 0.8 1.1 V FSVA I ₃ → 4 = 0.1A 0.8 1.1 V FSVA I ₃ → 4 = 0.1A 0.8 1.1 V FSVA I ₃ → 4 = 1A 0.8 1.1 V FSVA I ₃ → 4 = 1A 0.8 1.1 V FISHBACK Transistor of (output = V9 - 8V), V9 - V _{CC2} = 30V FOLIC Leakage Current Pin 3 <t< td=""><td></td><td>Saturation Voltage to V9 (V9 = 30V)</td><td></td><td>1</td><td></td><td></td></t<>		Saturation Voltage to V9 (V9 = 30V)		1		
Saturation Voltage to V9 in Flyback Mode (V10 > V9) FV10A 110 = 0.1A	HV10A			1.3	1.6	V
FV10AI10 = 0.1A1.62.1VFV10BI10 = 1A2.54.5VFLYBACK GENERATOR (Pin 3 and Pin 4)Flyback Transistor on (output = high state), $V_{CC2} = 30V$ V4/3 withF2DA $I_4 \rightarrow 3 = 0.1A$ 1.52.1VF2DB $I_4 \rightarrow 3 = 1A$ 3.04.5VFSVA $I_3 \rightarrow 4 = 0.1A$ 0.81.1VFSVB $I_3 \rightarrow 4 = 1A$ 0.81.1VFVBock Transistor off (output = V9 - 8V), V9 - V _{CC2} = 30VFCILeakage Current Pin 3170μASUPER SANDCASTLE OUTPUT (Pin 19)Output Voltages (R load = 2.2kΩ)SAND12Frame blanking pulse level22.53VSANDL2Line blanking pulse level44.55VBG2Burst key pulse level89VPulses width and timingSC3Delay between middle of sync pulse and leading edge of burst key pulse2.32.73.1μsSC2Duration of burst key pulse Vertical blanking pulse width2.32.73.1μsLINE FLYBACK INPUT (Pin 18)Switching level2VMaximum imput current at V _{PEAK} = 800V8mALimiting voltage at maximum current4.3V	HV10B	I10 = -1A		1.7	2.4	V
FV10B I10 = 1A		Saturation Voltage to V9 in Flyback Mode (V10 > V9)		•		
FLYBACK GENERATOR (Pin 3 and Pin 4) Flyback Transistor on (output = high state), $V_{CC2} = 30V \ V4/3 \ with$ F2DA $ 1_4 \rightarrow 3 = 0.1A$	FV10A	I10 = 0.1A		1.6	2.1	V
Flyback Transistor on (output = high state), $V_{CC2} = 30V \ V4/3 \ with$ F2DA $I_4 \rightarrow 3 = 0.1A$	FV10B	I10 = 1A		2.5	4.5	V
F2DA $I_4 \rightarrow_3 = 0.1A$ 1.52.1VF2DB $I_{4\rightarrow3} = 1A$ 3.04.5VFSVA $I_{3\rightarrow4} = 0.1A$ 0.81.1VFSVB $I_{3\rightarrow4} = 1A$ 0.81.1VFVID Leakage Current Pin 3170 μA SUPER SANDCASTLE OUTPUT (Pin 19)Output Voltages (R load = 2.2kΩ)SANDT2Frame blanking pulse level22.53VSANDL2Line blanking pulse level44.55VBG2Burst key pulse level89VPulses width and timingSC3Delay between middle of sync pulse and leading edge of burst key pulse2.32.73.1 μs SC2Duration of burst key pulse vidth3.745 μs LINE FLYBACK INPUT (Pin 18)Switching level2VMaximum imput current at $V_{PEAK} = 800V$ 8mALimiting voltage at maximum current4.3V	FLYBACK (GENERATOR (Pin 3 and Pin 4)				
F2DB $I_{4\rightarrow3}$ = 1A3.04.5VFlyback Transistor on (output = high state), V _{CC2} = 30V V3/4 withFSVA $I_{3\rightarrow4}$ = 0.1A0.81.1VFSVB $I_{3\rightarrow4}$ = 1A2.24.5VFlyback Transistor off (output = V9 - 8V), V9 - V _{CC2} = 30VFCILeakage Current Pin 3170 μ ASUPER SANDCASTLE OUTPUT (Pin 19)Output Voltages (R load = 2.2kΩ)SANDT2Frame blanking pulse level22.53VSANDL2Line blanking pulse level44.55VBG2Burst key pulse level89VPulses width and timingSC3Delay between middle of sync pulse and leading edge of burst key pulse2.32.73.1 μ sSC2Duration of burst key pulse vidth3.745 μ sLINE FLYBACK INPUT (Pin 18)2VSwitching level2VMaximum imput current at V _{PEAK} = 800V8mALimiting voltage at maximum current4.3V		Flyback Transistor on (output = high state), V _{CC2} = 30V V4/3 with				
Flyback Transistor on (output = high state), $V_{CC2} = 30V V3/4$ with FSVA $I_{3\rightarrow 4} = 0.1A$ 0.8 1.1 V FSVB $I_{3\rightarrow 4} = 1A$ 2.2 4.5 V Flyback Transistor off (output = V9 - 8V), V9 - $V_{CC2} = 30V$ FCI Leakage Current Pin 3 170 μA SUPER SANDCASTLE OUTPUT (Pin 19) Output Voltages (R load = 2.2kΩ) SANDT2 Frame blanking pulse level 2 2.5 3 V SANDL2 Line blanking pulse level 4 4.5 5 V BG2 Burst key pulse level 8 9 V Pulses width and timing SC3 Delay between middle of sync pulse and leading edge of burst key pulse 2.3 2.7 3.1 μs SC2 Duration of burst key pulse Vertical blanking pulse width 18 V LINE FLYBACK INPUT (Pin 18) Switching level 2 V Maximum imput current at $V_{PEAK} = 800V$ 8 mA Limiting voltage at maximum current 4 4.3 V	F2DA	$I_4 \rightarrow_3 = 0.1A$		1.5	2.1	V
FSVA $I_{3\rightarrow4}=0.1A$ 0.81.1VFSVB $I_{3\rightarrow4}=1A$ 2.24.5VFIJBOACK Transistor off (output = V9 - 8V), V9 - V _{CC2} = 30VFCILeakage Current Pin 3170μASUPER SANDCASTLE OUTPUT (Pin 19)Output Voltages (R load = 2.2kΩ)SANDT2Frame blanking pulse level22.53VSANDL2Line blanking pulse level44.55VBG2Burst key pulse level89VPulses width and timingSC3Delay between middle of sync pulse and leading edge of burst key pulse2.32.73.1μsSC2Duration of burst key pulse Vertical blanking pulse width3.74 Note 15 Note 1μsLINE FLYBACK INPUT (Pin 18)2VSwitching level2VMaximum imput current at V _{PEAK} = 800V8mA Limiting voltage at maximum current4.3V	F2DB	$I_{4\rightarrow3}=1A$		3.0	4.5	V
FSVB $I_{3\rightarrow4}=1A$ 2.24.5VFlyback Transistor off (output = V9 - 8V), V9 - V _{CC2} = 30VFCILeakage Current Pin 3170μASUPER SANDCASTLE OUTPUT (Pin 19)Output Voltages (R load = $2.2k\Omega$)SANDT2Frame blanking pulse level22.53VSANDL2Line blanking pulse level44.55VBG2Burst key pulse level89VPulses width and timingSC3Delay between middle of sync pulse and leading edge of burst key pulse2.32.73.1μsSC2Duration of burst key pulse Vertical blanking pulse width3.74 Note 15 Note 1μsLINE FLYBACK INPUT (Pin 18)2VSwitching level2VMaximum imput current at V _{PEAK} = 800V8mALimiting voltage at maximum current4.3V		Flyback Transistor on (output = high state), V _{CC2} = 30V V3/4 with	·	•	•	
Flyback Transistor off (output = V9 - 8V), V9 - V _{CC2} = 30V FCI Leakage Current Pin 3	FSVA	$I_{3\rightarrow4}=0.1A$		0.8	1.1	V
FCILeakage Current Pin 3170μASUPER SANDCASTLE OUTPUT (Pin 19)Output Voltages (R load = $2.2k\Omega$)SANDT2Frame blanking pulse level2 2.5 3VSANDL2Line blanking pulse level4 4.5 5VBG2Burst key pulse level89VPulses width and timingSC3Delay between middle of sync pulse and leading edge of burst key pulse 2.3 2.7 3.1 μ sSC2Duration of burst key pulse Vertical blanking pulse width 3.7 4 Note 1 5 y substituting level 2 Maximum imput current at $V_{PEAK} = 800V$ 2 y mA Limiting voltage at maximum current 4.3 V	FSVB	$I_{3\rightarrow 4}=1A$		2.2	4.5	V
SUPER SANDCASTLE OUTPUT (Pin 19) Output Voltages (R load = $2.2k\Omega$) SANDT2 Frame blanking pulse level 2 2.5 3 V SANDL2 Line blanking pulse level 4 4.5 5 V BG2 Burst key pulse level 8 9 V Pulses width and timing SC3 Delay between middle of sync pulse and leading edge of burst key pulse 2.3 2.7 3.1 μ s SC2 Duration of burst key pulse Vertical blanking pulse width 1 Note 1 V LINE FLYBACK INPUT (Pin 18) Switching level 2 V Maximum imput current at $V_{PEAK} = 800V$ 8 mA Limiting voltage at maximum current 4 4.3 V		Flyback Transistor off (output = V9 - 8V), V9 - V _{CC2} = 30V				
Output Voltages (R load = 2.2kΩ) SANDT2 Frame blanking pulse level 2 2.5 3 V SANDL2 Line blanking pulse level 4 4.5 5 V BG2 Burst key pulse level 8 9 V Pulses width and timing SC3 Delay between middle of sync pulse and leading edge of burst key pulse 2.3 2.7 3.1 μs SC2 Duration of burst key pulse Vertical blanking pulse width 3.7 4 5 μs LINE FLYBACK INPUT (Pin 18) Switching level 2 V Maximum imput current at V _{PEAK} = 800V 8 mA Limiting voltage at maximum current 4.3 V	FCI	Leakage Current Pin 3			170	μΑ
SANDT2 Frame blanking pulse level SANDL2 Line blanking pulse level BG2 Burst key pulse level Pulses width and timing SC3 Delay between middle of sync pulse and leading edge of burst key pulse Vertical blanking pulse width LINE FLYBACK INPUT (Pin 18) Switching level Maximum imput current at V _{PEAK} = 800V Limiting voltage at maximum current 2 2.5 3 V 4.5 V 8 9 V Vertical blanking pulse and leading edge of burst key pulse 2.3 2.7 3.1 μs 8 μs Vertical blanking pulse width Auximum imput current at V _{PEAK} = 800V Maximum imput current at V _{PEAK} = 800V Vertical blanking voltage at maximum current Auximum imput current	SUPER SA	NDCASTLE OUTPUT (Pin 19)				
SANDL2 Line blanking pulse level 4 4.5 5 V BG2 Burst key pulse level 8 9 V Pulses width and timing SC3 Delay between middle of sync pulse and leading edge of burst key pulse 2.3 2.7 3.1 μs SC2 Duration of burst key pulse Vertical blanking pulse width 3.7 4 5 μs LINE FLYBACK INPUT (Pin 18) Switching level 2 V Maximum imput current at V _{PEAK} = 800V Limiting voltage at maximum current 4.3 V		Output Voltages (R load = 2.2kΩ)				
BG2 Burst key pulse level Pulses width and timing SC3 Delay between middle of sync pulse and leading edge of burst key pulse Vertical blanking pulse width LINE FLYBACK INPUT (Pin 18) Switching level Maximum imput current at V _{PEAK} = 800V Limiting voltage at maximum current 8 9 V Vertical blanking sync pulse and leading edge of burst key pulse 2.3 2.7 3.1 μs 5 μs Note 1 V Maximum imput current at V _{PEAK} = 800V At 1 1 2 1 1 1 2 1 1 2 1 1 2 1 1 2 1 1 2 1 1 2 1 1 2 1 1 2 1 1 2 1 1 2 1 1 2	SANDT2	Frame blanking pulse level	2	2.5	3	V
Pulses width and timing SC3 Delay between middle of sync pulse and leading edge of burst key pulse 2.3 2.7 3.1 μs SC2 Duration of burst key pulse Vertical blanking pulse width 3.7 4 5 μs LINE FLYBACK INPUT (Pin 18) Switching level 2 V Maximum imput current at V _{PEAK} = 800V 8 mA Limiting voltage at maximum current 4.3 V	SANDL2	Line blanking pulse level	4	4.5	5	V
SC3 Delay between middle of sync pulse and leading edge of burst key pulse SC2 Duration of burst key pulse Vertical blanking pulse width SWitching level Maximum imput current at V _{PEAK} = 800V Limiting voltage at maximum current SC3 2.7 3.1 μs A 5 μs V Σ ν ν ν ν ν ν ν ν ν ν ν ν ν ν ν ν ν ν	BG2	Burst key pulse level	8	9		V
SC2 Duration of burst key pulse Vertical blanking pulse width 3.7 4 Note 1 5 μs LINE FLYBACK INPUT (Pin 18) Switching level 2 V Maximum imput current at V _{PEAK} = 800V 8 mA Limiting voltage at maximum current 4.3 V		Pulses width and timing	·		•	
Vertical blanking pulse width Note 1 LINE FLYBACK INPUT (Pin 18) 2 V Switching level 2 V Maximum imput current at V _{PEAK} = 800V 8 mA Limiting voltage at maximum current 4.3 V	SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	μs
Switching level 2 V Maximum imput current at V _{PEAK} = 800V 8 mA Limiting voltage at maximum current 4.3 V	SC2	Duration of burst key pulse Vertical blanking pulse width	3.7	-	5	μs
Maximum imput current at V _{PEAK} = 800V 8 mA Limiting voltage at maximum current 4.3 V	LINE FLYB	ACK INPUT (Pin 18)				
Limiting voltage at maximum current 4.3 V		Switching level		2		V
		Maximum imput current at V _{PEAK} = 800V		8		mA
τ RC network time constant (Note 2) 6 μs		Limiting voltage at maximum current		4.3		V
	τ	RC network time constant (Note 2)		6		μs

Notes: 1. Width of vertical blanking pulse on SSC output is proportional to the frame flyback time, the switching level is V_{CC}2 - 2V_{BE} and the other input of the comparator is tied to the frame amplifier output. Application circuit uses the frame flyback generator.
 An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse.

GENERAL DESCRIPTION

The TDA8214B performs all the video and power functions required to provide signals for the line driver and frame yoke.

It contains:

- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line driver

- A line phase detector and a voltage control oscillator
- A super sandcastle generator
- Video identification output.

The slice level of sync-separation is fixed by value of the external resistors R1 and R2. V_R is an internally fixed voltage.

The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

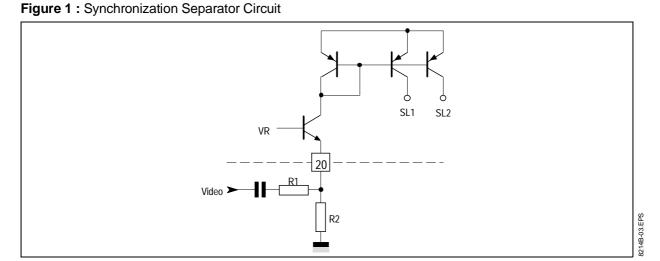


Figure 2: Frame Separator

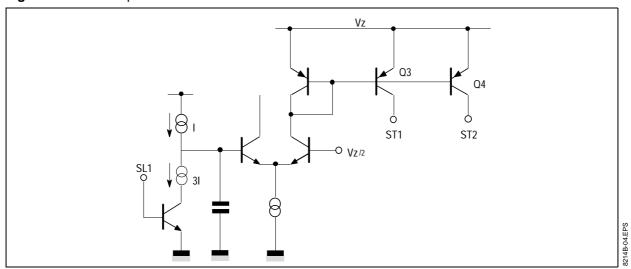
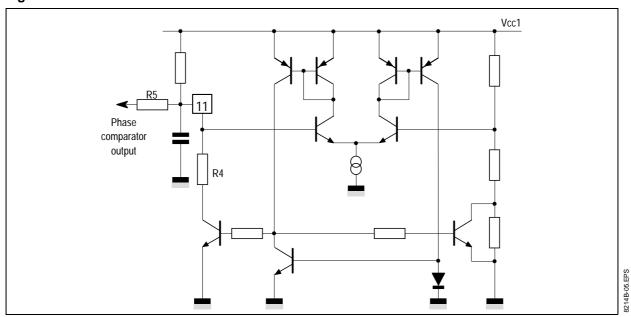
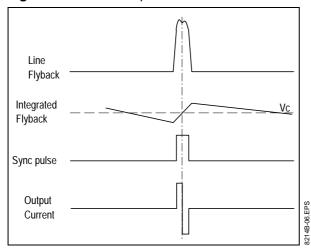


Figure 3: Line Oscillator



The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

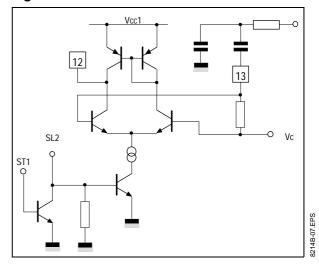
Figure 4: Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the

comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

Figure 5

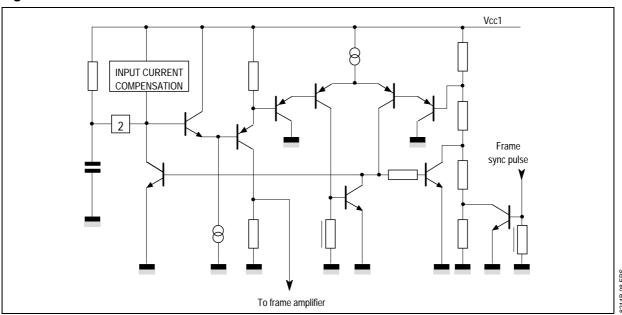


Line output (Pin 17)

It is an open-collector output. The output positive pulse time is $29\mu s$ for a $64\mu s$ period.

The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Figure 6: Frame Oscillator



Frame output amplifier

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

The frame blanking is detected by the frame fly-back generator. When the output voltage of the frame amplifier exceeds $V_{CC}2$ - $2V_{BE}$, the pulse is detected. The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (Pin 14). It is referenced to the middle of the line

flyback.

This stage will detect the coincidence between the line sync pulse (if present) and a $2\mu s$ sampling pulse. This $2\mu s$ pulse is positionned at the center of line sync pulse when the phase loop is locked. This sampled detection is stored by an external capacitor Pin 8.

The identification output level is high when video signal is present.

Important remark: minimum saw-tooth amplitude on Pin 13 has to be 2VPP (typ.: 2.5VPP).

Figure 7: Super Sandcastle Generator

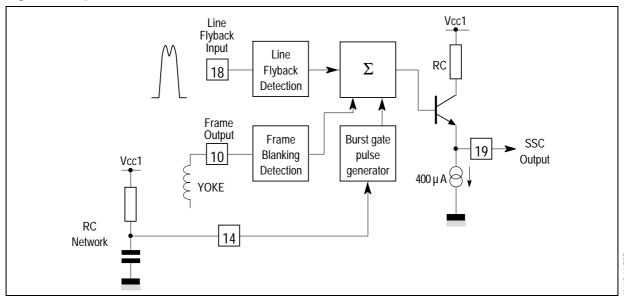
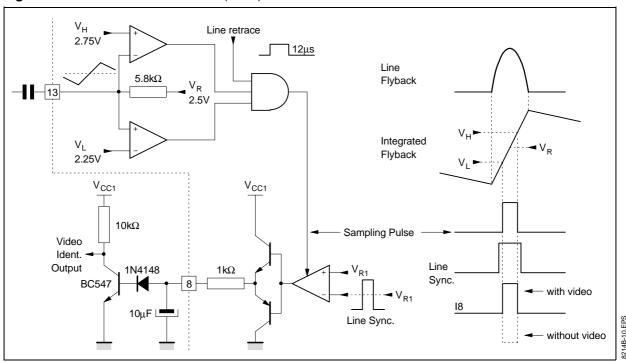
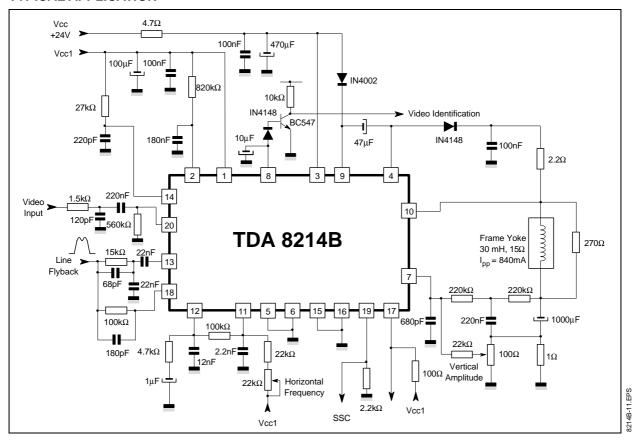


Figure 8: Video Identification Circuit (Pin 8)

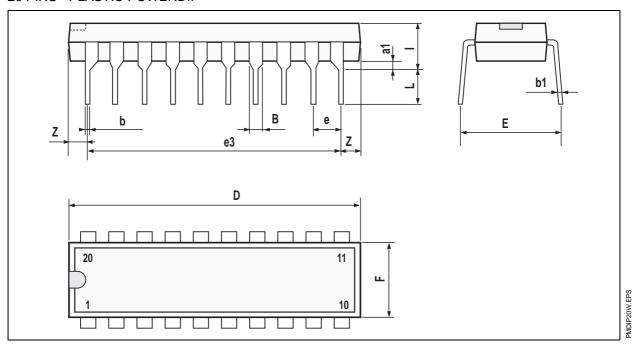


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC POWERDIP



Dimensions		Millimeters			Inches	
Difficusions	Min.	Тур.	Max.	Min.	Тур.	Max.
a1	0.51			0.020		
В	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
Е		8.8			0.346	
е		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

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