I²C-bus interface for colour decoders TDA8442

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38); SOT38-1; 1996 July 23.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX	UNIT
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

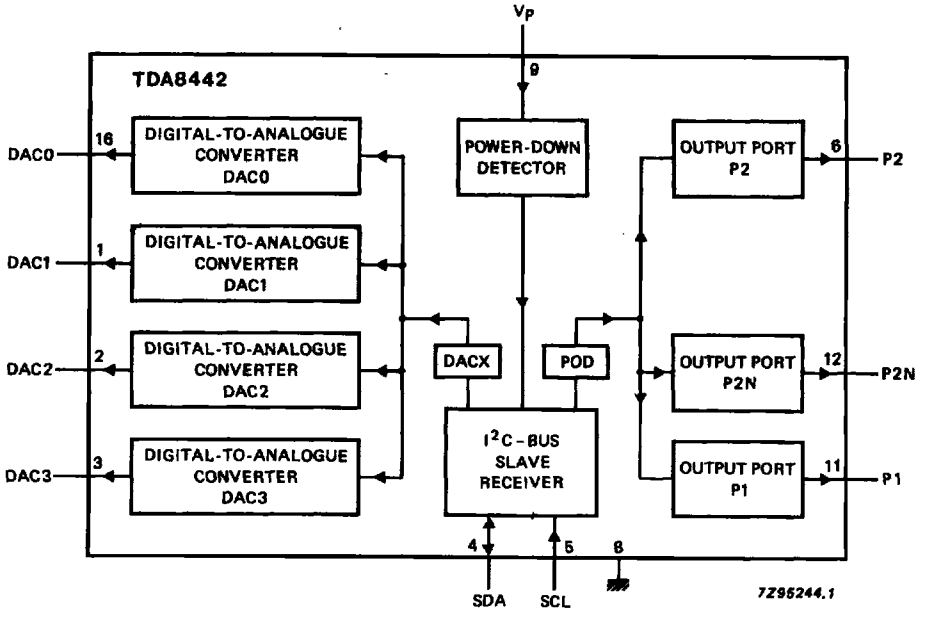


Fig.1 Block diagram.

PINNING

PIN	SYMBOL	DESCRIPTION
1	DAC1	analogue output 1
2	DAC2	analogue output 2
3	DAC3	analogue output 3
4	SDA	serial data line; I²C-bus
5	SCL	serial clock line; I²C-bus
6	P2	Port 2 npn collector output with internal pull-up resistor
7	n.c.	not connected
8	GND	supply return (ground)
9	V_P	positive supply voltage
10	n.c.	not connected
11	P1	Port 1 open npn emitter output
12	P2N	inverted P2 output
13	n.c.	not connected
14	n.c.	not connected
15	n.c.	not connected
16	DAC0	analogue output 0

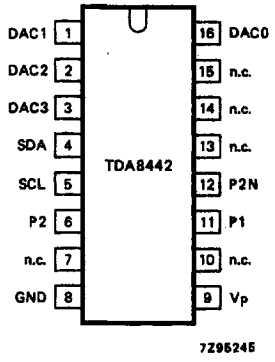


Fig.2 Pinning diagram

FUNCTIONAL DESCRIPTION

Control

Analogue control is facilitated by four 6-bit digital-to-analogue converters (DAC0 to DAC3).
The values of the output voltages from the DACs are set via the I²C-bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals.
It is an open npn emitter output capable of sourcing 14 mA (min.).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are npn collector outputs with internal pull-up resistors of 10 kΩ (typ.). Both outputs are capable of sinking up to 2 mA with a voltage drop of less than 400 mV. If one output is switched on (LOW), the other output is switched off, and vice versa.

Reset

The power-down-reset mode occurs whenever the positive supply voltage falls below 8.5 V (typ.) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C-bus (specifications for the I²C-bus will be supplied on request). Programming of the TDA8442 is performed using the format shown in Fig.3.

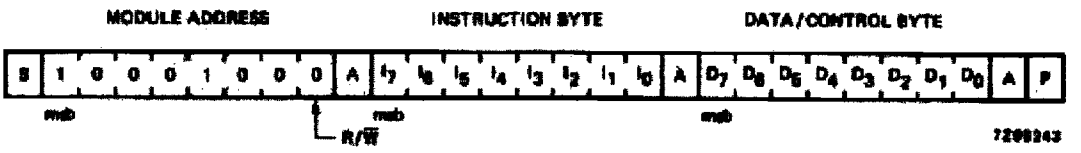


Fig.3 TDA8442 programming format.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down-reset mode (V_P > 8.5 V (typ.)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) together with the corresponding data/control bytes (see Fig.4).

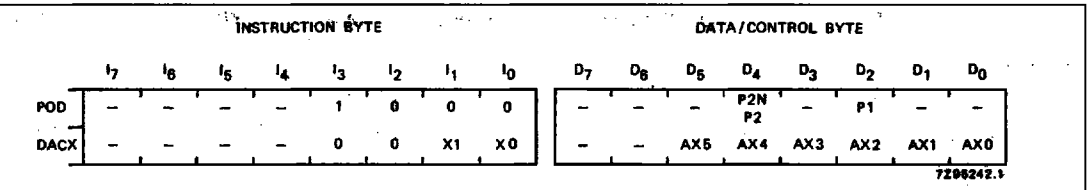


Fig.4 Control porgramming.

POD bit P1

If a logic 1 is programmed, the P1 output is switched on. If a logic 0 is programmed or after a power-down-reset, the P1 output is switched off (high-impedance state).

POD bit P2/P2N

If a logic 1 is programmed, the P2 output is switched off and the P2N output is switched on (LOW). If a logic 0 is programmed or after a power-down-reset, the P2 output is switched on (LOW) and the P2N output is switched off.

DAX bits AX5 to AX0

The digital-to-analogue converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using bits AX5 to AX0, the lowest value being with all data AX5 to AX0 at logic 0 or when power-down-reset has been activated.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage range (pin 9)	V_P	−0.3	+13.2	V
Input/output voltage ranges				
pin 4	V_{SDA}	−0.3	+13.2	V
pin 5	V_{SCL}	−0.3	+13.2	V
pin 6	V_{P2}	−0.3	V_P; note 1	V
pin 11	V_{P1}	−0.3	V_P; note 1	V
pin 12	V_{P2N}	−0.3	V_P; note 1	V
pin 1 to 3 and pin 16	V_{DAX}	−0.3	V_P; note 1	V
Total power dissipation	P_{tot}	–	1	W
Operating ambient temperature range	T_{amb}	−20	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

Note

1. Pin voltage may exceed V_P if the current in that pin is limited to 10 mA.

CHARACTERISTICS

V_P = 12 V; T_{amb} = +25 °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supplies						
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current (pin 9)	no outputs loaded	I_P	8	13	18	mA
I²C-bus inputs						
SDA (pin 4); SCL (pin 5)						
Input voltage HIGH	note 1	V_{IH}	3.0	–	V_P − 1	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input current HIGH	note 1	I_{IH}	–	–	10	μA
Input current LOW	note 1	I_{IL}	–	–	10	μA
I²C-bus output						
SDA (pin 4)	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	3	5	–	mA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Ports P2 and P2N						
(pins 6 and 12)	npn collector output with pull-up resistor to V_P					
Internal pull-up resistor to V_P		R_O	5	10	15	kΩ
Output voltage switched on (LOW)	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current		I_{OL}	2	5	–	mA
Leakage current output switched off		$-I_{leak}$	–	–	25	µA
Port P1 (pin 11)	open npn emitter output					
Output current switched on	V_O = 0 to 5 V	I_O	14	–	–	mA
Leakage current switched off	V_O = 0 to V_P	$\pm I_{leak}$	–	–	100	µA
Digital-to-analogue outputs	note 2					
DAC0 (pin 16)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	3.0	–	4.25	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.15	–	1.0	V
Positive value of smalles step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	16	–	72	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	45	mV
Output impedance	I_O = –2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC1 (pin 1)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = –2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DAC2 (pin 2)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	4.0	–	5.0	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	1.0	–	1.7	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	18	–	86	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	50	mV
Output impedance	I_O = −2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
DAC3 (pin 3)						
Maximum output voltage	unloaded; note 3	$V_{O\,max}$	10.0	–	11.2	V
Minimum output voltage	unloaded; note 3	$V_{O\,min}$	0.1	–	1.0	V
Positive value of smallest step	I_O = 2 mA (1 lsb); note 3	$V_{O\,lsb}$	70	–	250	mV
Deviation from linearity	I_O = 2 mA	ΔV	–	–	150	mV
Output impedance	I_O = −2 to +2 mA	Z_O	–	–	30	Ω
Maximum output source current		$-I_{OH}$	2	–	6	mA
Maximum output sink current		I_{OL}	2	8	–	mA
Power-down reset						
Maximum value of V_P at which power-down reset is active		V_{PD}	6	–	10	V
Rise time of V_P during power-on	V_P rising from 0 V to V_{PD}	t_r	5	–	–	µs

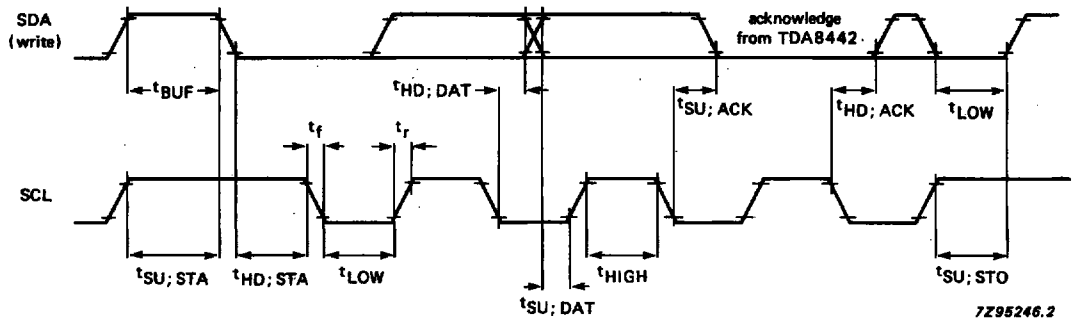
Notes to the Characteristics

1. If V_P < 1 V, the input current is limited to 10 µA at input voltages up to 13.2 V.
2. Pure capacitive load should be avoided because of possible oscillations.
3. Values are proportional to V_P.

I²C-BUS TIMING

Bus loading conditions: 4kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.
All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Bus free before start	t_{BUF}	4.0	–	–	µs
Start condition set-up time	$t_{SU;\,STA}$	4.0	–	–	µs
Start condition hold time	$t_{HD;\,STA}$	4.0	–	–	µs
LOW period SCL, SDA	t_{LOW}	4.0	–	–	µs
HIGH period SCL	t_{HIGH}	4.0	–	–	µs
Rise time SCL, SDA	t_r	–	–	1.0	µs
Fall time SCL, SDA	t_f	–	–	0.30	µs
Data set-up time (write)	$t_{SU;\,DAT}$	1	–	–	µs
Data hold time (write)	$t_{HD;\,DAT}$	1	–	–	µs
Acknowledge (from TDA8442) set-up time	$t_{SU;\,ACK}$	–	–	3.5	µs
Acknowledge (from TDA8442) hold time	$t_{HD;\,ACK}$	0	–	–	µs
Stop condition set-up time	$t_{SU;\,STO}$	4.0	–	–	µs



Reference levels are 10 and 90%.

Fig.5 I²C-bus timing; TDA8442.