



## 7.5 NS TRIPLE-CHANNEL HIGH VOLTAGE VIDEO AMPLIFIER

### FEATURES

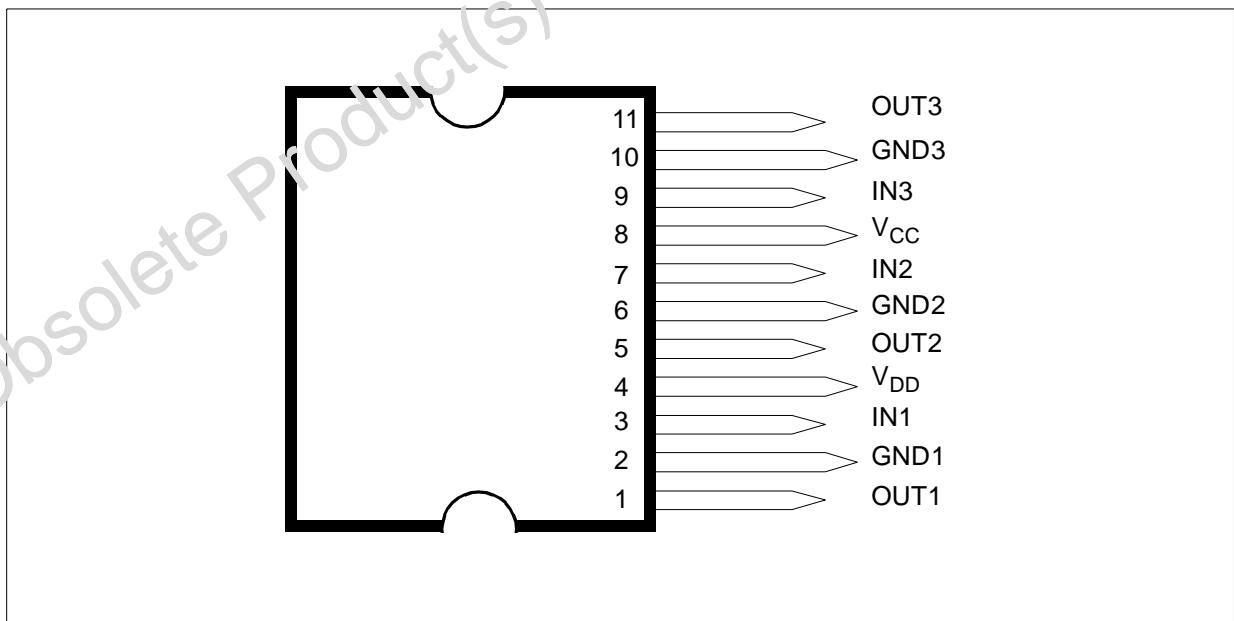
- Triple-Channel Video Amplifier
- Supports DC Coupling (optimum cost saving) and AC Coupling Applications.
- Built-in Voltage Gain: 19.3 (Typ.)
- Rise and Fall Times: 7.5ns (Typ.)
- Bandwidth: 50MHz (Typ.)
- 80V Output Dynamic Range
- Supply Voltage: 110V
- Perfectly matched with the TDA9210 Preamplifier
- Full Pin Compatibility with the TDA9535

### DESCRIPTION

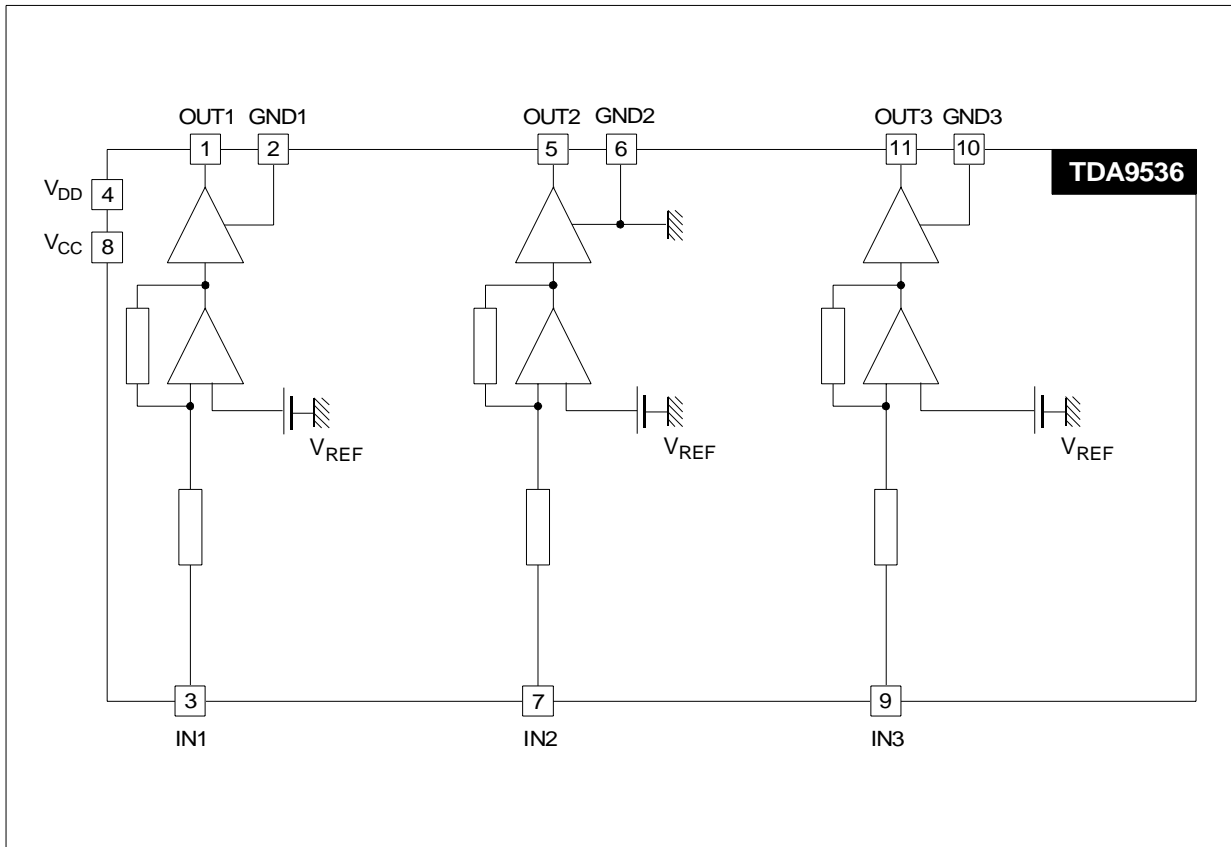
The TDA9536 is a triple-channel video amplifier designed in BCD technology (Bipolar/CMOS/DMOS) able to drive the 3 cathodes of a CRT monitor.

Perfectly matched with the ST Preamplifier TDA9210, it provides a high performance, and very cost effective DC coupling system.

### PIN CONNECTIONS



1 BLOCK DIAGRAM



2 PIN CONNECTIONS

Pin	Name	Function
1	OUT1	Output-Channel 1
2	GND1	Power Ground-Channel 1
3	IN1	Video Input-Channel 1
4	V <sub>DD</sub>	Amplifier High Supply Voltage
5	OUT2	Output-Channel 2
6	GND2	Power Ground-Channel 2/ Ground Substract
7	IN2	Video Input-Channel 2
8	V <sub>CC</sub>	Low Supply Voltage
9	IN3	Video Input-Channel 3
10	GND3	Power Ground-Channel 3
11	OUT3	Output-Channel 3

### 3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	High supply voltage	120	V
$V_{CC}$	Low supply voltage	17	V
$V_{ESD}$	ESD susceptibility Human Body Model (100pF discharged through 1.5K $\Omega$ ) EIAJ norm (200pF discharged through 0 $\Omega$ )	2 300	kV V
$I_{OD}$	Output source current (pulsed < 50 $\mu$ s)	80	mA
$I_{OG}$	Output sink current (pulsed < 50 $\mu$ s)	80	mA
$V_{IN Max}$	Maximum Input Voltage	15	V
$V_{IN Min}$	Minimum Input Voltage	- 0.5	V
$T_J$	Junction Temperature	150	$^{\circ}$ C
$T_{STG}$	Storage Temperature	-20 + 150	$^{\circ}$ C

### 4 THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction-Case Thermal Resistance (Max.)	3	$^{\circ}$ C/W
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance (Typ.)	35	$^{\circ}$ C/W

## 5 ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
<b>SUPPLY parameters (<math>V_{CC} = 12V</math>, <math>V_{DD} = 110V</math>, <math>T_{amb} = 25\text{ }^{\circ}C</math>, unless otherwise specified)</b>						
$V_{DD}$	High supply voltage (Pin 5)		20	110	115	V
$V_{CC}$	Low supply voltage (Pin 11)		10	12	15	V
$I_{DD}$	$V_{DD}$ supply current	$V_{OUT} = 50V$		25		mA
$I_{DDS}$	$V_{DD}$ stand-by supply current	$V_{CC}$ : switched off (<1.5V) $V_{OUT}$ : high (Note 1)		12		mA
$I_{CC}$	$V_{CC}$ supply current	$V_{OUT} = 50V$		60		mA
<b>STATIC parameters (<math>V_{CC} = 12V</math>, <math>V_{DD} = 110V</math>, <math>T_{amb} = 25\text{ }^{\circ}C</math>)</b>						
$dV_{OUT}/dV_{DD}$	High Voltage supply rejection	$V_{OUT} = 50V$		0.5		%
$dV_{OUT}/dT$	Output Voltage drift versus temperature	$V_{OUT} = 80V$		15		mV/ $^{\circ}C$
$d\Delta V_{OUT}/dT$	Output voltage matching versus temperature (Note 2)	$V_{OUT} = 80V$		5		mV/ $^{\circ}C$
$R_{IN}$	Video Input Resistor	$V_{OUT} = 50V$		2		k $\Omega$
$V_{SATH}$	Output Saturation Voltage to Supply	$I_0 = -60mA$ (Note 3)		$V_{DD} - 6.5$		V
$V_{SATL}$	Output Saturation Voltage to GND	$I_0 = 60mA$ (Note 3)		11		V
VG	Video Gain	$V_{OUT} = 50V$		19.3		
LE	Linearity Error	$17 < V_{OUT} < V_{DD} - 15V$		5	8	%
$V_{REF}$	Internal Voltage Reference			5.5		V

**Note 1:** The TDA 9536 goes into stand-by mode when  $V_{CC}$  is switched off (<1.5V).  
In stand-by mode,  $V_{out}$  is set to high level.

**Note 2:** Matching measured between each channel.

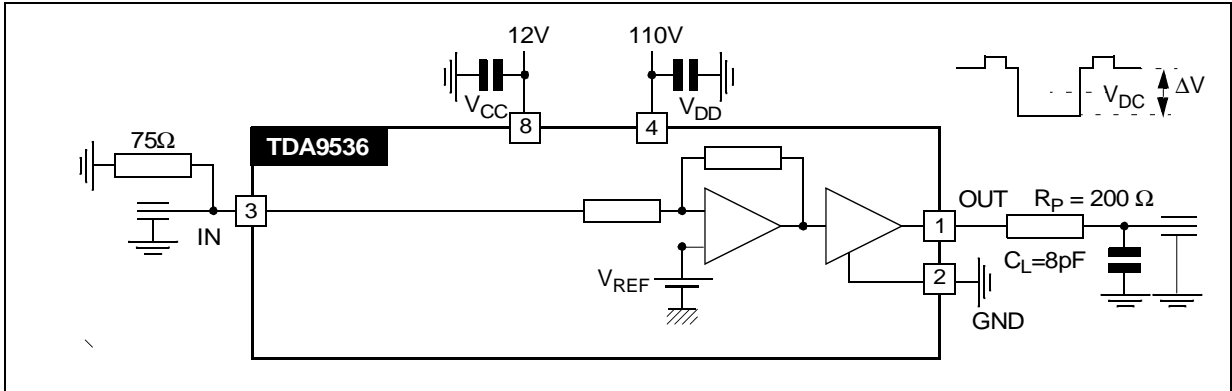
**Note 3:** Pulsed current width < 50 $\mu$ s

**ELECTRICAL CHARACTERISTICS (continued)**

Symbol	Parameter	Test Conditions	Min.	Typ	Max	Unit
<b>DYNAMIC parameters (see Figure 1)</b>						
OS1	Overshoot, White to Black transition			5		%
OS2	Overshoot, Black to White transition			1		%
$\Delta VG$	Low frequency gain matching (Note 4)	$V_{DC} = 50V, f=1MHz$			5	%
BW	Bandwidth at -3dB	$V_{DC}=50V, \Delta V=20V_{PP}$		50		MHz
$t_R$	Rise time	$V_{DC}=50V, \Delta V=40V_{PP}$		7.2		ns
$t_F$	Fall time	$V_{DC}=50V, \Delta V=40V_{PP}$		7.9		ns
$t_{SET}$	2.5% Settling time	$V_{DC}=50V, \Delta V=40V_{PP}$		15		ns
$CT_L$	Low frequency Crosstalk	$V_{DC}=50V, \Delta V=20V_{PP}$ $f = 1 MHz$		50		dB
$CT_H$	High frequency Crosstalk	$V_{DC}=50V, \Delta V=20V_{PP}$ $f = 20MHz$		32		dB

**Note 4:** Matching measured between each channel.

**Figure 1. AC test circuit**



## 6 THEORY OF OPERATION

### 6.1 - General

The TDA9536 is a three-channel video amplifier supplied by a low supply voltage:  $V_{CC}$  (typ.12V) and a high supply voltage:  $V_{DD}$  (up to 115V).

The high values of  $V_{DD}$  supplying the amplifier output stage allow direct control of the CRT cathodes (DC coupling mode).

In DC coupling mode, the application schematic is very simple and only a few external components are needed to drive the cathodes. In particular,

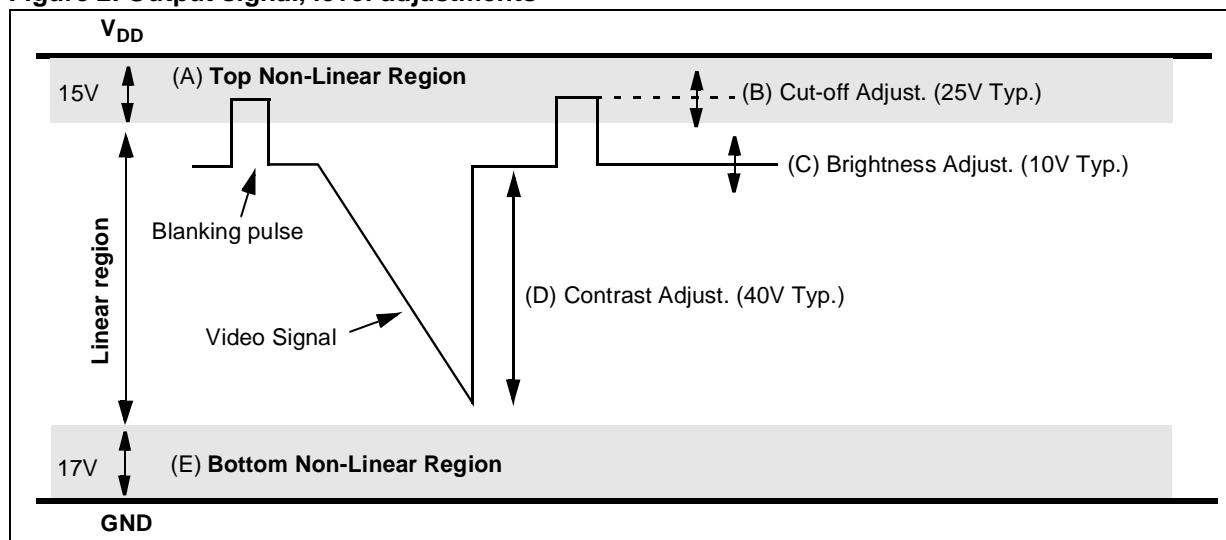
there is no need of the DC-restore circuitry which is used in classical AC coupling applications.

The output voltage range is wide enough (Figure 2) to provide simultaneously :

- Cut-off adjustment (typ. 25V)
- Video contrast (typ. up to 40V),
- Brightness (with the remaining voltage range).

In normal operation, the output video signal must remain inside the linear region whatever the cut-off / brightness / contrast adjustment is.

**Figure 2. Output signal, level adjustments**



### 6.2 - How to choose the high supply voltage value ( $V_{DD}$ )

The  $V_{DD}$  high supply voltage must be chosen carefully. It must be high enough to provide the necessary video adjustment but set to minimum value to avoid unnecessary power dissipation.

Example:

The following example shows how the optimum  $V_{DD}$  voltage value is determined:

- Cut-off adjustment range (B) : 25V
- Max contrast (D) : 40V

Case 1:

10V Brightness (C) adjusted by the preamplifier :

$$V_{DD} = A + B + C + D + E$$

$$V_{DD} = 15V + 25V + 10V + 40V + 17V = 107V$$

Case 2:

10V Brightness (C) adjusted by the G1 anode:

$$V_{DD} = A + B + D + E$$

$$V_{DD} = 15V + 25V + 40V + 17V = 97V$$

**6.3 - Amplifier gain and cut-off adjustment**

A very simplified schematic of each TDA9536 channel is shown in Figure 3.

The feedback net of each channel is integrated with a built-in voltage gain of 19.3 (40k/2k).

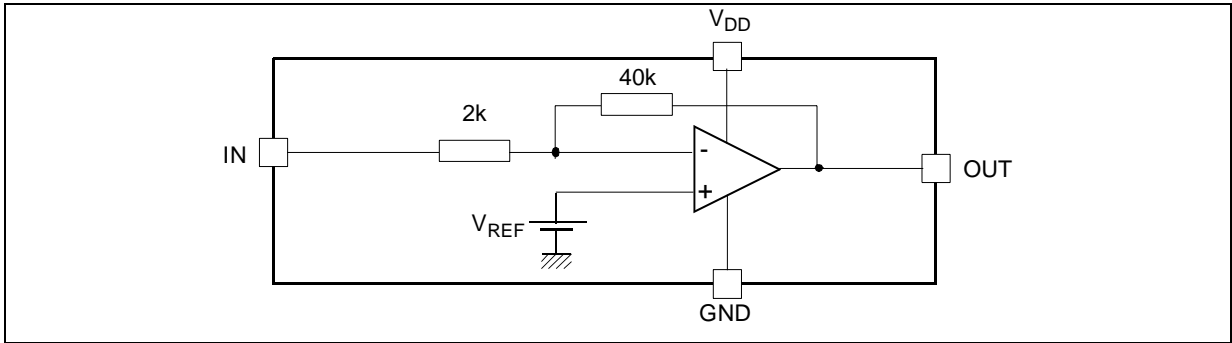
The output voltage  $V_{OUT}$  is given by the following formula:

$$V_{OUT} = (VG+1) \times V_{REF} - (VG \times V_{IN})$$

for  $VG = 19.3$  and  $V_{REF} = 5.5V$ , we have

$$V_{OUT} = 111.6 - 19.3 \times V_{IN}$$

**Figure 3. Simplified schematic of one channel**



**7 ARCING PROTECTION**

As the amplifier outputs are connected to the CRT cathodes, special attention must be given to protect them against possible arcing inside the CRT.

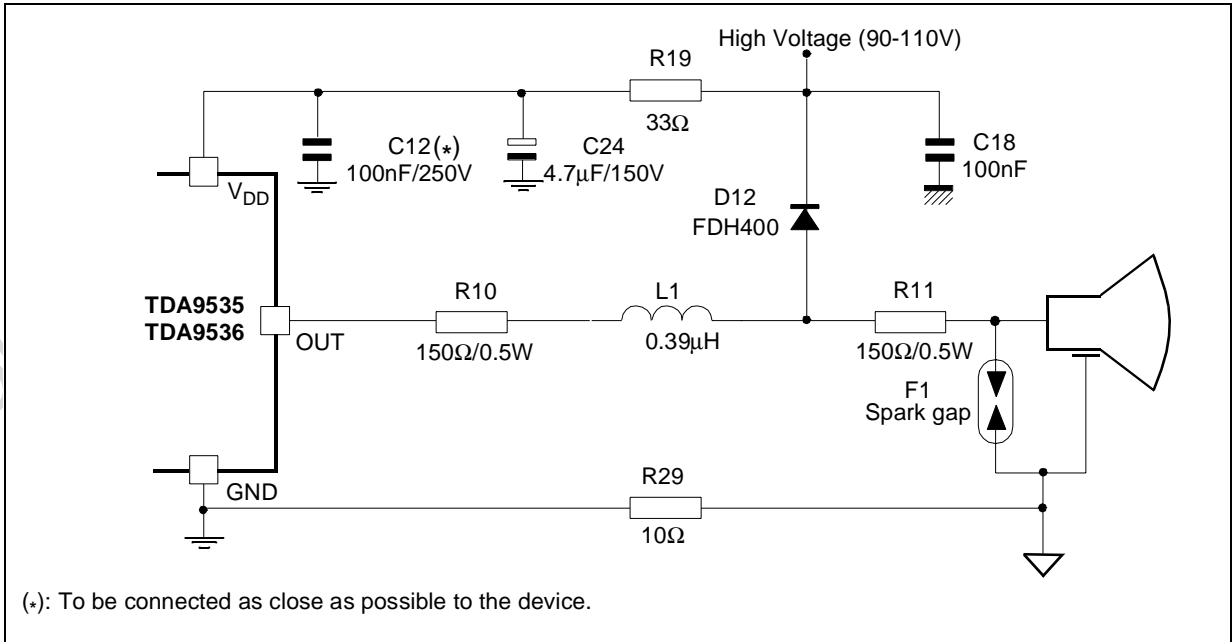
Protection must be considered when starting the design of the video CRT board. It should always be implemented before starting to adjust the dynamic video response of the system.

The arcing network that we recommend (see Figure 4) provides efficient protection without deteriorating the amplifier video performances.

The total resistance value between the amplifier and the CRT cathode ( $R10+R11$ ) should not be less than 300  $\Omega$ .

Spark gap diodes are strongly recommended for protection against arcing.

**Figure 4. Arcing protection network (one channel)**

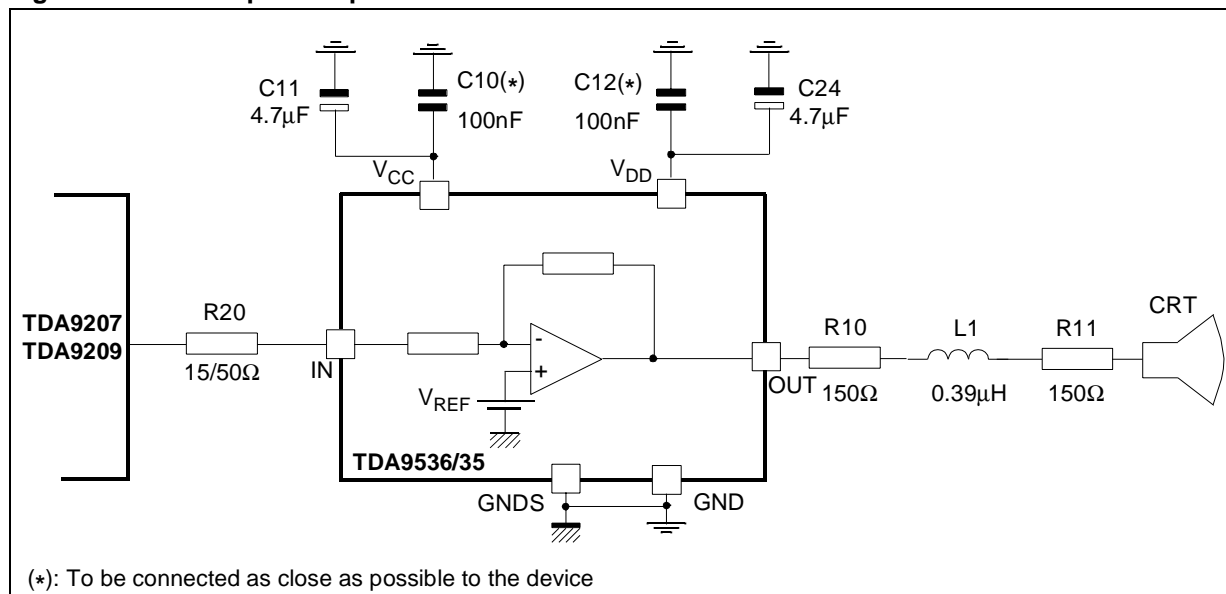


## 8 VIDEO RESPONSE OPTIMIZATION

The dynamic video response is optimized by carefully designing the supply decoupling of the video board (see Section 8.1), the tracks (see Section 8.2), then by adjusting the input/output component network (see Section 8.3).

For dynamic measurements such as rise/fall time and bandwidth, a 8pF load is used (total load including the parasitic capacitance of the PC board and CRT Socket).

Figure 5. Video response optimization for one channel



### 8.1 Supply decoupling

The decoupling of  $V_{CC}$  and  $V_{DD}$  through good quality HF capacitors (respectively C10 and C12) close to the device is necessary to improve the dynamic performance of the video signal.

### 8.2 - Tracks

Careful attention has to be given to the three output channels of the amplifier.

- Capacitor: The parasitic capacitive load on the amplifier outputs must be as small as possible. Figure 11 clearly shows the deterioration of the  $t_R/t_F$  when the capacitive load increases. Reducing this capacitive load is achieved moving away the output tracks from the other tracks (especially ground) and by using thin tracks (<0.5mm), see Figure 13.
- Cross talk: Output and input tracks must be set apart. We recommend to install input and output tracks on opposite sides of the amplifier. Once again, this is achievable by using thin tracks (<0.5 mm) to pass through the pin of the device, see Figure 13 (b).

- Length: Connection between amplifier output and cathode must be as short and direct as possible.

### 8.3 - Network adjustment

Video response is always a compromise between several parameters. An improvement of the rise/fall time leads to a deterioration of the overshoot.

The recommended way to optimize the video response is:

- 1 To set  $R_{10}+R_{11}$  for arcing protection (min. 300  $\Omega$ )
- 2 To adjust R20 and  $R_{10}+R_{11}$ . Increasing their value increases the  $t_R/t_F$  values and decrease the overshoot
- 3 To adjust L1  
Increasing L1 speeds up the device and increases the overshoot.

We recommend our customers to use the schematic shown on Figure 5 as a starting point for the video board and then to apply the optimization they need.



## 9 POWER DISSIPATION

The total power dissipation is the sum of the static DC and the dynamic dissipation:

$$P_{TOT} = P_{STAT} + P_{DYN}$$

The static DC power dissipation is approximately:

$$P_{STAT} = V_{DD} \times I_{DD} + V_{CC} \times I_{CC}$$

The dynamic dissipation is, in the worst case (1 pixel On/ 1 pixel Off pattern):

$$P_{DYN} = 3 V_{DD} \times C_L \times V_{OUT(PP)} \times f \times K$$

where f is the video frequency and K the ratio between the active line and the total horizontal line duration.

Example:

for  $V_{DD} = 110V$ ,  $V_{CC} = 12V$ ,

$I_{DD} = 25mA$ ,  $I_{CC} = 60mA$ ,

$V_{OUT} = 40 V_{PP}$ ,  $f = 40MHz$ ,

$C_L = 8pF$  and  $K = 0.72$ .

We have:

$$P_{STAT} = 3.47W, P_{DYN} = 3.04W$$

Therefore:

$$P_{TOT} = 6.51W.$$

**Note 4:**

This worst thermal case must only be considered for  $T_{Jmax}$  calculation.

Nevertheless, during the average life of the circuit, the conditions are closer to the white picture conditions.



### 10 TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD}=110V$ ,  $V_{CC}=12V$ ,  $C_L=8pF$ ,  $R_p=300\Omega$ ,  $\Delta V=40V_{PP}$ , unless otherwise specified - see Figure 1

Figure 6. TDA9536 pulse response

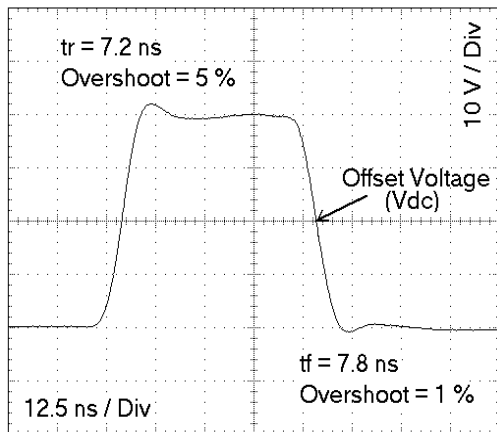


Figure 7.  $V_{OUT}$  versus  $V_{IN}$

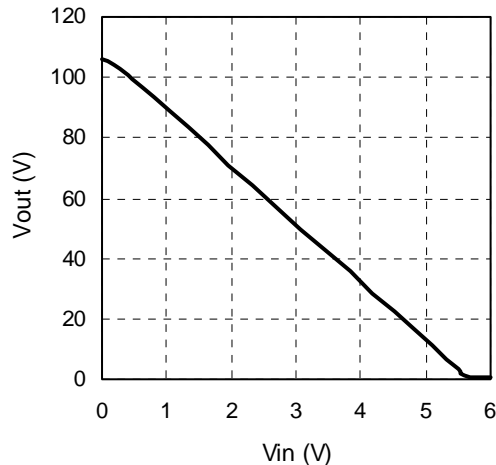


Figure 8. Power dissipation versus frequency

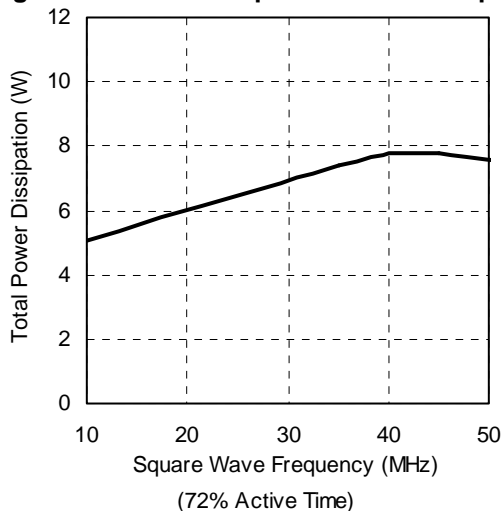


Figure 9. Speed versus temperature

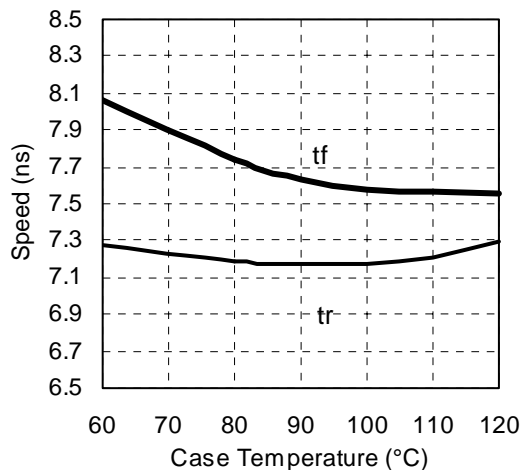


Figure 10. Speed versus offset

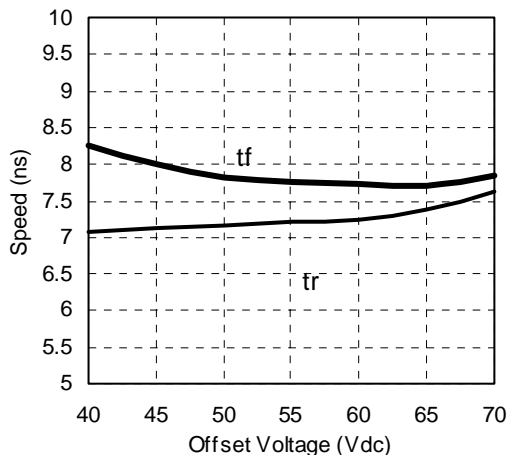


Figure 11. Speed versus load capacitance

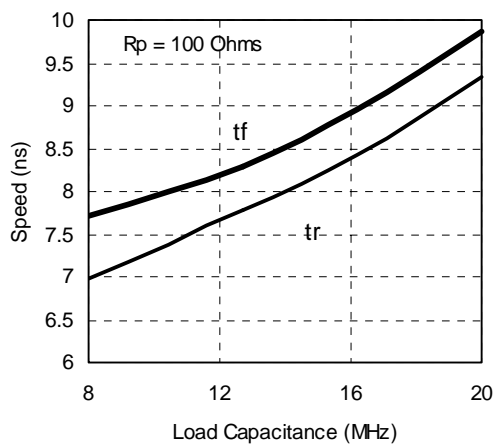


Figure 12. TDA9210 - TDA9535/9536 Demonstration Board: Silk Screen and Trace

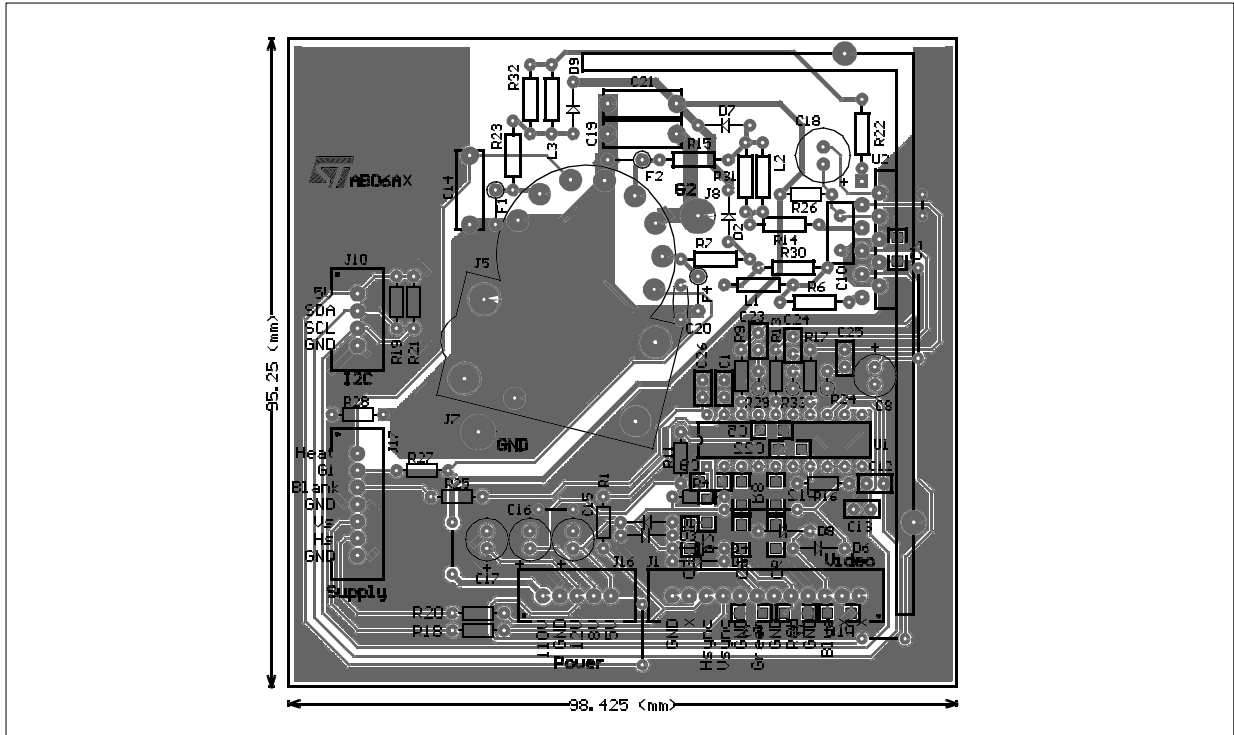
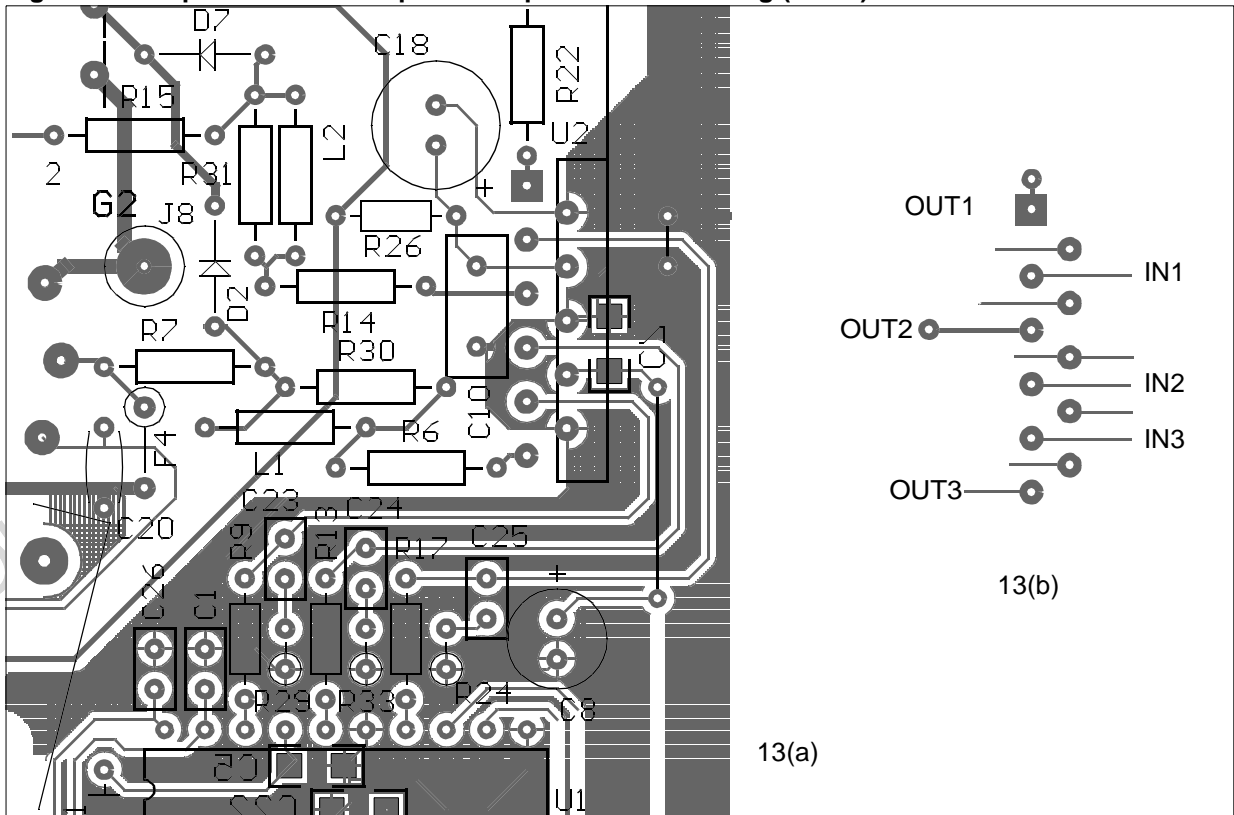
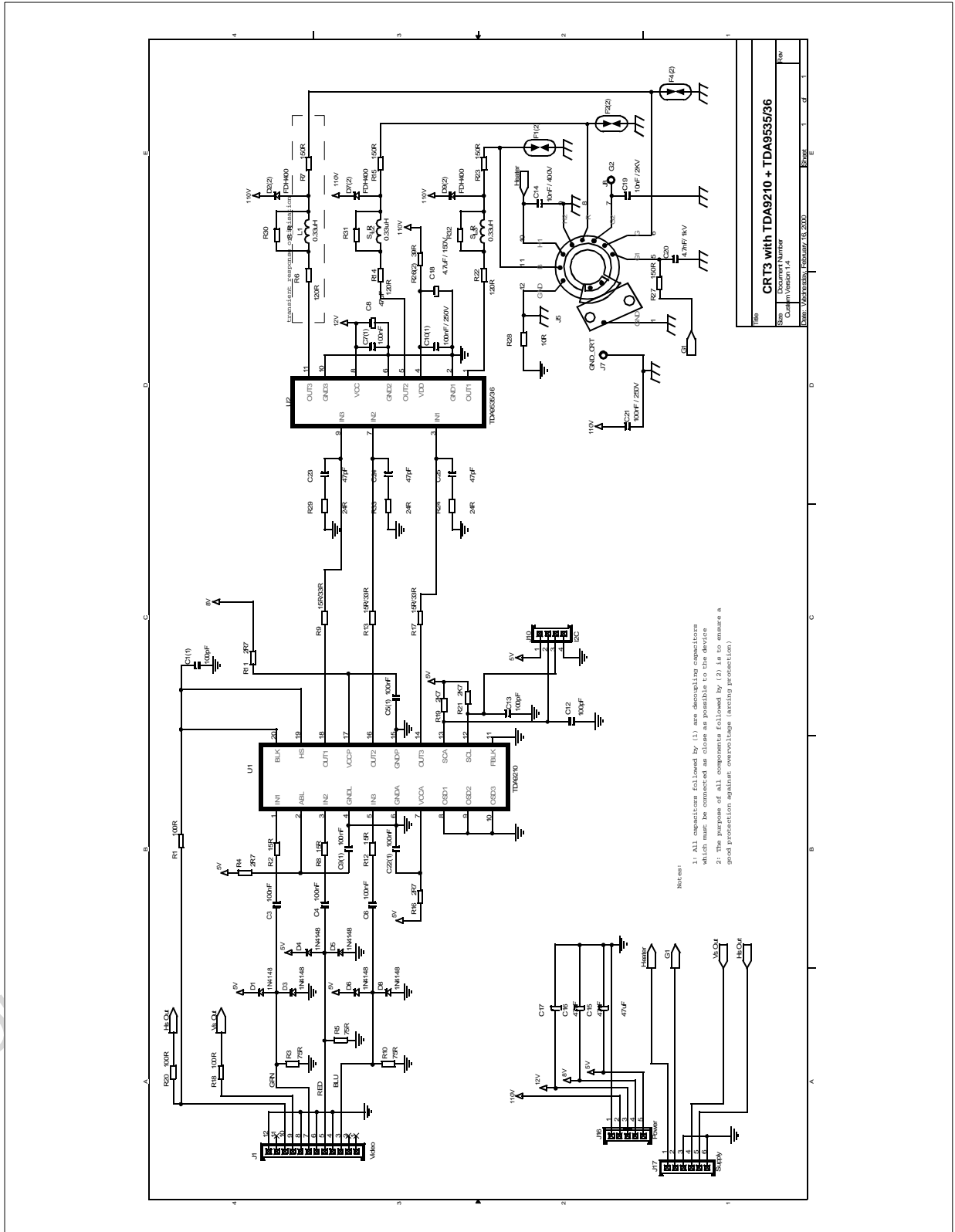


Figure 13. Amplifier and Pre-amplifier Outputs. Trace Routing (detail)



# TDA9536

## Figure 14. TDA9535/9536 - TDA9210 Demonstration Board Schematic



11 PACKAGE MECHANICAL DATA

11 PIN - CLIPWATT

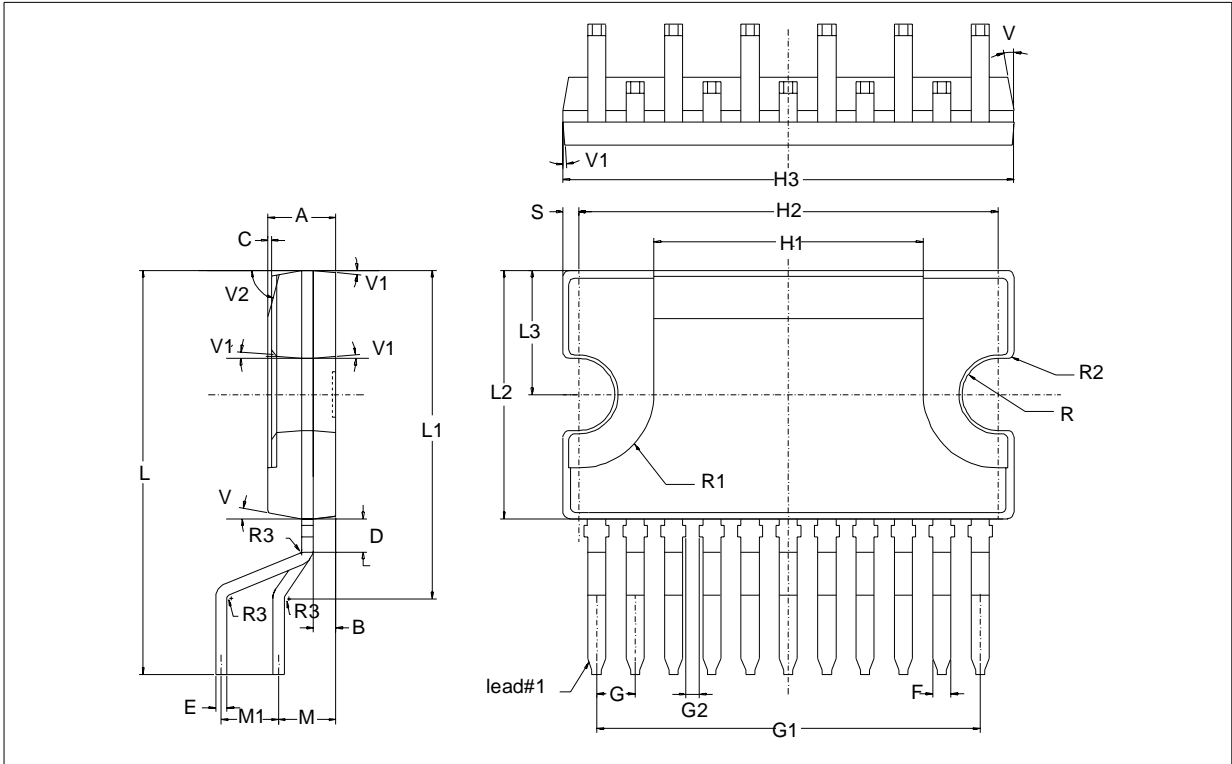


Table 1

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.95	3.00	3.05	0.116	0.118	0.120
B	0.95	1.00	1.05	0.037	0.039	0.041
C		0.15			0.006	
D	1.30	1.50	1.70	0.051	0.059	0.066
E	0.49	0.515	0.55	0.019	0.020	0.021
F	0.78	0.80	0.88	0.031	0.033	0.034
G	1.60	1.70	1.80	0.063	0.067	0.071
G1	16.90	17.00	17.10	0.665	0.669	0.673
H1		12.00			0.472	
H2	18.55	18.60	18.65	0.730	0.732	0.734
H3	19.90	20.00	20.10	0.783	0.787	0.791 (5)
L	17.70	17.90	18.10	0.696	0.704	0.712
L1	14.35	14.55	14.65	0.564	0.572	0.576
L2	10.90	11.00	11.10	0.429	0.433	0.437(5)
L3	5.40	5.50	5.60	0.212	0.216	0.220
M	2.34	2.54	2.74	0.092	0.100	0.107
M1	2.34	2.54	2.74	0.092	0.100	0.107
R	1.45			0.057		

## TDA9536

Table 1

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R1	3.20	3.30	3.40	0.126	0.130	0.134
R2		0.30			0.012	
R3		0.50			0.019	
S	0.65	0.70	0.75	0.025	0.027	0.029
V		10deg.			10deg.	
V1		5deg.			5deg.	
V2		75deg.			75deg.	

**Note 5:** "H3 and L2" do not include mold flash or protrusions  
Mold flash or protrusions shall not exceed 0.15mm per side.

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