DATA SHEET

TDA9815
Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator

Product specification
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Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator

TDA9815

FEATURES

- 5 V supply voltage
- Two switched VIF inputs, gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Robustness for over-modulation better than 105% due to gated phase detector at L/L accent standard
- VCO frequency switchable between L and L accent (alignment external) picture carrier frequency
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF-AGC detector for gain control, operating as peak sync detector for B/G, peak white detector for L and peak level for MAC (optional external AGC); signal controlled reaction time for L and MAC
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- AC-coupled limiter amplifier for sound intercarrier signal with input switch for additional FM signal
- Two alignment-free FM-PLL demodulators with high linearity
- SIF input for single reference QSS mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode
- AM demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- ESD protection for all pins.

GENERAL DESCRIPTION

The TDA9815 is an integrated circuit for multistandard vision IF signal processing (inclusive MAC) and sound AM and dual FM demodulation, with single reference QSS-IF in TV and VCR sets.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9815	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	5	5.5	V
I_P	supply current		93	109	125	mA
$V_{i\ VIF(rms)}$	vision IF input signal voltage sensitivity (RMS value)	−1 dB video at output	–	60	100	μV
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage (peak-to-peak value)		1.7	2.0	2.3	V
B_{-3}	−3 dB video bandwidth on pin CVBS	B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
		MAC standard	11	14	–	MHz
S/N (W)	weighted signal-to-noise ratio for video		56	60	–	dB
$IM_{\alpha 1.1}$	intermodulation attenuation at ‘blue’	f = 1.1 MHz	58	64	–	dB
$IM_{\alpha 3.3}$	intermodulation attenuation at ‘blue’	f = 3.3 MHz	58	64	–	dB
$\alpha_{H(sup)}$	suppression of harmonics in video signal		35	40	–	dB
$V_{i\ SIF(rms)}$	sound IF input signal voltage sensitivity (RMS value)	−3 dB at intercarrier output	–	30	70	μV
$V_{o(rms)}$	audio output signal voltage for FM (RMS value)	B/G standard; 54% modulation	–	0.5	–	V
	audio output signal voltage for AM (RMS value)	L standard; 54% modulation	–	0.5	–	V
THD	total harmonic distortion	54% modulation				
	FM		–	0.15	0.5	%
	AM		–	0.5	1.0	%
S/N (W)	weighted signal-to-noise ratio	54% modulation				
	FM		–	60	–	dB
	AM		47	53	–	dB

BLOCK DIAGRAM

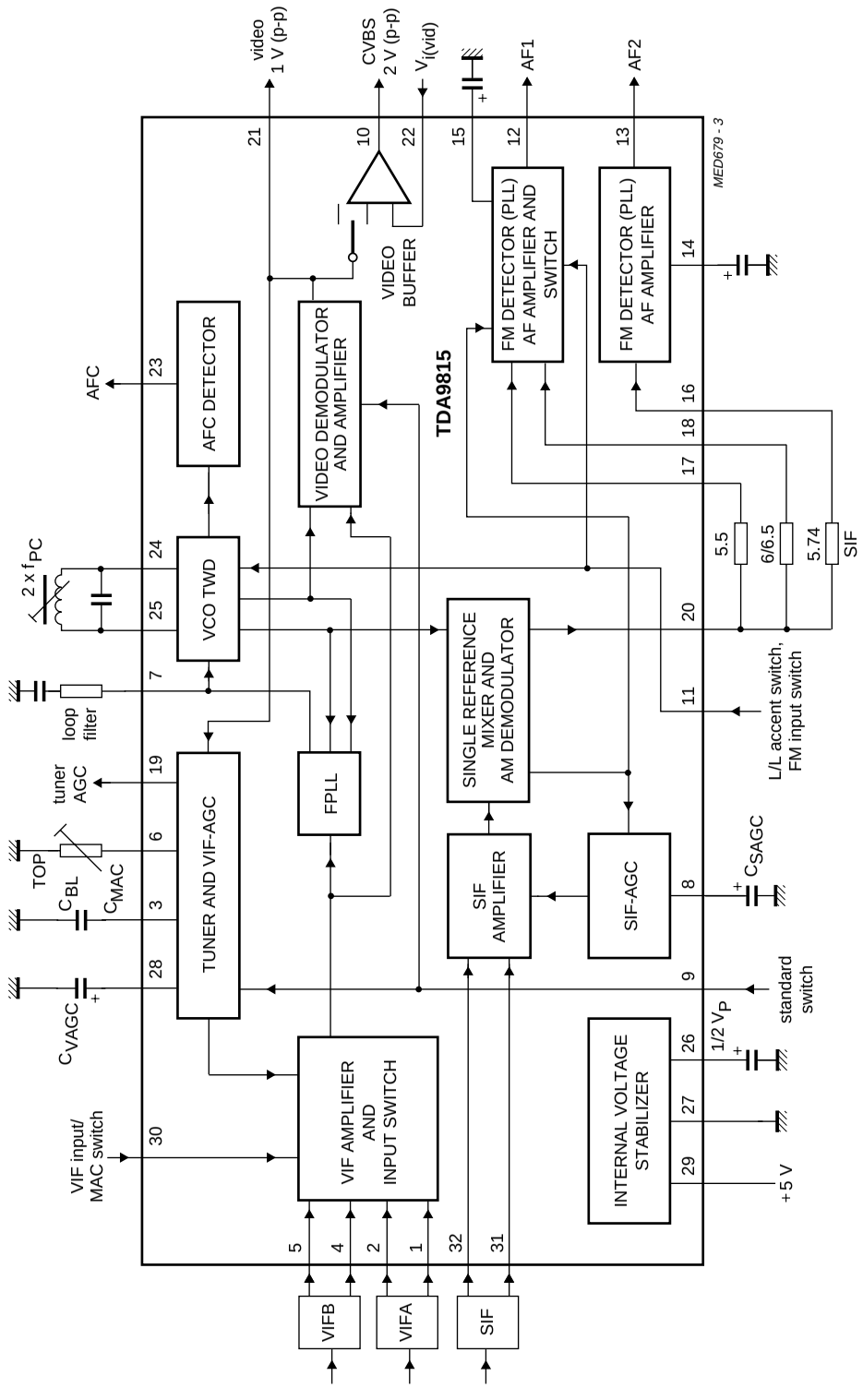


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
$C_{BL/MAC}$	3	black level detector/MAC capacitor
$V_{i\ VIF3}$	4	VIF differential input signal voltage 3
$V_{i\ VIF4}$	5	VIF differential input signal voltage 4
TADJ	6	tuner AGC takeover adjust (TOP)
T_{PLL}	7	PLL loop filter
C_{SAGC}	8	SIF AGC capacitor
STD	9	standard switch
$V_{o\ CVBS}$	10	CVBS output signal voltage
FMLSWI	11	FM input select and L/L accent switch
$V_{o\ AF1}$	12	audio voltage frequency output 1
$V_{o\ AF2}$	13	audio voltage frequency output 2
C_{DEC2}	14	decoupling capacitor 2
C_{DEC1}	15	decoupling capacitor 1
$V_{i\ FM2}$	16	sound intercarrier input voltage 2
$V_{i\ FM1}$	17	sound intercarrier input voltage 1
$V_{i\ FM3}$	18	sound intercarrier input voltage 3
TAGC	19	tuner AGC output
$V_{o\ QSS}$	20	single reference QSS output voltage
$V_{o(vid)}$	21	composite video output voltage
$V_{i(vid)}$	22	video buffer input voltage
AFC	23	AFC output
VCO1	24	VCO1 reference circuit for $2f_{PC}$
VCO2	25	VCO2 reference circuit for $2f_{PC}$
C_{ref}	26	$\frac{1}{2}V_P$ reference capacitor
GND	27	ground
C_{VAGC}	28	VIF-AGC capacitor
V_P	29	supply voltage
INSWI	30	VIF input switch
$V_{i\ SIF1}$	31	SIF differential input signal voltage 1
$V_{i\ SIF2}$	32	SIF differential input signal voltage 2

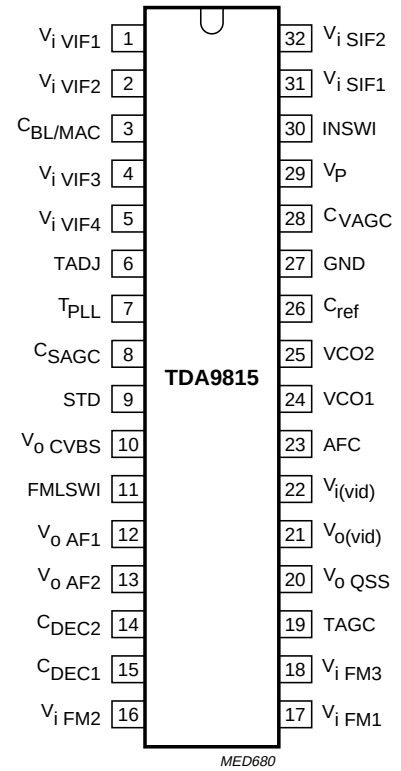


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The integrated circuit comprises the functional blocks as shown in Fig.1:

- Vision IF amplifier and input switch
- Tuner and VIF-AGC
- Frequency Phase Locked Loop detector (FPLL)
- VCO, Travelling Wave Divider (TWD) and AFC
- Video demodulator and amplifier
- Video buffer
- SIF amplifier and AGC
- Single reference QSS mixer
- AM demodulator
- FM-PLL demodulator
- Internal voltage stabilizer and $\frac{1}{2}V_P$-reference.

Vision IF amplifier and input switch

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration. The first differential stage is extended by two pairs of emitter followers to provide two IF input channels. The VIF input can be selected by pin 30.

Tuner and VIF-AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output). The tuner AGC takeover point can be adjusted. This allows the tuner and the SAW filter to be matched to achieve the optimum IF input level.

The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive (or MAC) modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black level detector voltage.

Frequency Phase Locked Loop detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the frequency-phase detector (FPLL) and fed via the loop filter to the first variable capacitor. This control voltage is amplified and additionally converted into a current which represents the AFC output signal. The VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the L accent switch. In this event the second variable capacitor can be controlled by a variable resistor at the L accent switch for setting the VCO centre frequency to the required L accent value. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the ‘in phase’ signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used in the event of B/G and L standard. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted for operating in combination with ceramic sound traps. The output stage delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.

For MAC standard a second buffer amplifier with 6 dB gain is used. This buffer amplifier is selected by the standard switch.

SIF amplifier and AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF input signals (average level of AM or FM carriers) and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. The SIF AGC reaction time is set to ‘slow’ for nominal video conditions. But with a decreasing VIF amplitude step the SIF AGC is set to ‘fast’ mode controlled by the VIF-AGC detector. In FM mode this reaction time is also set to ‘fast’ controlled by the standard switch.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 20. With this system a high performance hi-fi stereo sound processing can be achieved.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the AF amplifier.

FM-PLL demodulator

Each FM-PLL demodulator consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC-coupled in order to minimize the DC offset and to save pins for DC decoupling.

At the input of one limiter a signal switch is available for selecting one of the two intercarrier signals. Controlled by the voltage at pin 11, either the input pin 17 or pin 18 is active for handling different intercarrier frequencies.

The other limiter is extended with an additional level detector consisting of a rectifier and a comparator. By means of this the AF2 signal is set to mute and the PLL VCO is switched off, if the intercarrier signal at pin 16 is below 1 mV (RMS) in order to avoid false identification of a stereo decoder. Note that noise at pin 16 disables the mute state (at low SIF input signal), but this will not lead to false identification. This ‘auto-mute’ function can be disabled by connecting a 5.6 kΩ resistor from pin 16 to V_P (see Fig.13).

Furthermore the AF output signals can be muted by connecting a resistor between the limiter inputs pin 16 or pin 17 and ground.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM-demodulator.

The AF amplifier consists of two parts:

1. The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to AM/FM or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer and $\frac{1}{2}V_P$-reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $\frac{1}{2}V_P$ voltage has to be filtered via a low-pass filter by using an external capacitor together with an integrated resistor (f_g = 5 Hz). For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 29)	maximum chip temperature of 125 °C; note 1	0	7.0	V
V_i	voltage at pins 1 to 9, 11 to 19, 22, 23 and 26 to 32		0	V_P	V
$t_{s(max)}$	maximum short-circuit time		–	10	s
V_{19}	tuner AGC output voltage		0	13.2	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling voltage	note 2	–300	+300	V

Notes

1. I_P = 125 mA; T_{amb} = 70 °C; $R_{th(j-a)}$ = 60 K/W.
2. Machine model class B (L = 2.5 μH).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; see Table 1 for input frequencies and carrier ratios; input level $V_{i\ IF\ 1\text{-}2,\ 4\text{-}5}$ = 10 mV RMS value (sync-level for B/G, peak white level for L, peak level for MAC); video modulation DSB; residual carrier B/G and MAC: 10%; L = 3%; video signal in accordance with *"CCIR, line 17"*; measurements taken in Fig.13; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 29)						
V_P	supply voltage	note 1	4.5	5	5.5	V
I_P	supply current		93	109	125	mA
Vision IF amplifier (pins 1, 2, 4 and 5)						
$V_{i\ VIF(rms)}$	input signal voltage sensitivity (RMS value)	B/G standard; −1 dB video at output	–	60	100	μV
$V_{i\ max(rms)}$	maximum input signal voltage (RMS value)	B/G standard; +1 dB video at output	120	200	–	mV
$\Delta V_{o(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range				
		B/G standard; Δf = 5.5 MHz	–	0.7	1	dB
		MAC standard; Δf = 8.4 MHz	–	1.0	1.3	dB
G_{IFcr}	IF gain control range	see Fig.3	65	70	–	dB
$R_{i(diff)}$	differential input resistance	note 2; activated input	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2; activated input	1.2	1.7	2.5	pF
$V_{1,2,4,5}$	DC input voltage	note 2; activated input	–	3.4	–	V
R_i	input resistance to ground	note 2; not activated input	–	1.1	–	kΩ
$V_{1,2,4,5}$	DC input voltage	note 2; not activated input	–	0.2	–	V
$\alpha_{ct\ IF}$	crosstalk attenuation of IF input switch at pins 1, 2, 4 and 5	notes 2 and 3	55	60	–	dB
True synchronous video demodulator; note 4						
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	125	130	–	MHz
$\Delta f_{osc}/\Delta T$	oscillator drift as a function of temperature	oscillator is free-running; I_{AFC} = 0; note 5	–	–	$\pm 20 \times 10^{-6}$	K^{-1}
$V_{0\ ref(rms)}$	oscillator voltage swing at pins 24 and 25 (RMS value)		70	100	130	mV
$f_{PC\ CR}$	picture carrier capture range	B/G, L and MAC standard	±1.4	±1.8	–	MHz
		L accent standard; f_{PC} = 33.9 MHz; R_{11} = 5.6 kΩ	±0.9	±1.2	–	MHz
$Qf_{PC(fr)}$	picture carrier frequency (free-running) accuracy	L accent standard; f_{PC} = 33.9 MHz; R_{11} = 5.6 kΩ	–	±200	±400	kHz
$f_{PC(alg)CR}$	L accent alignment frequency range	I_{AFC} = 0	±400	±600	–	kHz
t_{acq}	acquisition time	BL = 75 kHz; note 6	–	–	30	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i\ VIF(rms)}$	VIF input signal voltage sensitivity for PLL to be locked (RMS value; pins 1, 2, 4 and 5)	maximum IF gain; note 7	–	30	70	μV
Composite video amplifier (pin 21; sound carrier off)						
$V_{o\ video(p-p)}$	output signal voltage (peak-to-peak value)	see Fig.8	0.88	1.0	1.12	V
V/S	ratio between video (black-to-white) and sync level		1.9	2.33	3.0	–
$\Delta V_{o(video)}$	output signal voltage difference	difference between B/G and L standard	–	–	±12	%
$V_{21(sync)}$	sync voltage level	B/G and L standard	–	1.5	–	V
$V_{21(clu)}$	upper video clipping voltage level		$V_P - 1.1$	$V_P - 1$	–	V
$V_{21(cll)}$	lower video clipping voltage level		–	0.7	0.9	V
$R_{o,21}$	output resistance	note 2	–	–	10	Ω
$I_{int\ 21}$	internal DC bias current for emitter-follower		2.2	3.0	–	mA
$I_{21\ max(sink)}$	maximum AC and DC output sink current		1.6	–	–	mA
$I_{21\ max(source)}$	maximum AC and DC output source current		2.9	–	–	mA
B_{-1}	–1 dB video bandwidth	B/G and L standard; $C_L < 50$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
B_{-3}	–3 dB video bandwidth	B/G and L standard; $C_L < 50$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
$\alpha_{H(sup)}$	suppression of video signal harmonics	$C_L < 50$ pF; $R_L > 1$ kΩ; AC load; note 8a	35	40	–	dB
PSRR	power supply ripple rejection at pin 21	video signal; grey level; see Fig.11				
		B/G standard	32	35	–	dB
		L standard	26	30	–	dB
CVBS buffer amplifier (only) and noise clipper (pins 10 and 22)						
$R_{i,22}$	input resistance	note 2	2.6	3.3	4.0	kΩ
$C_{i,22}$	input capacitance	note 2	1.4	2	3.0	pF
$V_{I,22}$	DC input voltage		1.4	1.7	2.0	V
G_v	voltage gain	B/G and L standard; note 9	6.5	7	7.5	dB
$V_{10(clu)}$	upper video clipping voltage level		3.9	4.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{10(cll)}$	lower video clipping voltage level		–	1.0	1.1	V
$R_{o,10}$	output resistance	note 2	–	–	10	Ω
$I_{int\ 10}$	DC internal bias current for emitter-follower		2.0	2.5	–	mA
$I_{o,10\ max(sink)}$	maximum AC and DC output sink current		1.4	–	–	mA
$I_{o,10\ max(source)}$	maximum AC and DC output source current		2.4	–	–	mA
B_{-1}	–1 dB video bandwidth	B/G and L standard; C_L < 20 pF; R_L > 1 kΩ; AC load	8.4	11	–	MHz
B_{-3}	–3 dB video bandwidth	B/G and L standard; C_L < 20 pF; R_L > 1 kΩ; AC load	11	14	–	MHz
Measurements from IF input to CVBS output (pin 10; 330 Ω between pins 21 and 22, sound carrier off)						
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage on pin 10 (peak-to-peak value)	note 9	1.7	2.0	2.3	V
$V_{o\ CVBS(sync)}$	sync voltage level	B/G standard	–	1.35	–	V
		L standard	–	1.35	–	V
$V_{o\ CVBS(peak)}$	peak voltage level	MAC standard	–	1.35	–	V
ΔV_o	deviation of CVBS output signal voltage at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
$\Delta V_{o(blB/G)}$	black level tilt in B/G standard	gain variation; note 10	–	–	1	%
$\Delta V_{o(blL)}$	black level tilt for worst case in L standard	picture carrier modulated by test line (VITS) only; gain variation; note 10	–	–	1.9	%
G_{diff}	differential gain	*"CCIR, line 330"*	–	2	5	%
φ_{diff}	differential phase	*"CCIR, line 330"*	–	1	2	deg
B_{-1}	–1 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load				
		B/G and L standard	5	6	–	MHz
		MAC standard	8.4	11	–	MHz
B_{-3}	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load				
		B/G and L standard	7	8	–	MHz
		MAC standard	11	14	–	MHz
S/N (W)	weighted signal-to-noise ratio	see Fig.5 and note 11	56	60	–	dB
S/N	unweighted signal-to-noise ratio	see Fig.5 and note 11	49	53	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$IM\alpha_{1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz; see Fig.6 and note 12	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 1.1 MHz; see Fig.6 and note 12	60	66	–	dB
$IM\alpha_{3.3}$	intermodulation attenuation at 'blue'	f = 3.3 MHz; see Fig.6 and note 12	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 3.3 MHz; see Fig.6 and note 12	59	65	–	dB
$\alpha_{pc(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics				
		B/G and L standard	–	2	5	mV
		MAC standard	–	5	20	mV
$\Delta f_{unwanted(p-p)}$	robustness for unwanted frequency deviation of picture carrier (peak-to-peak value)	L standard; residual carrier: 3%; serration pulses: 50%; note 2	–	–	12	kHz
$\Delta\varphi$	robustness for modulator imbalance	L standard; residual carrier: 0%; serration pulses: 50%; note 2	–	–	3	%
$\alpha_{H(sup)}$	suppression of video signal harmonics	note 8a	35	40	–	dB
$\alpha_{H(spur)}$	spurious elements	note 8b	40	–	–	dB
PSRR	power supply ripple rejection at pin 10	video signal; grey level; see Fig.11				
		B/G standard	25	28	–	dB
		L standard	20	23	–	dB
VIF-AGC detector (pin 28)						
I_{28}	charging current	B/G, L and MAC standard; note 10	0.75	1	1.25	mA
	additional charging current	L standard in event of missing VITS pulses and no white video content	1.9	2.5	3.1	µA
	discharging current	B/G standard	15	20	25	µA
		normal mode L and MAC standard	225	300	375	nA
		fast mode L and MAC standard	30	40	50	µA
t_{resp}	AGC response to an increasing VIF step	B/G, L and MAC standard; note 13	–	0.05	0.1	ms/dB
	AGC response to a decreasing VIF step	B/G standard	–	2.2	3.5	ms/dB
		fast mode L and MAC standard	–	1.1	1.8	ms/dB
		normal mode L and MAC standard; note 13	–	150	240	ms/dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔIF	VIF amplitude step for activating fast AGC mode	L and MAC standard	–2	–6	–10	dB
$V_{3(th)}$	threshold voltage level additional charging current	see Fig.8				
		L standard	–	1.95	–	V
		L standard; fast mode L	–	1.65	–	V
		MAC standard; fast mode MAC	–	1.9	–	V
Tuner AGC (pin 19)						
$V_{i(rms)}$	IF input signal voltage for minimum starting point of tuner takeover (RMS value)	input at pins 1, 2, 4 and 5; R_{TOP} = 22 kΩ; I_{19} = 0.4 mA	–	2	5	mV
	IF input signal voltage for maximum starting point of tuner takeover (RMS value)	input at pins 1, 2, 4 and 5; R_{TOP} = 0 Ω; I_{19} = 0.4 mA	50	100	–	mV
$V_{o,19}$	permissible output voltage	from external source; note 2	–	–	13.2	V
$V_{sat,19}$	saturation voltage	I_{19} = 1.5 mA	–	–	0.2	V
$\Delta V_{TOP,19}/\Delta T$	variation of takeover point by temperature	I_{19} = 0.4 mA	–	0.03	0.07	dB/K
$I_{19(sink)}$	sink current	see Fig.3				
		no tuner gain reduction; V_{19} = 13.2 V	–	–	1	μA
		maximum tuner gain reduction	1.5	2	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 23); see Fig.7 and note 14						
S	control steepness $\Delta I_{23}/\Delta f$	note 15	0.5	0.75	1.0	μA/kHz
$\Delta f_{IF}/\Delta T$	frequency variation by temperature	I_{AFC} = 0; note 6				
		B/G and L standard	–	–	$\pm 20 \times 10^{-6}$	K^{-1}
		L accent standard	–	–	$\pm 60 \times 10^{-6}$	K^{-1}
$V_{o,23}$	output voltage upper limit	see Fig.7 without external components	V_P – 0.6	V_P – 0.3	–	V
	output voltage lower limit		–	0.3	0.6	V
$I_{o,23(source)}$	output source current	see Fig.7	150	200	250	μA
$I_{o,23(sink)}$	output sink current		150	200	250	μA
$\Delta I_{23(p-p)}$	residual video modulation current (peak-to-peak value)	B/G and L standard	–	20	30	μA
Sound IF amplifier (pins 31 and 32)						
$V_{i\ SIF(rms)}$	input signal voltage sensitivity (RMS value)	FM mode; –3 dB at intercarrier output pin 20	–	30	70	μV
		AM mode; –3 dB at AF output pin 12	–	70	100	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i\ max(rms)}$	maximum input signal voltage (RMS value)	FM mode; +1 dB at intercarrier output pin 20	50	70	–	mV
		AM mode; +1 dB at AF output pin 12	80	140	–	mV
G_{SIFcr}	SIF gain control range	FM and AM mode; see Fig.4	60	67	–	dB
$R_{i(diff)}$	differential input resistance	note 2	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2	1.2	1.7	2.5	pF
$V_{I(31,32)}$	DC input voltage		–	3.4	–	V
$\alpha_{ct(SIF,VIF)}$	crosstalk attenuation between SIF and VIF input	between pins 1, 2, 4 and 5 and pins 31 and 32; note 3	50	–	–	dB
SIF-AGC detector (pin 8)						
I_8	charging current	FM mode	8	12	16	μA
		AM mode	0.8	1.2	1.6	μA
	discharging current	FM mode	8	12	16	μA
		normal mode AM	1	1.4	1.8	μA
		fast mode AM	60	85	110	μA
Single reference QSS intercarrier mixer (B/G standard; pin 20)						
$V_{o(rms)}$	IF intercarrier level (RMS value)	SC_1; sound carrier 2 off	75	100	125	mV
B_{-3}	–3 dB intercarrier bandwidth	upper limit	7.5	9	–	MHz
$\alpha_{SC(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	2	–	mV
$R_{o,20}$	output resistance	note 2	–	–	25	Ω
$V_{O,20}$	DC output voltage		–	2.0	–	V
$I_{int\ 20}$	DC internal bias current for emitter-follower		1.5	1.9	–	mA
$I_{20\ max(sink)}$	maximum AC and DC output sink current		1.1	1.5	–	mA
$I_{20\ max(source)}$	maximum AC and DC output source current		3.0	3.5	–	mA
FM input stage and limiter amplifier 1 (pins 17 and 18); note 16						
$V_{i\ FM(rms)}$	input signal voltage for lock-in (RMS value)		–	–	100	μV
$V_{i\ FM(rms)}$	input signal voltage (RMS value)	$\frac{S+N}{N}$ = 40 dB	–	300	400	μV
	allowed input signal voltage (RMS value)		200	–	–	mV
$R_{i(17,18)}$	input resistance	activated input; note 2	480	600	720	Ω
		not activated input; note 2	–	–	100	Ω
$V_{I(17,18)}$	DC input voltage	activated input	–	2.8	–	V
		not activated input pin 17	–	1.8	–	V
		not activated input pin 18	–	–	0.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cr}	crosstalk attenuation	activated to not activated input; not activated input terminated with an impedance of 600 Ω (AC-coupled)	44	50	–	dB
Limiter amplifier 2 (pin 16); note 16						
$V_{i\ FM(rms)}$	input signal voltage for lock-in (RMS value)		–	–	100	μV
$V_{i\ FM(rms)}$	input signal voltage (RMS value)	$\frac{S+N}{N}$ = 40 dB PLL1 has to be in locked mode; auto mute off	–	300	400	μV
	allowed input signal voltage (RMS value)		200	–	–	mV
	input signal voltage for no auto mute; PLL enabled (RMS value)		0.7	1	1.5	mV
HYS_{16}	hysteresis of level detector for auto mute		–3	–6	–8	dB
$R_{i,16}$	input resistance	note 2	480	600	720	Ω
$V_{I,16}$	DC input voltage		–	2.0	–	V
FM-PLL demodulator						
$f_{i\ FM(catch)}$	catching range of PLL	upper limit	7.0	–	–	MHz
		lower limit	–	–	4.0	MHz
$f_{i\ FM(hold)}$	holding range of PLL	upper limit	8.0	–	–	MHz
		lower limit	–	–	3.5	MHz
t_{acq}	acquisition time		–	–	4	μs
FM operation (B/G standard; pins 12 and 13); notes 16 and 16a						
$V_{o\ AF12,13(rms)}$	AF output signal voltage (RMS value)	27 kHz (54% FM deviation); see Fig.13 and note 17				
		$R_x = R_y = 470\ \Omega$	200	250	300	mV
		$R_x = R_y = 0\ \Omega$	400	500	600	mV
$V_{o\ AF12,13(cl)}$	AF output clipping signal voltage level	THD < 1.5%	1.3	1.4	–	V
Δf_{AF}	frequency deviation	THD < 1.5%; note 17	–	–	53	kHz
$\Delta V_o/\Delta T$	temperature drift of AF output signal voltage		–	3×10^{-3}	7×10^{-3}	dB/K
$V_{14,15}$	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 18	1.2	–	3.0	V
$R_{12,13}$	output resistance	note 2	–	–	100	Ω
$V_{12,13}$	DC output voltage	tracked with supply voltage	–	$\frac{1}{2}V_P$	–	V
$I_{12,13max(sink)}$	maximum AC and DC output sink current		–	–	1.1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{12,13max(source)}$	maximum AC and DC output source current		–	–	1.1	mA
B_{-3}	–3 dB video bandwidth		100	125	–	kHz
THD	total harmonic distortion		–	0.15	0.5	%
S/N (W)	weighted signal-to-noise ratio	FM-PLL only; with 50 µs de-emphasis; 27 kHz (54% FM deviation); *"CCIR 468-4"*	55	60	–	dB
$\alpha_{SC(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	–	75	mV
α_{AM}	AM suppression	50 µs de-emphasis; AM: f = 1 kHz; m = 0.3 refer to 27 kHz (54% FM deviation)	46	50	–	dB
$\alpha_{12,13}$	mute attenuation of AF signal	B/G and L standard	70	80	–	dB
$\Delta V_{12,13}$	DC jump voltage of AF output terminals for switching AF output to mute state and vice versa	FM-PLLs in lock mode; note 19	–	±50	±150	mV
PSRR	power supply ripple rejection at pins 12 and 13	$R_x = R_y = 0\ \Omega$; see Figs 11 and 13	22	28	–	dB
Single reference QSS AF performance for FM operation (B/G standard); (notes 20, 21 and 22; see Table 1)						
S/N (W)	weighted signal-to-noise ratio (SC_1/SC_2)	PC/SC_1 ratio at pins 1 and 2; 27 kHz (54% FM deviation); *"CCIR 468-4"*	40	–	–	dB
		black picture	53/48	58/55	–	dB
		white picture	50/46	55/52	–	dB
		6 kHz sine wave; black-to-white modulation	42/40	48/46	–	dB
		250 kHz square wave; black-to-white modulation; see note 2 in Fig.13	45/42	53/50	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	45/44	51/50	–	dB
		sound carrier subharmonics; f = 2.87 MHz ±3 kHz	46/45	52/51	–	dB
AM operation (L standard; pin 12); note 23						
$V_{o\ AF12(rms)}$	AF output signal voltage (RMS value)	54% modulation	400	500	600	mV
THD	total harmonic distortion	54% modulation; see Fig.10	–	0.5	1.0	%
B_{-3}	–3 dB AF bandwidth		100	125	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N (W)	weighted signal-to-noise ratio	*"CCIR 468-4"*; see Fig.9	47	53	–	dB
V_{12}	DC potential voltage	tracked with supply voltage	–	$\frac{1}{2}V_P$	–	V
PSRR	power supply ripple rejection	see Fig.11	22	25	–	dB
Standard switch (pin 9); see also Table 2						
V_9	DC potential voltage for preferred settings					
	input voltage for negative standard	B/G and MAC standard; note 24	2.8	–	V_P	V
	input voltage for negative standard	negative AGC **off**	1.3	–	2.3	V
	input voltage for positive standard	L standard	0	–	0.8	V
I_{IL}	LOW-level input current	V_9 = 0 V	190	250	310	μA
VIF input switch (pin 30); see also Table 2						
V_{30}	DC potential voltage for preferred settings					
	input voltage for VIF input A	B/G and L standard; note 24	2.8	–	V_P	V
	input voltage for VIF input B	MAC standard	1.3	–	2.3	V
	input voltage for VIF input B	B/G and L standard	0	–	0.8	V
I_{IL}	LOW-level input current	V_{30} = 0 V	170	230	290	μA
FM input and L accent switch (pin 11)						
V_{11}	DC potential voltage for FM input selection					
	input pin 17 activated	note 24	2.8	–	V_P	V
	input pin 18 activated	22 kΩ potentiometer only for L accent alignment required; see Fig.13	0	–	2.0	V
	DC potential voltage for L standard VCO frequency switching					
	L standard	note 24	2.8	–	V_P	V
	L accent standard and alignment		0	–	2.0	V
I_{IL}	LOW-level input current	V_{11} = 0 V	150	200	250	μA

Notes to the characteristics

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as application information for designing the television receiver.
3. Source impedance: 2.3 kΩ in parallel to 12 pF (SAW filter); f_{IF} = 38.9 MHz.

4. Loop bandwidth BL = 75 kHz (natural frequency f_n = 11 kHz; damping factor d ≈ 3.5; calculated with sync level within gain control range). Resonance circuit of VCO: Q_0 > 50; C_{ext} = 8.2 pF ±0.25 pF; C_{int} ≈ 8.5 pF (loop voltage approximately 2.7 V).
5. Temperature coefficient of external LC-circuit is equal to zero.
6. $V_{i\ IF}$ = 10 mV RMS; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
7. $V_{i\ IF}$ signal for nominal video signal.
8. Measurements taken with SAW filter G3962 (sound carrier suppression: 40 dB); loop bandwidth BL = 75 kHz:
   a) Modulation VSB; sound carrier **off**; f_{video} > 0.5 MHz.
   b) Sound carrier **on**; SIF SAW filter L9453; f_{video} = 10 kHz to 10 MHz.
9. The 7 dB buffer gain accounts for 1 dB loss (not valid for MAC) in the sound trap. Buffer output signal is typical 2 V (p-p), in event of CVBS video amplifier output typical 1 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 21 to pin 22).
10. The leakage current of the AGC capacitor should not exceed 1 μA at B/G standard respectively 10 nA current at L standard. Larger currents will increase the tilt.
11. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 10). B = 5 MHz weighted in accordance with *"CCIR 567"*.
12. The intermodulation figures are defined:

    $\alpha_{1.1} = 20 \log\left(\frac{V_0 \text{ at } 4.4\text{ MHz}}{V_0 \text{ at } 1.1\text{ MHz}}\right) + 3.6\,\text{dB}$; $\alpha_{1.1}$ value at 1.1 MHz referenced to black/white signal;

    $\alpha_{3.3} = 20 \log\left(\frac{V_0 \text{ at } 4.4\text{ MHz}}{V_0 \text{ at } 3.3\text{ MHz}}\right)$; $\alpha_{3.3}$ value at 3.3 MHz referenced to colour carrier.
13. Response speed valid for a VIF input level range of 200 μV up to 70 mV.
14. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.7. The AFC-steepness can be changed by the resistors at pin 23.
15. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO (Q_0 > 50; see note 4; $C_0 = C_{int} + C_{ext}$).
16. Input level for second IF from an external generator with 50 Ω source impedance. AC-coupled with 10 nF capacitor, f_{mod} = 1 kHz, 27 kHz (54% FM deviation) of audio references. A VIF/SIF input signal is not permitted. Pins 8 and 28 have to be connected to positive supply voltage for minimum IF gain. S/N and THD measurements are taken at 50 μs de-emphasis. The not tested FM-PLL has to be locked to an unmodulated carrier.
    a) Second IF input level 10 mV RMS.
17. Measured with an FM deviation of 27 kHz the typical AF output signal is 500 mV RMS ($R_x = R_y$ = 0 Ω; see Fig.13). By using $R_x = R_y$ = 470 Ω the AF output signal is attenuated by 6 dB (250 mV RMS) and adapted to the stereo decoder family TDA9840. For handling an FM deviation of more than 53 kHz the AF output signal has to be reduced by using R_x and R_y in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended with $R_x = R_y$ = 470 Ω.
18. The leakage current of the decoupling capacitor (2.2 μF) should not exceed 1 μA.
19. In the event of activated auto mute state the second FM-PLL oscillator is switched off, if the input signal at pin 16 is missing or too weak (see Fig.13). In the event of switching the second FM-PLL oscillator on by the auto mute stage an increased DC jump is the consequence. Note, that noise at pin 16 disables the mute state (at low SIF input signal), but this will not lead to false identification of the used stereo decoder family TDA9840.

20. For all S/N measurements the used vision IF modulator has to meet the following specifications:
    a) Incidental phase modulation for black-to-white jump less than 0.5 degrees.
    b) QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 27 kHz) for 6 kHz sine wave black-to-white video modulation.
    c) Picture-to-sound carrier ratio; PC/SC_1 = 13 dB (transmitter).
21. Measurements taken with SAW filter G3962 (Siemens) for vision IF (suppressed sound carrier) and G9350 (Siemens) for sound IF (suppressed picture carrier). Input level $V_{i\ SIF}$ = 10 mV RMS, 27 kHz (54% FM deviation).
22. The PC/SC ratio at pins 1 and 2 is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N(W) values as noted. A different PC/SC ratio will change these values.
23. Measurements taken with SAW filter L9453 (Siemens) for AM sound IF (suppressed picture carrier).
24. The input voltage has to be V_i > 2.8 V or open-circuit.

Table 1 Input frequencies and carrier ratios

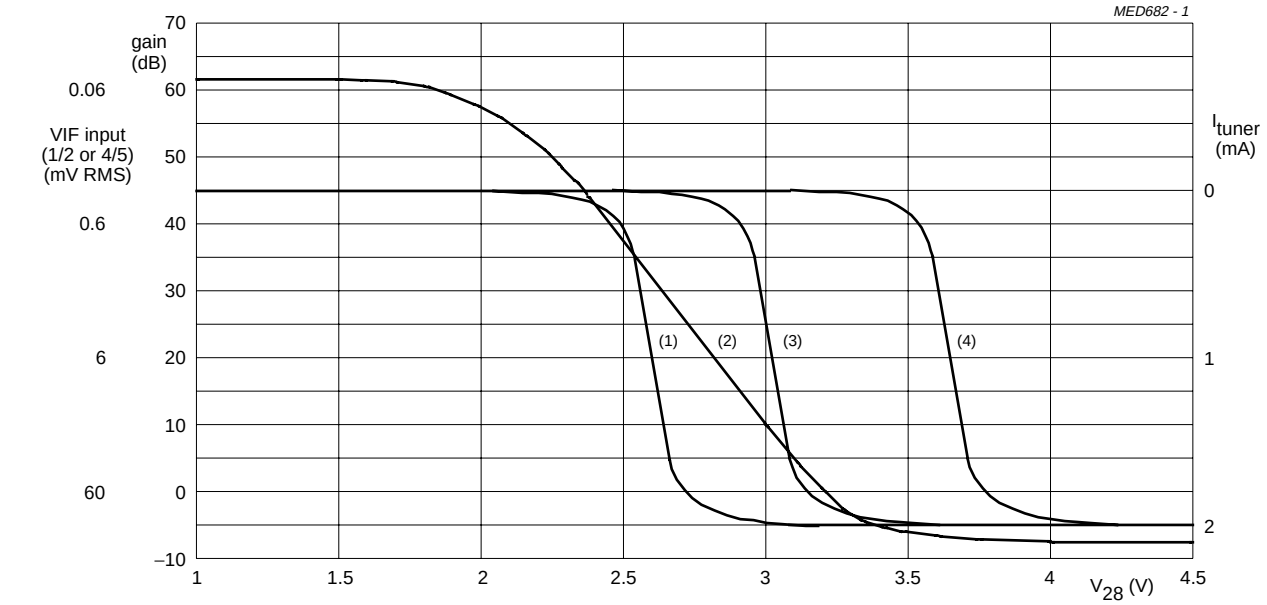
DESCRIPTION	SYMBOL	B/G STANDARD	L STANDARD	L ACCENT STANDARD	UNIT
Picture carrier	f_{PC}	38.9	38.9	33.9	MHz
Sound carrier	f_{SC1}	33.4	32.4	40.4	MHz
	f_{SC2}	33.158	–	–	MHz
Picture-to-sound carrier ratio	SC_1	13	10	10	dB
	SC_2	20	–	–	dB

Table 2 Switch logic

INPUT SWITCH (PIN 30)	STANDARD SWITCH (PIN 9)	SELECTED VIF INPUT	SELECTED STANDARD	VIDEO POLARITY	FM-PLL		AF-AMPLIFIER	
					1	2	1	2
2.8 V to V_P	2.8 V to V_P	A	B/G	negative	on	on	FM	FM
	1.3 to 2.3 V	A	B/G, with external VIF-AGC	negative	on	on	FM	FM
	0 to 0.8 V	A	L	positive	off	off	AM	mute
1.3 to 2.3 V	2.8 V to V_P	B	MAC (note 1)	negative	off	off	mute	mute
	1.3 to 2.3 V	B	MAC (note 1), with external VIF-AGC	negative	off	off	mute	mute
	0 to 0.8 V	B	L (note 1)	positive	off	off	AM	mute
0 to 0.8 V	2.8 V to V_P	B	B/G	negative	on	on	FM	FM
	1.3 to 2.3 V	B	B/G, with external VIF-AGC	negative	on	on	FM	FM
	0 to 0.8 V	B	L	positive	off	off	AM	mute

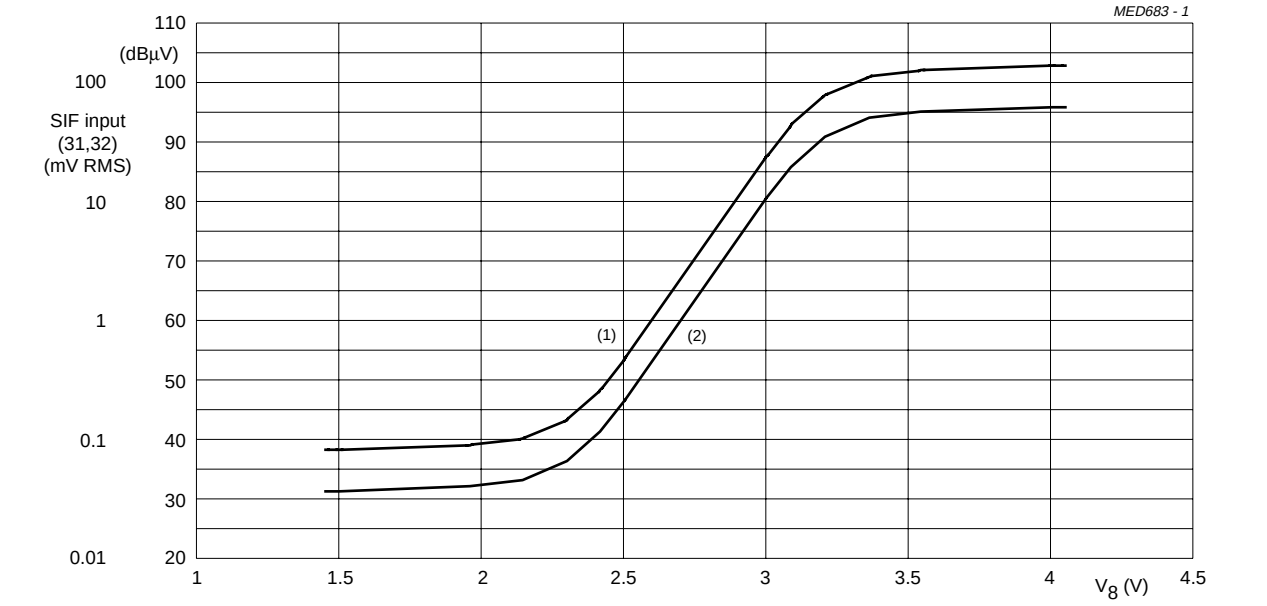
Note

1. Without external sound trap (video signal internally switched to video buffer).



(1) I_{tuner}; R_{TOP} = 22 kΩ.
(2) Gain.
(3) I_{tuner}; R_{TOP} = 11 kΩ.
(4) I_{tuner}; R_{TOP} = 0 Ω.

Fig.3 Typical VIF and tuner AGC characteristic.



(1) AM mode.
(2) FM mode.

Fig.4 Typical SIF AGC characteristic.

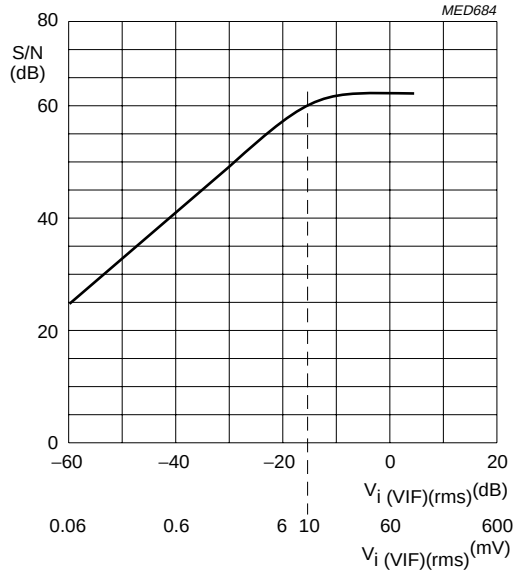
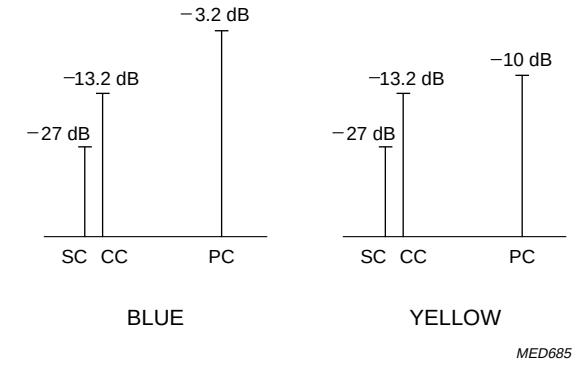
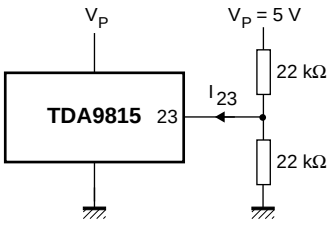


Fig.5 Typical signal-to-noise ratio as a function of IF input voltage.



SC = sound carrier, with respect to sync level.
CC = chrominance carrier, with respect to sync level.
PC = picture carrier, with respect to sync level.
The sound carrier levels are taking into account a sound shelf attenuation of 20 dB (SAW filter G1962).

Fig.6 Input signal conditions.



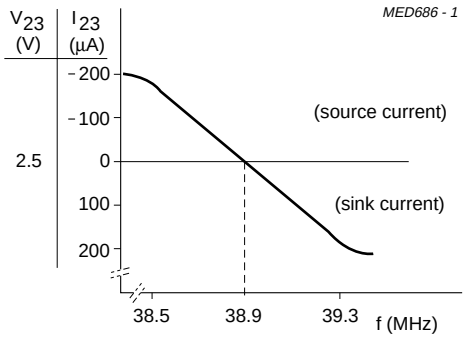


Fig.7 Measurement conditions and typical AFC characteristic.

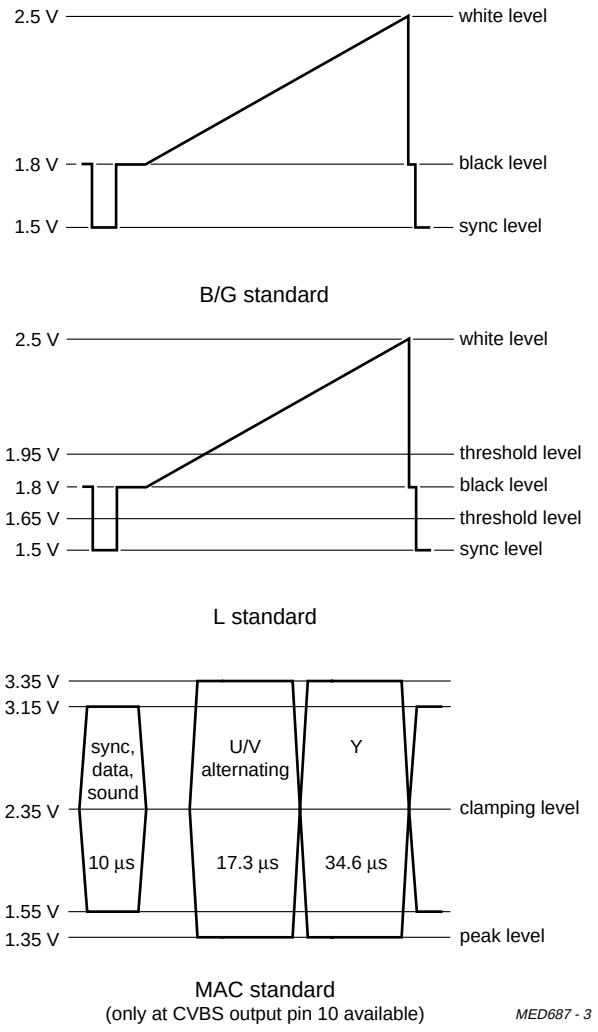
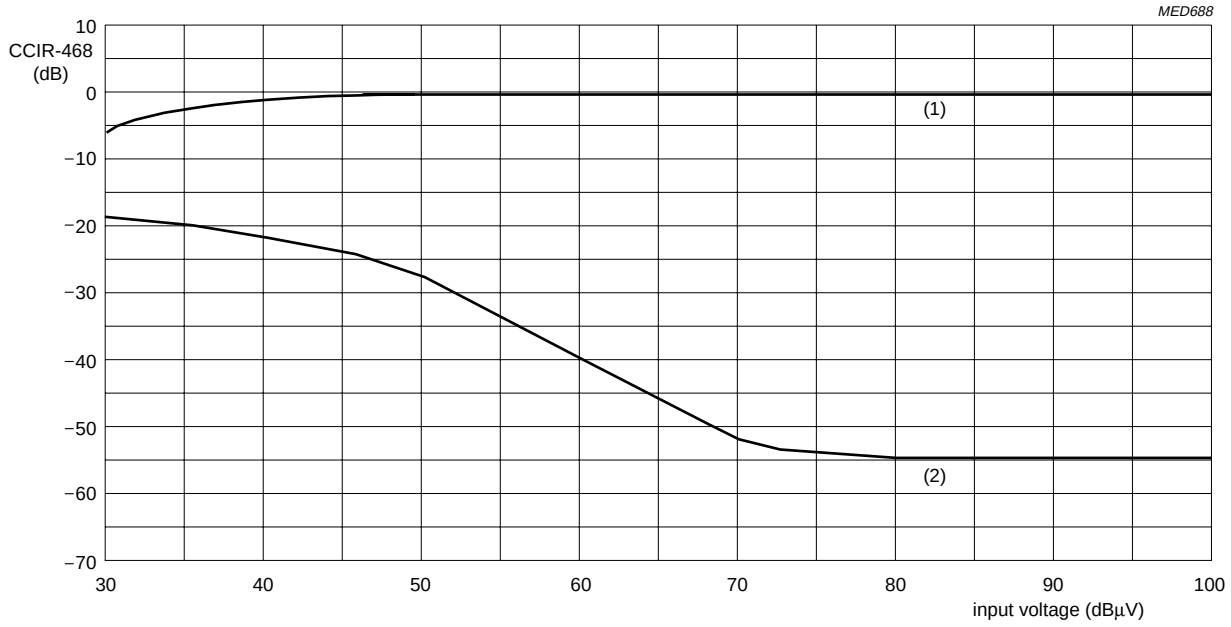
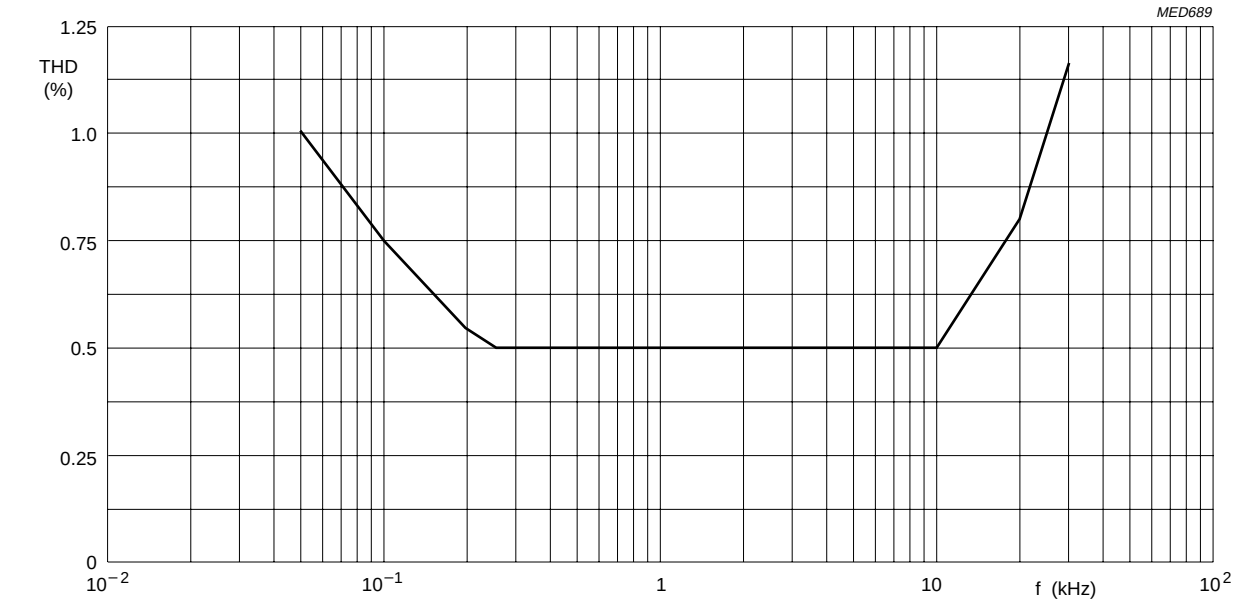


Fig.8 Typical video signal levels on output pin 21 (sound carrier **off**).



(1) Signal. m = 54%.
(2) Noise.

Fig.9 Typical audio signal-to-noise ratio as a function of input signal at AM standard.



C_{AGC} = 2.2 μF.
m = 54%.

Fig.10 Typical total harmonic distortion as a function of audio frequency at AM standard.

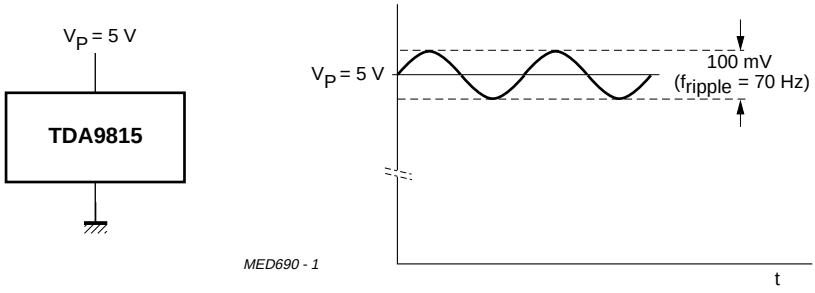
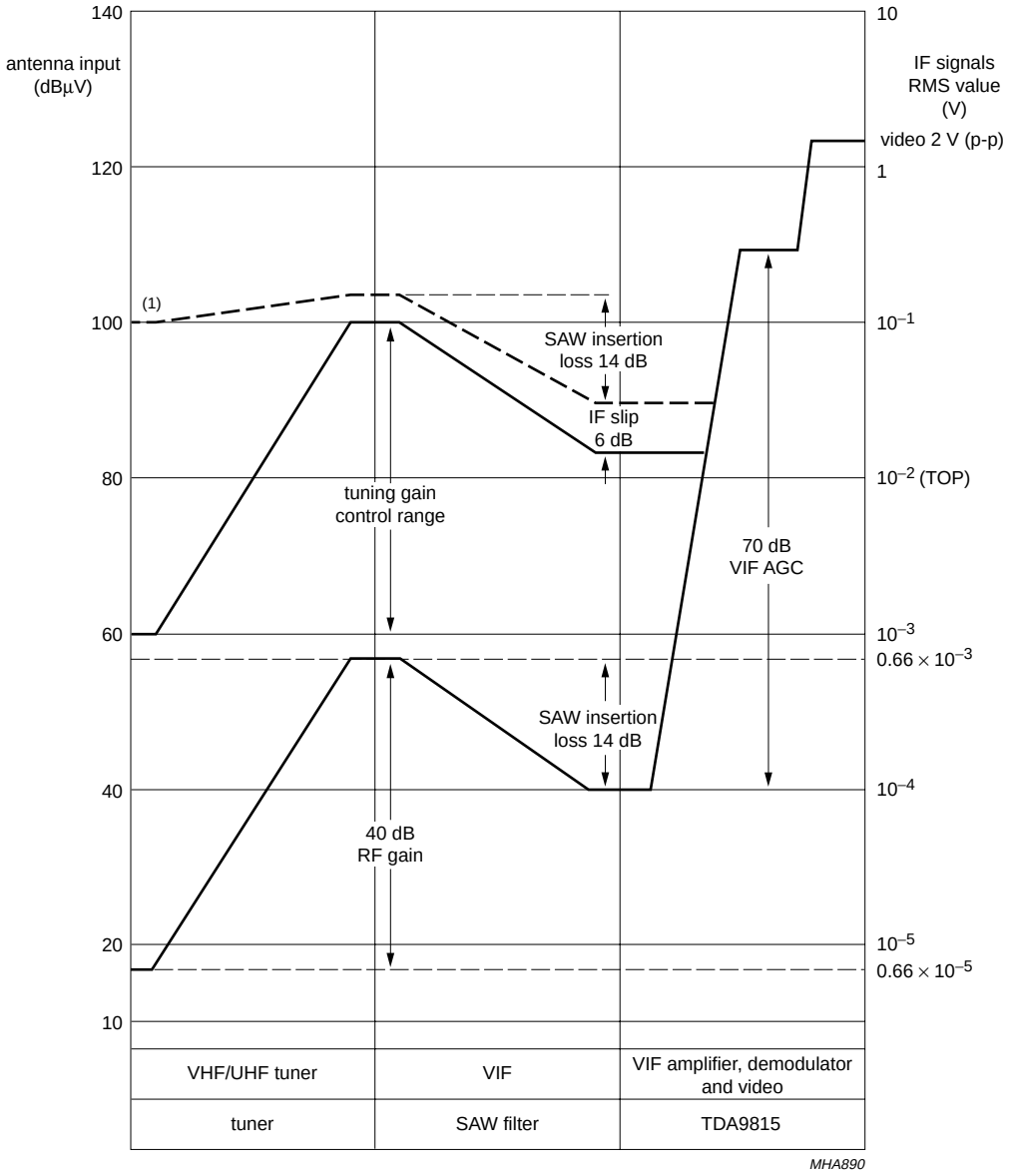


Fig.11 Ripple rejection condition.

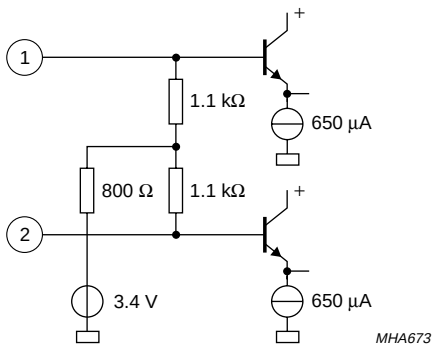
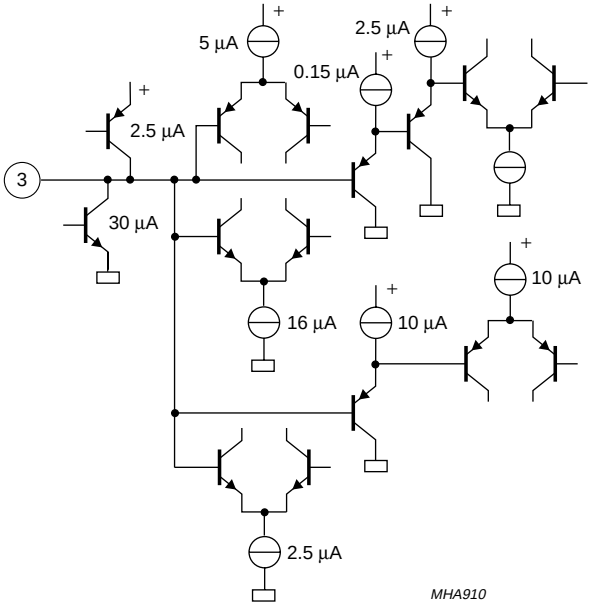
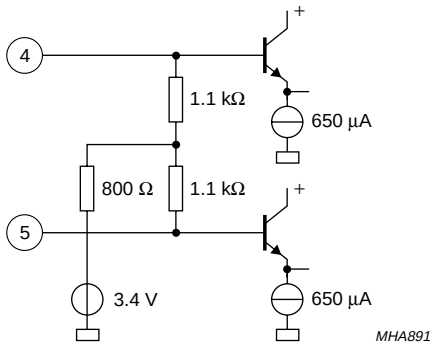


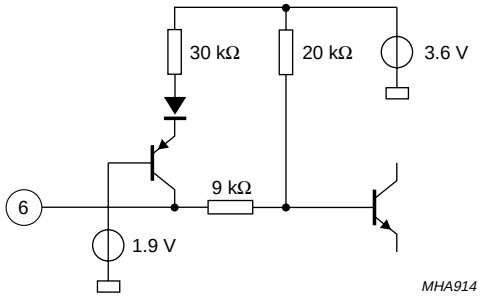
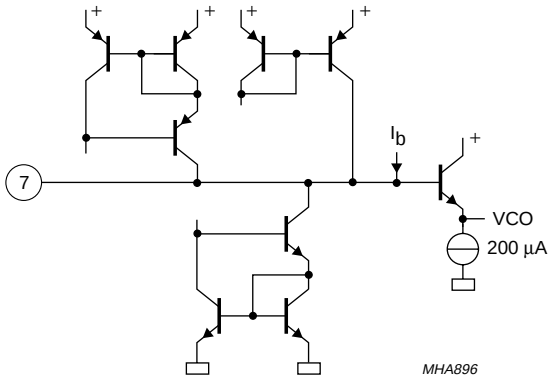
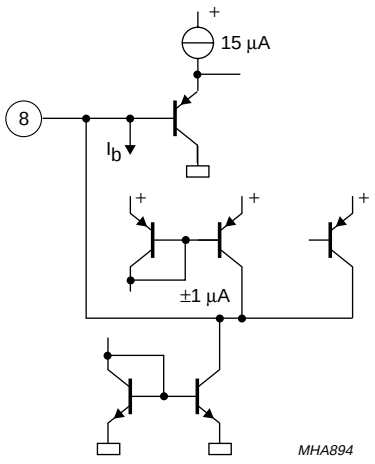
(1) Depends on TOP.

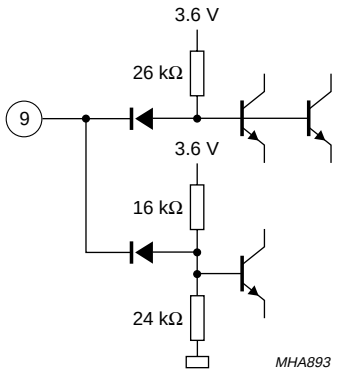
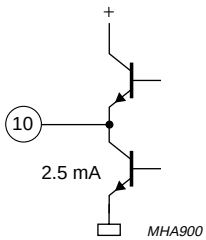
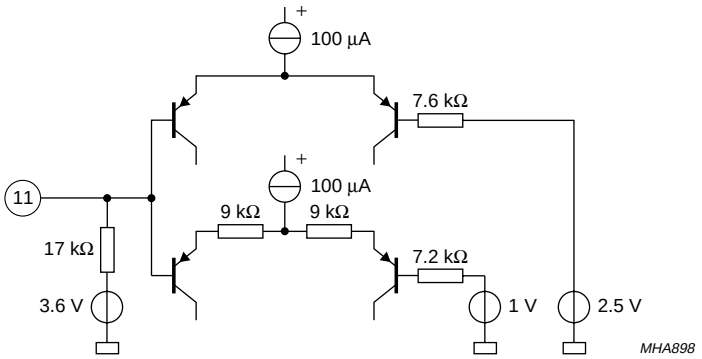
Fig.12 Front end level diagram.

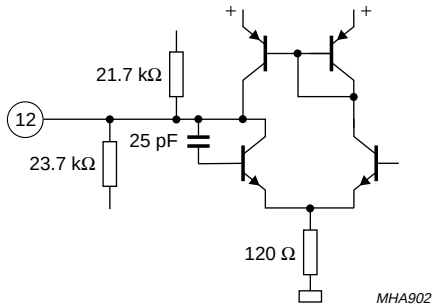
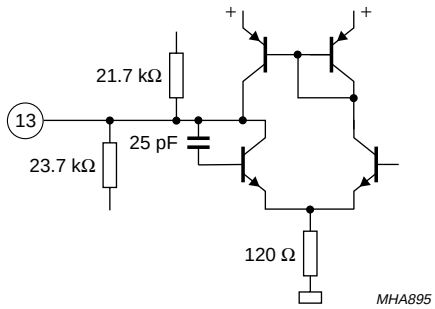
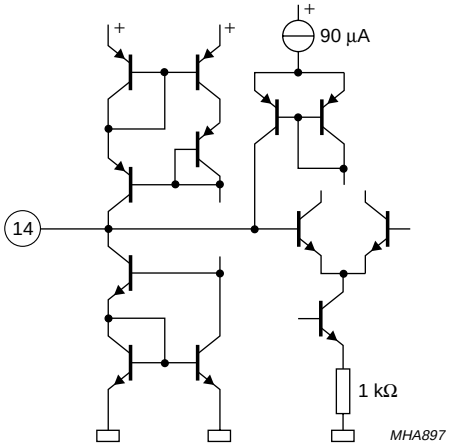
INTERNAL CIRCUITRY

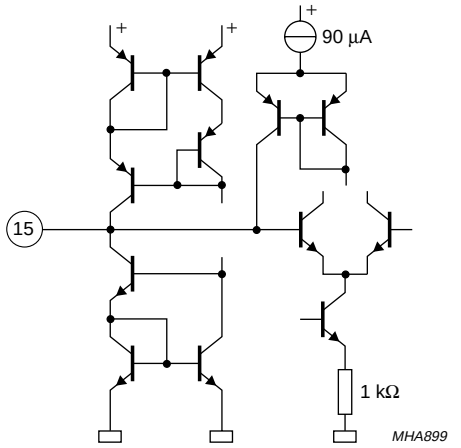
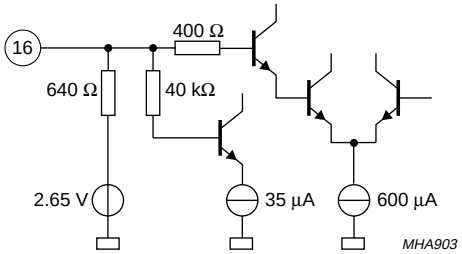
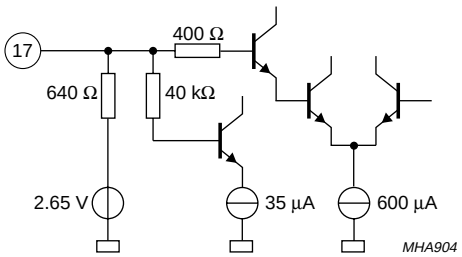
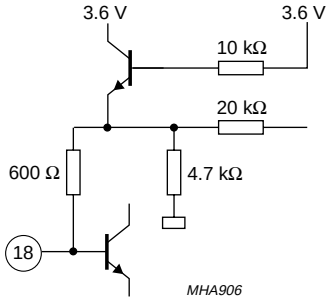
Table 3 Equivalent pin circuits and pin voltages

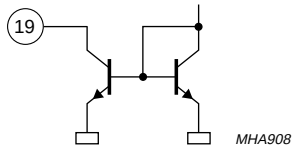
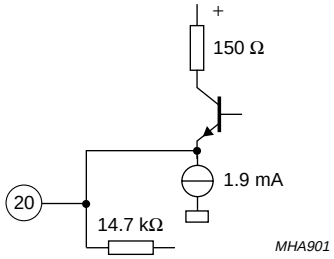
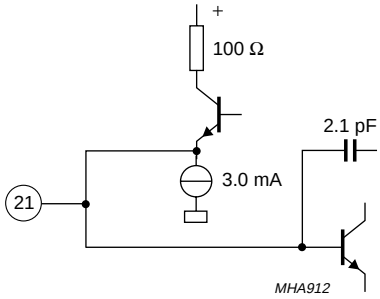
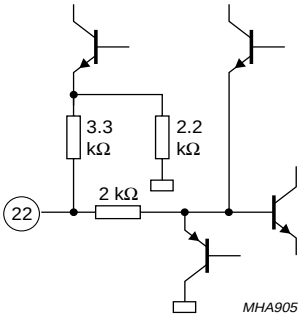
PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
1	$V_{i\ VIF1}$	3.4	
2	$V_{i\ VIF2}$	3.4	
3	$C_{BL/MAC}$	0 to 3.2	
4	$V_{i\ VIF3}$	3.4	
5	$V_{i\ VIF4}$	3.4	

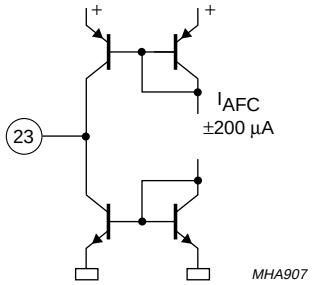
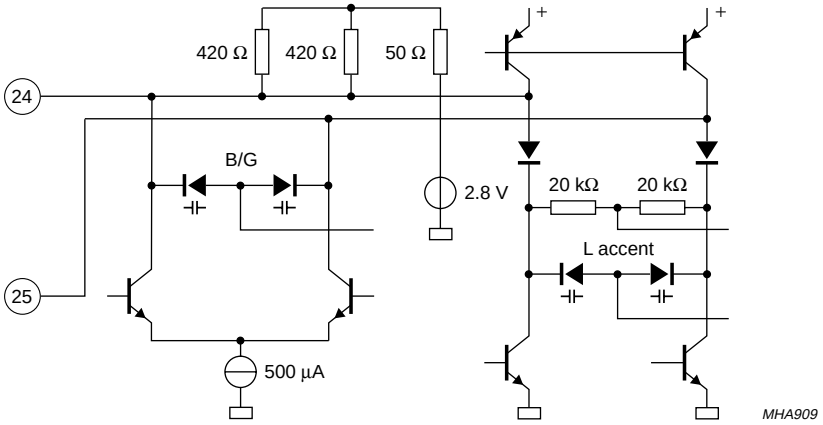
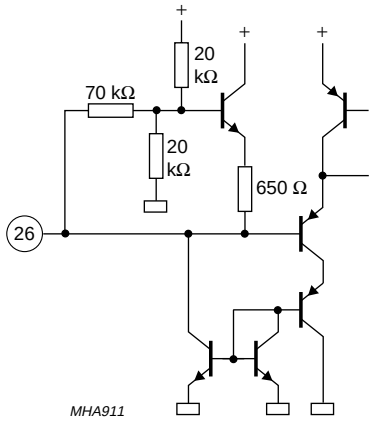
PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
6	TADJ	0 to 1.9	
7	T_{PLL}	1.5 to 4.0	
8	C_{SAGC}	1.5 to 4.0	

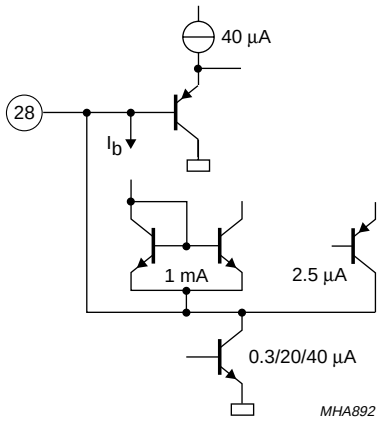
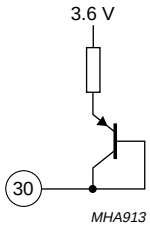
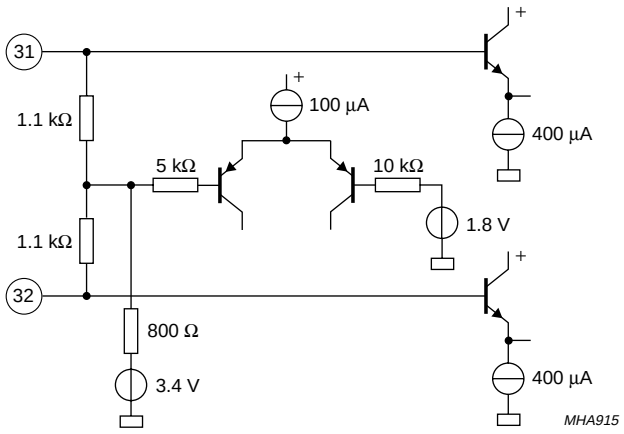
PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
9	STD	0 to V_P	
10	$V_{o\ CVBS}$	sync level: 1.35	
11	FMLSWI	0 to V_P	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
12	$V_{o\ AF1}$	2.3	
13	$V_{o\ AF2}$	2.3	
14	C_{DEC2}	1.2 to 3.0	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
15	C_{DEC1}	1.2 to 3.0	
16	$V_{i\ FM2}$	2.65	
17	$V_{i\ FM1}$	2.65	
18	$V_{i\ FM3}$	2.65	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
19	TAGC	0 to 13.2	
20	$V_{o\ QSS}$	2.0	
21	$V_{o(vid)}$	sync level: 1.5	
22	$V_{i(vid)}$	1.7	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
23	AFC	0.3 to V_P – 0.3	
24	VCO1	2.7	
25	VCO2	2.7	
26	C_{ref}	½V_P	
27	GND	0	

PIN NO.	PIN SYMBOL	DC VOLTAGE (V)	EQUIVALENT CIRCUIT (WITHOUT ESD PROTECTION CIRCUIT)
28	C_{VAGC}	1.5 to 4.0	
29	V_P	V_P	
30	INSWI	0 to V_P	
31	$V_{i\ SIF1}$	3.4	
32	$V_{i\ SIF2}$	3.4	

TEST AND APPLICATION INFORMATION

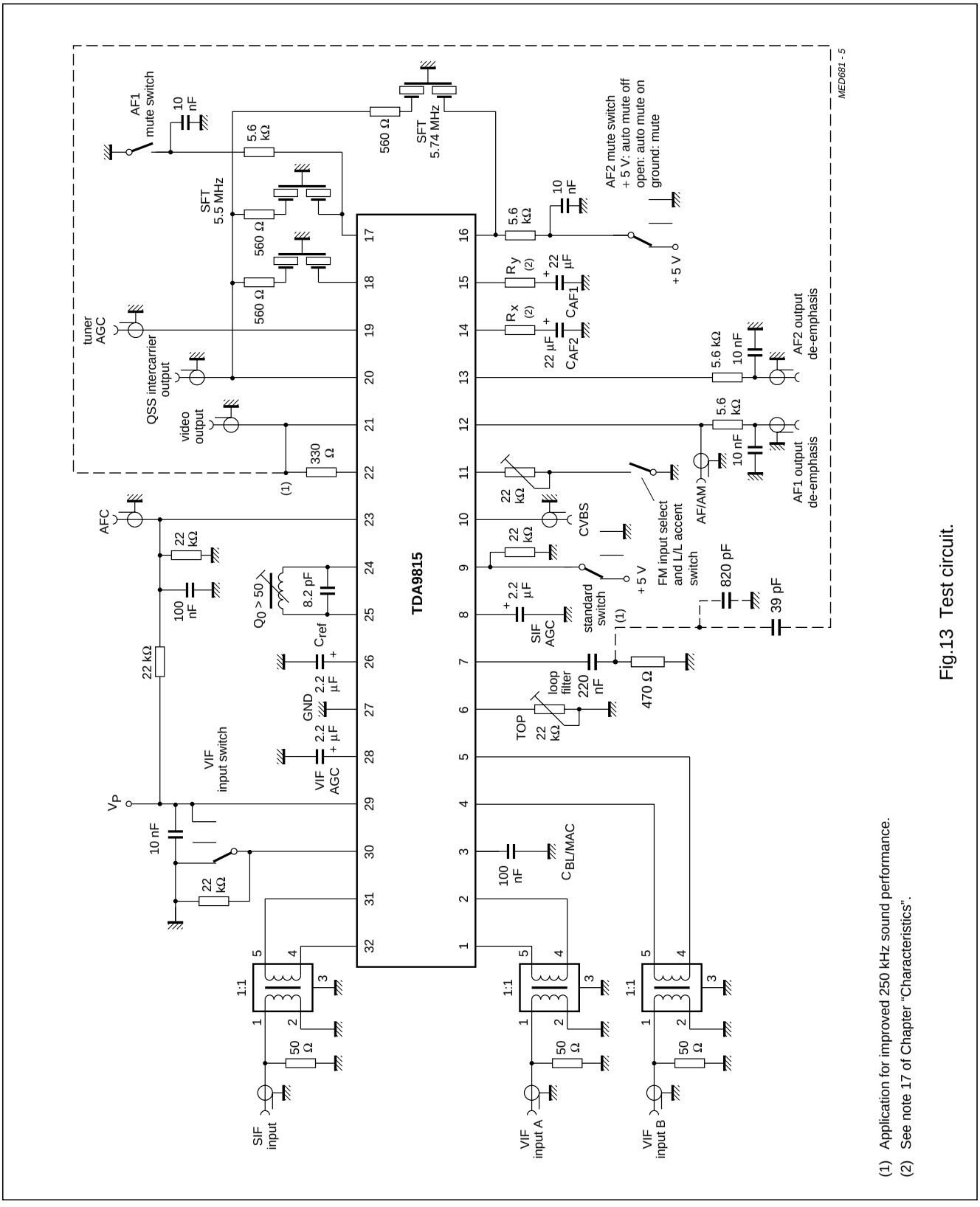


Fig.13 Test circuit.

(1) Application for improved 250 kHz sound performance.
(2) See note 17 of Chapter "Characteristics".

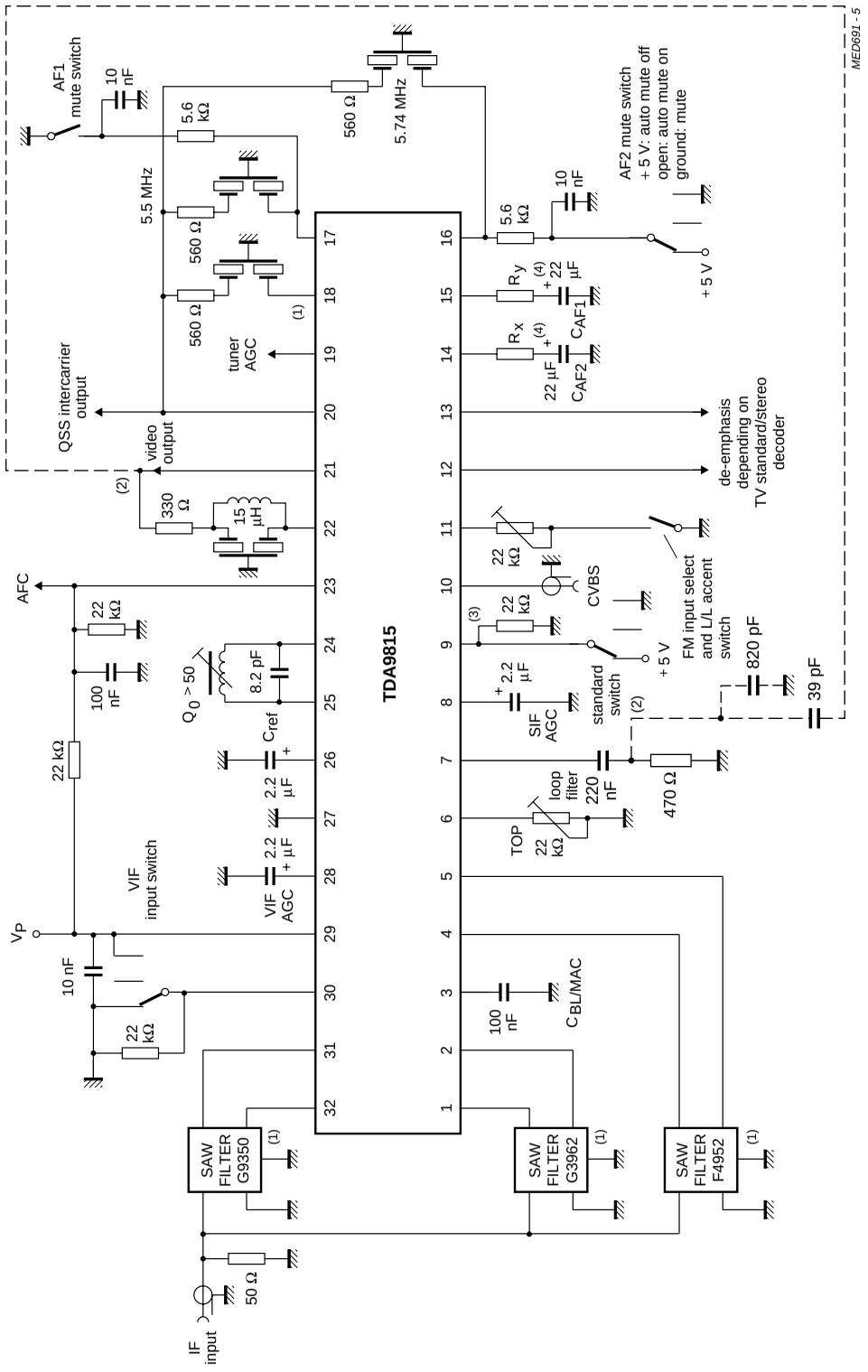
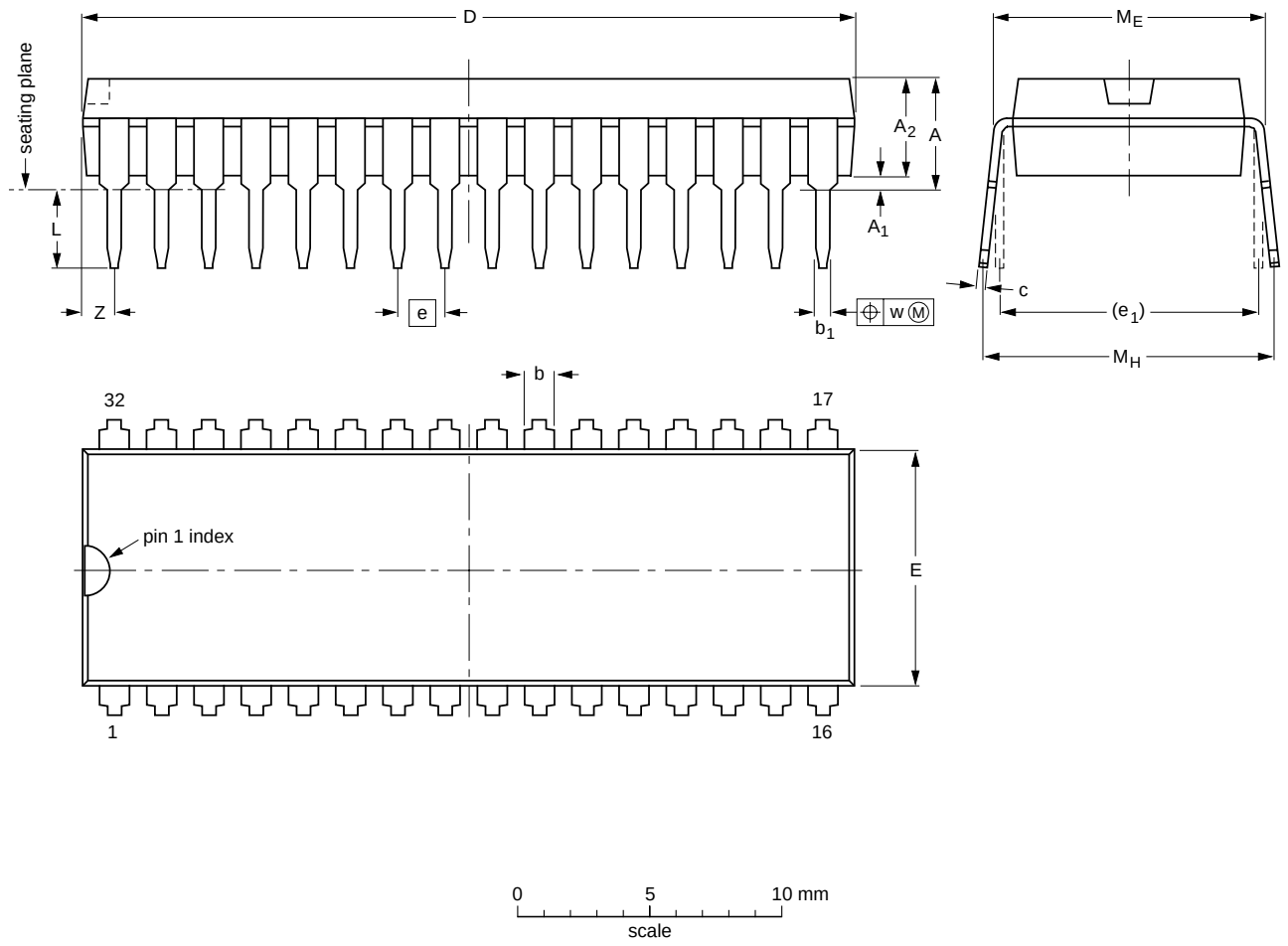


Fig.14 Application circuit.

(1) Depends on standard.
(2) Application for improved 250 kHz sound performance.
(3) Only required for external AGC mode.
(4) See note 17 of Chapter “Characteristics”.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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