INTEGRATED CIRCUITS

DATA SHEET

TDA9821
Dual channel TV FM intercarrier sound demodulator

Product specification
Supersedes data of March 1991
File under Integrated Circuits, IC02

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Philips Semiconductors

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FEATURES

- Two alignment-free PLL FM demodulators
- Automatic second sound carrier mute
- Mono and dual channel application
- Low power consumption
- Few external components required.

GENERAL DESCRIPTION

The TDA9821 is a monolithic, integrated, TV FM intercarrier sound demodulator for all FM standards. The circuit contains two separate FM demodulators using Phase Locked Loop (PLL) reference frequency generation. The circuit requires a minimum number of external components.

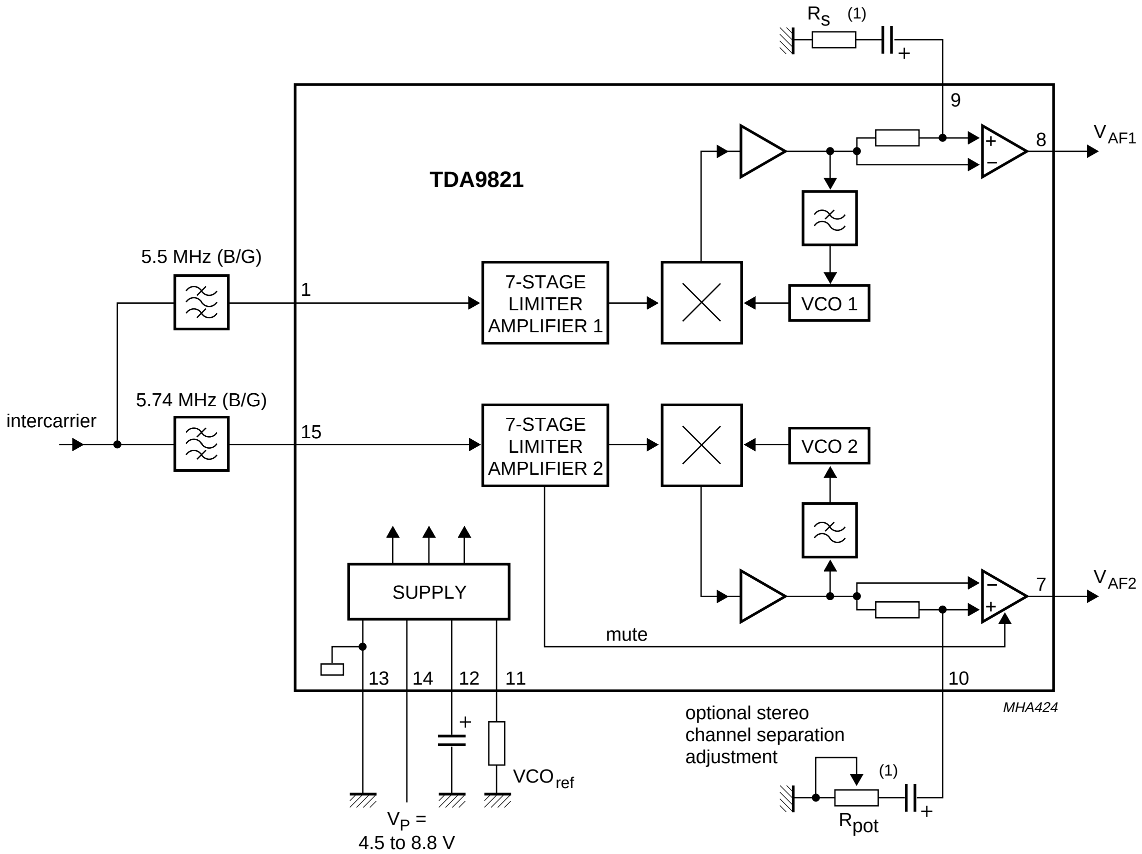
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 14)		4.5	5.0	8.8	V
I_P	supply current (pin 14)		23	30	37	mA
I_M	AC peak current (pins 7 and 8)		–	–	1.5	mA
$V_{i(rms)}$	input signal (RMS value)	$\frac{S+N}{N} = 40$ dB	–	150	250	μV
$V_{o(rms)}$	output signal (pins 7 and 8; RMS value)	$\Delta f_i = \pm 50$ kHz	0.4	0.5	0.6	V
$\frac{S+N}{N}$	signal plus noise-to-noise ratio (pins 7 and 8)	in accordance with *“CCIR 468-3”*	64	68	–	dB
$\alpha_{8/7}$	crosstalk attenuation	f = 50 to 12500 Hz	60	70	–	dB
RR	supply voltage ripple rejection (pins 7 and 8)	V_{RR} < 200 mV; f = 70 Hz	16	20	–	dB
T_{amb}	operating ambient temperature		0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9821	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

BLOCK DIAGRAM



(1) Resistor and potentiometer between capacitor and earth are inserted if adjustment of stereo channel separation is required.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$IN_{1(B/G)}$	1	intercarrier input 1 at 5.5 MHz
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
V_{AF2}	7	audio output voltage 2
V_{AF1}	8	audio output voltage 1
C_1	9	decoupling capacitor 1
C_2	10	decoupling capacitor 2
VCO_{ref}	11	VCO reference
C_{STAB}	12	supply voltage stabilization
GND	13	ground
V_P	14	supply voltage
$IN_{2(B/G)}$	15	intercarrier input 2
n.c.	16	not connected

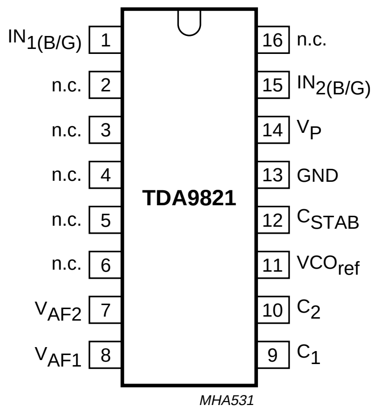


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The complete circuit consists of two separate channels, each consisting of a limiter-amplifier, FM demodulator and AF amplifier. Circuit operation is also described in Fig.1.

FM demodulators

The intercarrier signal is fed through external ceramic band-pass filters which are tuned to the sound carrier frequencies.

Each limiter-amplifier is AC-coupled into a FM demodulator. The integrated FM demodulator PLLs are alignment-free. The FM demodulator outputs are amplified to 500 mV (RMS value). High amplification and DC error signals of the PLLs, which are superimposed on the FM demodulator outputs, require DC decoupling at pins 9 and 10 of the AF amplifier inputs.

Stereo channel separation adjustment (optional)

Optimal stereo channel separation is achieved by adjusting V_{AF1} (pin 8) and V_{AF2} (pin 7) as follows:

1. V_{AF1} by a resistor in series with the DC decoupling capacitor at pin 9
2. V_{AF2} by a variable resistor in series with the DC decoupling capacitor on pin 10 to the same voltage as V_{AF1}.

Normally stereo channel separation is adjusted in the stereo decoder for the B/G standard.

Second sound carrier mute

The output of the second FM demodulator is muted when the signal level (signal and/or noise) at pin 15 is less than typically 0.5 mV (RMS value). This avoids an incorrect stereo or dual sound identification when a mono signal is transmitted. Therefore, with a mono transmission, there is no audio output at pin 7. When the signal level at pin 15 is greater than typically 1.0 mV (RMS value) mute is switched off.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 14)		–0.5	+9.0	V
V_i	input signal (pins 1 and 15)		–0.5	+5.0	V
t_s	short-circuit time (each pin except pins 13 and 14 to be tested; one at the time)		–	10	s
T_{stg}	storage temperature				
	device		–25	+125	°C
	device in packing		–25	+85	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		0	70	°C
V_{es}	electrostatic handling for all pins	note 1	–500	+500	V
		note 2	–4000	+4000	V

Notes

1. Equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	74	K/W

CHARACTERISTICS

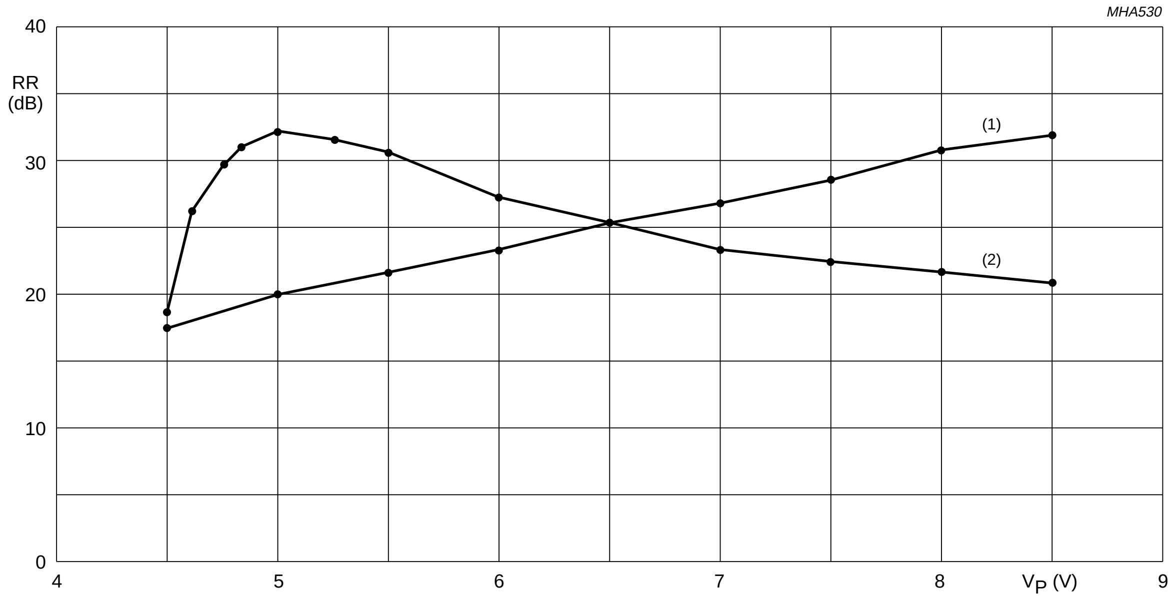
All voltages are measured to GND (pin 13); V_P = 5 V; T_{amb} = 25 °C; Δf_i = ±50 kHz; f_{mod} = 1 kHz; $V_{1,15}$ = 10 mV (RMS value); measurements taken in Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 14)						
V_P	supply voltage		4.5	5.0	8.8	V
I_P	supply current		23	30	37	mA
Limiter-amplifier 1						
V_1	DC input voltage		2.25	2.5	2.75	V
R_1	input resistance		480	600	720	Ω
$V_{1(rms)}$	input signal (RMS value)	$\frac{S+N}{N}$ = 40 dB	–	150	250	μV
	allowed input signal (RMS value)		200	–	–	mV
Limiter-amplifier 2						
V_{15}	DC input voltage		2.25	2.5	2.75	V
$V_{15(rms)}$	input signal (RMS value)	$\frac{S+N}{N}$ = 40 dB ; note 1	–	150	250	μV
	input signal for mute off (RMS value)		0.7	1.0	1.5	mV
	allowed input signal (RMS value)		200	–	–	mV
ΔV_{15}	mute hysteresis		8	12	16	dB
R_{15}	input resistance		480	600	720	Ω
PLL FM demodulators VCO1 and VCO2						
f_{VCO1}	free-running frequency	R_{11} = 27 kΩ	–	5.5	–	MHz
f_{VCO2}	free-running frequency	R_{11} = 27 kΩ	–	5.7	–	MHz
Δf_{fr}	negative/positive free-running frequency spread		–	–	10	%
$D/\Delta f_{fr}$	drift of free-running frequencies	T_{amb} = 0 to 70 °C	–	500	–	kHz
$\Delta f_{fr(shift)}$	shift of free-running frequencies	4.5 V < V_P < 8.8 V	–	200	–	kHz
$\Delta f_{fr(ar)}$	negative/positive adjustment range of free-running frequencies	R_{11} = 22 kΩ	1	–	–	MHz
R_{11}	adjustment resistance for free-running frequencies (pin 11)		15	–	29	kΩ
S	negative slope of free-running frequency adjustment	R_{11} = 22 kΩ	–	200	–	kHz/kΩ
Δf1	negative/positive catching range of PLLs		1.4	1.9	–	MHz
Δf2	negative/positive holding range of PLLs		2.0	3.0	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output amplifiers AF1 (pin 8) and AF2 (pin 7) and overall performance						
V_O	DC output voltage		1.8	2.1	2.5	V
$V_{o(rms)}$	output signal (RMS value)		0.4	0.5	0.6	V
		clipping level	1.2	–	–	V
I_M	AC peak current		–	–	1.5	mA
I_O	DC source current		–	–	2.0	mA
$\Delta V_o/V_o$	absolute drift of AF output signals	T_{amb} = 0 to 70 °C	–	0.7	–	dB
$\Delta V_{o1}/\Delta V_{o2}$	relative drift of AF output signals	T_{amb} = 0 to 70 °C	–	0.2	–	dB
$\Delta V_{AF(1-2)}$	negative/positive difference between output signals	50 µs de-emphasis	–	0.3	1.0	dB
R_o	output resistance		–	100	–	Ω
$\alpha_{cs(ar)}$	adjustment range of channel separation	R_s = 1.1 kΩ; R_{pot} = 2.2 kΩ	1.5	–	–	dB
THD	total harmonic distortion	50 µs de-emphasis				
		pin 8	–	0.1	0.3	%
		pin 7	–	0.25	0.5	%
α_{AM}	AM suppression of AF(1-2)	50 µs de-emphasis; m = 0.3; f_{AM} = 1 kHz	46	66	–	dB
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	50 µs de-emphasis; in accordance with *“CCIR 468-3”*	64	68	–	dB
AF_{resp}	LOW-level AF frequency response	$\Delta V_{AF(1-2)}$ = –3 dB	–	–	20	Hz
	HIGH-level AF frequency response		200	–	–	kHz
$AM_{res(rms)}$	residual sound carrier signal and harmonics (RMS value)		–	50	80	mV
$\alpha_{8/7}$	crosstalk attenuation between AF outputs	f = 50 to 12500 Hz	60	70	–	dB
RR	supply voltage ripple rejection	V_{RR} < 200 mV; f_r = 20 Hz to 200 kHz				
		V_P = 5 V	16	20	–	dB
		V_P = 8 V	24	28	–	dB
RR	supply voltage ripple rejection with improved application for V_P = 5 V	f_r = 20 Hz to 3 kHz; see Fig.3 and note 2				
		V_P = 4.5 V	18	24	–	dB
		V_P = 4.75 V	21	27	–	dB
		V_P = 5.0 V	24	30	–	dB
		V_P = 5.5 V	21	27	–	dB

Notes

1. The output signal at pin 7 can only be measured when mute is disabled. This is achieved by inserting a resistor of 2.7 kΩ between pin 15 and ground. In this event the input impedance is 490 Ω.
2. Improvement of ripple rejection is possible by connecting series RC between pin 11 and pin 14 (15 kΩ + 2.2 μF; see Fig.5) for a supply voltage of 4.5 to 5.5 V. The rejection of ripple frequencies up to 3 kHz is improved, but up to 200 kHz is worse; see Fig.3.



The curves are typical and valid for ripple frequencies between 50 Hz and 3 kHz.

Conditions: input signal: f = 5.5 MHz, 10 mV (RMS value); ripple on V_P = 100 mV (RMS value), f_r = 1 kHz; ripple rejection measurement: unweighted RMS.

(1) Without RC.

(2) With R = 15 kΩ and C = 2.2 μF.

Fig.3 Typical improvement.

INTERNAL CIRCUITRY

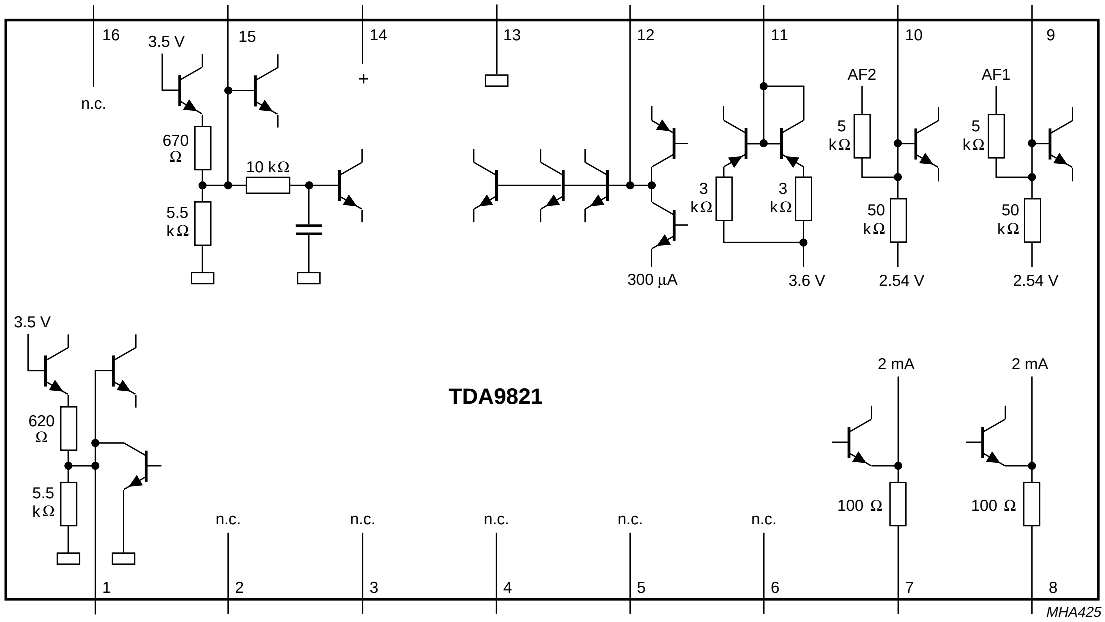
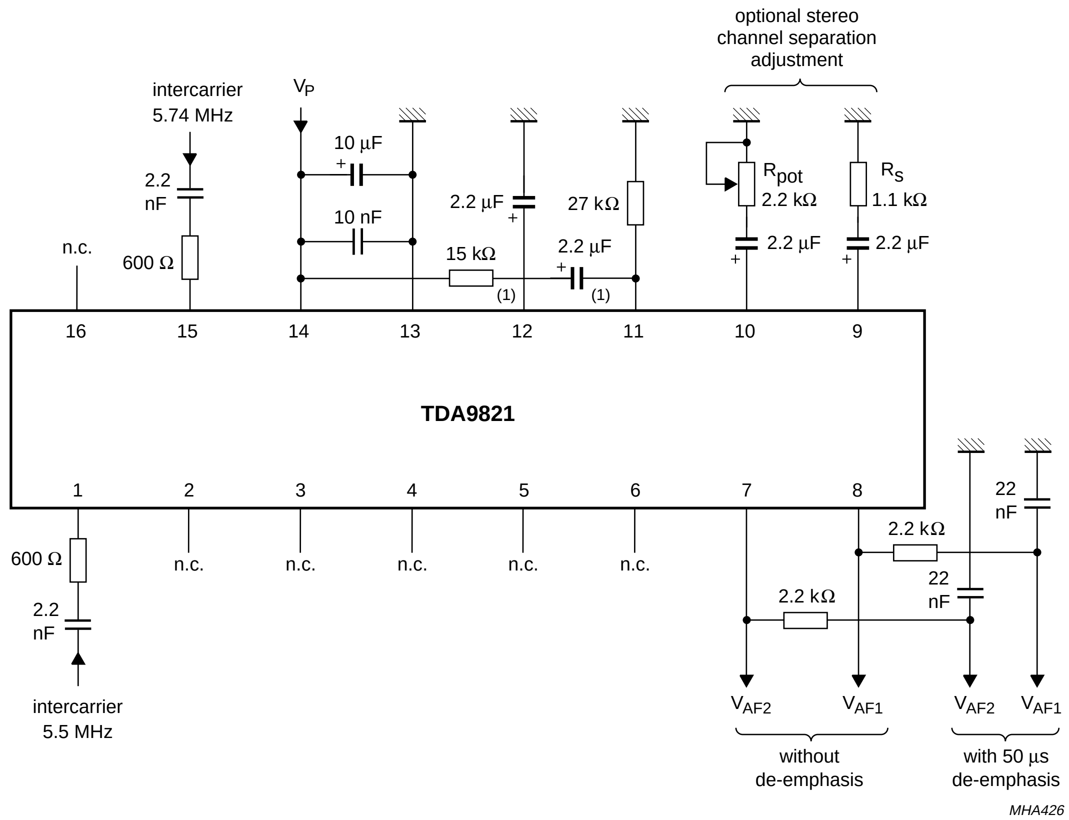


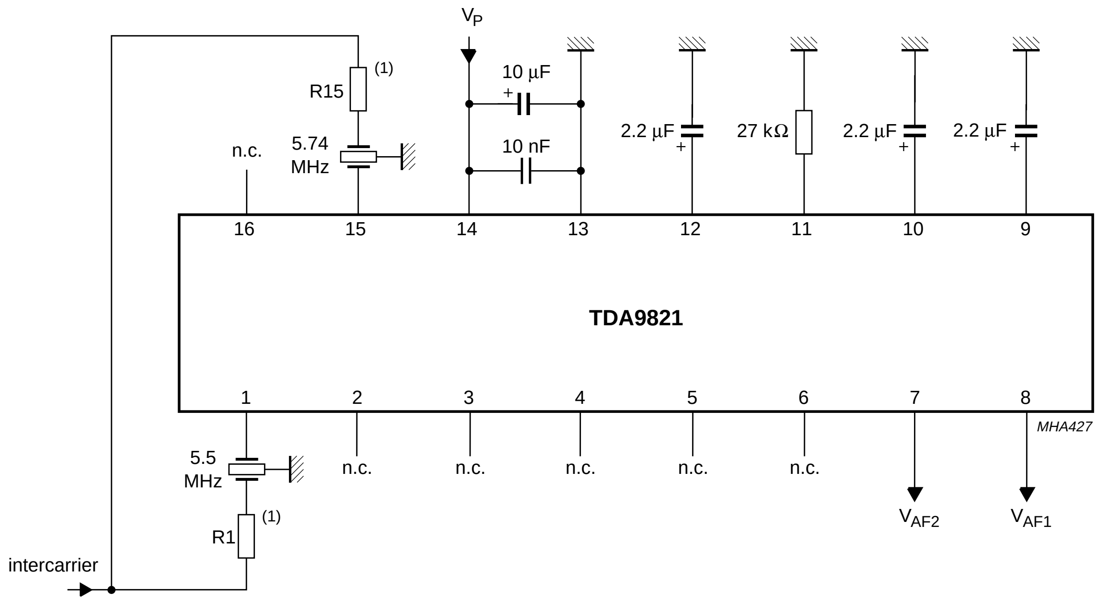
Fig.4 Internal circuitry.

TEST AND APPLICATION INFORMATION



(1) See note 2 of Chapter “Characteristics”.

Fig.5 Test circuit.

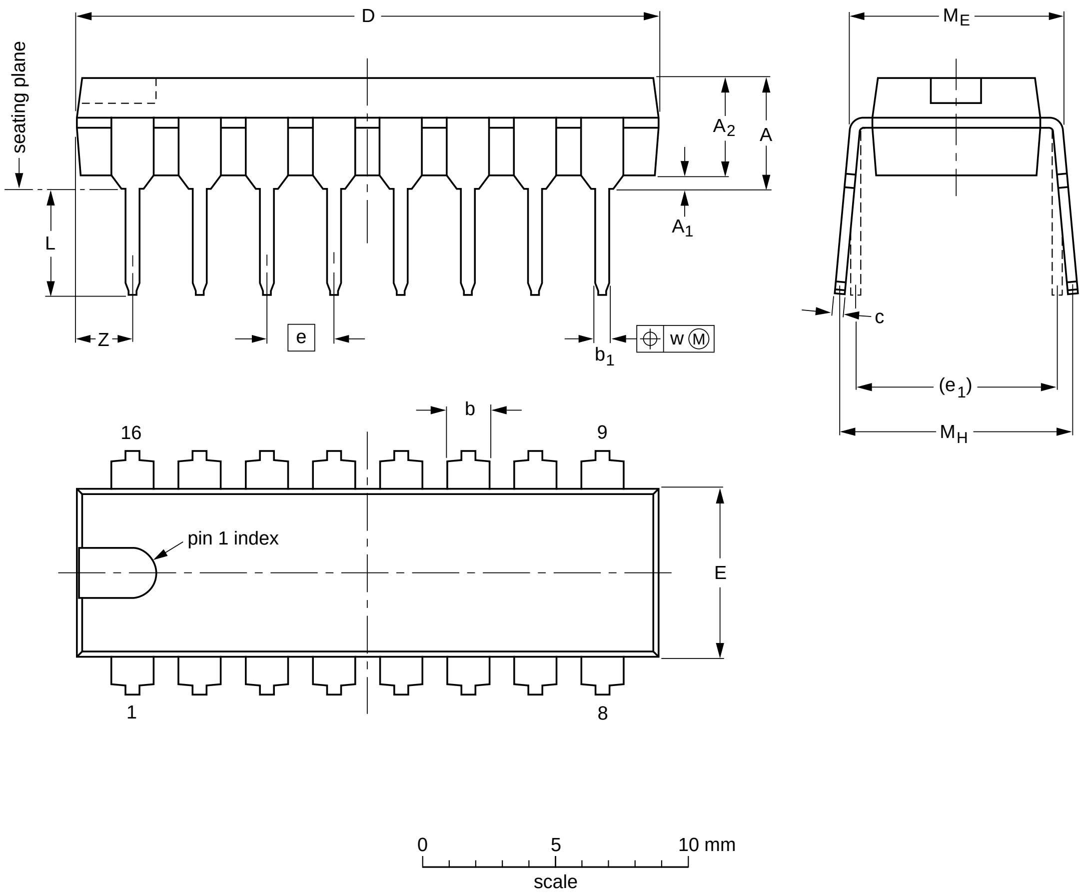


(1) Resistor value depends on filter.

Fig.6 Application circuit.

PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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