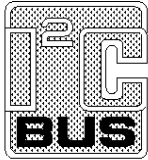


# DATA SHEET



## **TDA9874H** Digital TV sound demodulator/decoder

Preliminary specification  
File under Integrated Circuits, IC02

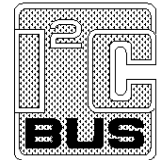
1998 Apr 27

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## Digital TV sound demodulator/decoder

TDA9874H

**1 FEATURES**

- SIF input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF AGC with 21 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- DQPSK demodulation for different standards, simultaneously with 1-channel FM demodulation
- NICAM decoding (B/G, I and L standard)
- Two-carrier multi-standard FM demodulation (B/G, D/K and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2\*) and satellite sound
- Adaptive de-emphasis for satellite
- Programmable identification (B/G, D/K and M standard) and different identification times
- Optional AM demodulation for system L, simultaneously with NICAM
- Monitor selection for FM/AM demodulator outputs and FM and NICAM signals
- Digital crossbar switch
- I<sup>2</sup>S serial audio output with matrix, level adjust and mute
- Dual audio Digital-to-Analog Converter (DAC) from digital crossbar switch to analog crossbar switch, bandwidth 15 kHz
- Analog crossbar switch with inputs for mono and stereo
- Output selection of mono, stereo, dual, dual A or dual B
- 20 kHz bandwidth for analog path
- Standby mode.

**2 GENERAL DESCRIPTION**

The TDA9874H is a single-chip Digital TV Sound Demodulator/Decoder (DTVSD1) for analog and digital multi-channel sound systems in TV/VCR sets and satellite receivers.

**2.1 Supported standards**

The multi-standard/multi-stereo capability of the TDA9874H is mainly of interest in Europe, but also in Hong Kong/PR China and South East Asia. This includes B/G, D/K, I, M and L standard. In other application areas there exist subsets of those standard combinations or only single standards are transmitted.

Standard M is transmitted in Europe by the American Forces Network with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

The AM sound of L/L' standard is normally demodulated in the 1st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9874H. A second possibility is to use the internal AM demodulator stage, giving limited performance.

Korea has a stereo sound system similar to Europe and is supported by the TDA9874H. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards and sound systems and their key parameters is given in Table 1.

The analog multi-channel systems are sometimes also named 2CS (2 carrier systems).

Digital TV sound demodulator/decoder

TDA9874H

2.1.1 ANALOG 2-CARRIER SYSTEMS

**Table 1** Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz)			MODULATION		BANDWIDTH/ DE-EMPHASIS (kHz/μs)
			NOM.	MAX.	OVER.	SC1	SC2	
M	mono	4.5	15	25	50	mono	–	15/75
M	A2+	4.5/4.724	15	25	50	$\frac{1}{2}(L + R)$	$\frac{1}{2}(L - R)$	15/75 (Korea)
B/G	A2	5.5/5.742	27	50	80	$\frac{1}{2}(L + R)$	R	15/50
I	mono	6.0	27	50	80	mono	–	15/50
D/K	A2	6.5/6.742	27	50	80	$\frac{1}{2}(L + R)$	R	15/50
D/K	A2*	6.5/6.258	27	50	80	$\frac{1}{2}(L + R)$	R	15/50

**Table 2** Identification for A2 systems

PARAMETER	A2; A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 × line frequency	55.0699 kHz = 3.5 × line frequency
Stereo identification frequency	117.5 Hz = $\frac{\text{line frequency}}{133}$	149.9 Hz = $\frac{\text{line frequency}}{105}$
Dual identification frequency	274.1 Hz = $\frac{\text{line frequency}}{57}$	276.0 Hz = $\frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 2-CARRIER SYSTEMS WITH NICAM

**Table 3** NICAM

STANDARD	SC1						SC2 (MHz) NICAM	DE-EMPHASIS	ROLL-OFF (%)	NICAM CODING
	FREQUENCY (MHz)	TYPE	MODULATION							
			INDEX (%)		DEVIATION (kHz)					
			NOM.	MAX.	NOM.	MAX.				
B/G	5.5	FM	–	–	27	50	5.85	J17	40	note 1
I	6.0	FM	–	–	27	50	6.552	J17	100	note 1
D/K	6.5	FM	–	–	27	50	5.85	J17	40	tbf
L	6.5	AM	54	100	–	–	5.85	J17	40	note 1

**Note**

1. See "EBU specification" or equivalent specification.

## Digital TV sound demodulator/decoder

TDA9874H

## 2.1.3 SATELLITE SYSTEMS

An important specification for satellite TV reception is the Astra specification. The TDA9874H is suited for the reception of Astra and other satellite signals, with sound carrier frequencies from 4 to 9.2 MHz.

Table 4 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH/ DE-EMPHASIS (kHz/ $\mu$ s)
Main	6.50 <sup>(1)</sup>	0.26	85	mono	15/50 <sup>(1)</sup>
Sub	7.02/7.20	0.15	50	m/st/d <sup>(2)</sup>	15/adaptive <sup>(3)</sup>
Sub	7.38/7.56	0.15	50	m/st/d <sup>(2)</sup>	15/adaptive <sup>(3)</sup>
Sub	7.74/7.92	0.15	50	m/st/d <sup>(2)</sup>	15/adaptive <sup>(3)</sup>
Sub	8.10/8.28	0.15	50	m/st/d <sup>(2)</sup>	15/adaptive <sup>(3)</sup>

## Notes

- For other satellite systems, frequencies of e.g. 5.80 MHz, 6.60 MHz or 6.65 MHz can also be received. A de-emphasis of 60  $\mu$ s or in accordance with J17 is available.
- m/st/d = mono or stereo or dual language sound.
- Adaptive de-emphasis = compatible to transmitter specification.

## 3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9874H	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

Digital TV sound demodulator/decoder

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4 BLOCK DIAGRAM

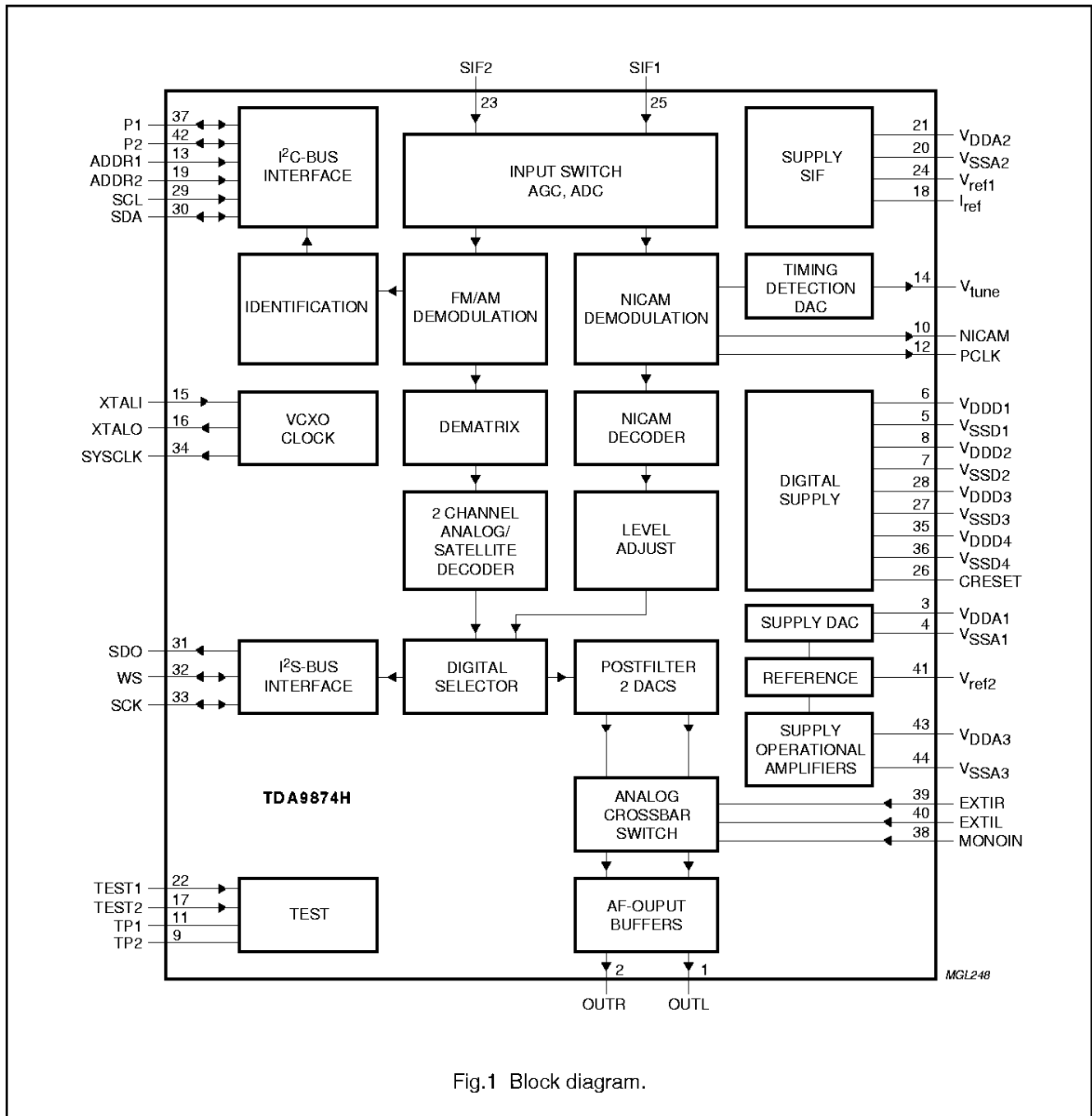


Fig.1 Block diagram.

Digital TV sound demodulator/decoder

TDA9874H

5 PINNING INFORMATION

5.1 Pinning

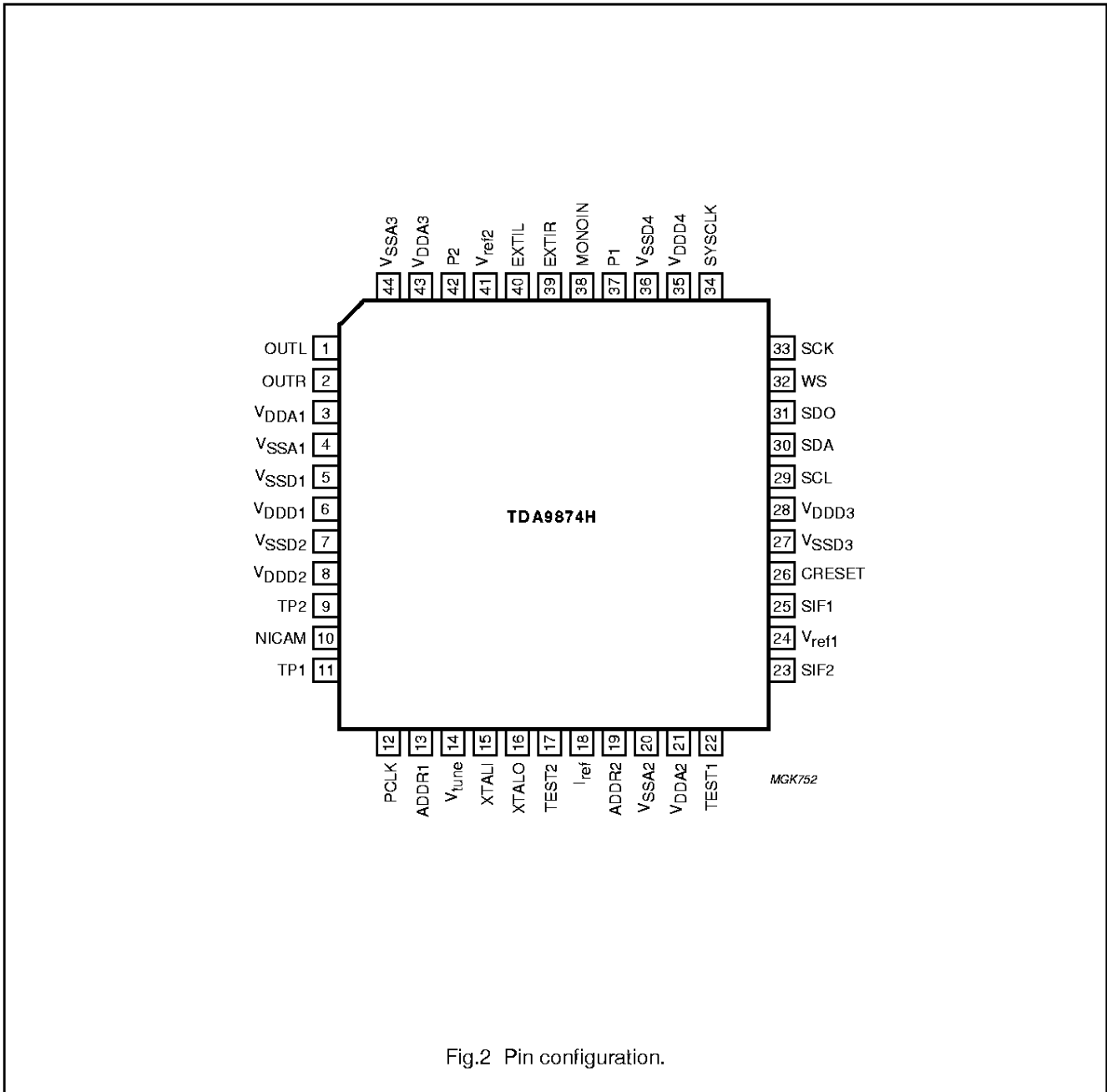


Fig.2 Pin configuration.

## Digital TV sound demodulator/decoder

TDA9874H

## 5.2 Pin description

Table 5 SOT205-1 package

SYMBOL	PIN	DESCRIPTION
OUTL	1	analog output left
OUTR	2	analog output right
V <sub>DDA1</sub>	3	analog supply voltage 1; DAC circuitry
V <sub>SSA1</sub>	4	analog ground supply 1; DAC circuitry
V <sub>SSD1</sub>	5	digital ground supply 1; DAC circuitry
V <sub>DDD1</sub>	6	digital supply voltage 1; DAC circuitry
V <sub>SSD2</sub>	7	digital ground supply 2; DSP part
V <sub>DDD2</sub>	8	digital supply voltage 2; DSP part
TP2	9	additional test pin 2; connected to V <sub>SSD</sub> for normal operation
NICAM	10	serial NICAM data output at 728 kHz
TP1	11	additional test pin 1; connected to V <sub>SSD</sub> for normal operation
PCLK	12	NICAM clock output at 728 kHz
ADDR1	13	first I <sup>2</sup> C-bus slave address modifier
V <sub>tune</sub>	14	tuning voltage output for crystal oscillator
XTALI	15	crystal oscillator input
XTALO	16	crystal oscillator output
TEST2	17	test pin 2; connected to V <sub>SSD</sub> for normal operation
I <sub>ref</sub>	18	resistor for reference current generation; front end circuitry
ADDR2	19	second I <sup>2</sup> C-bus slave address modifier
V <sub>SSA2</sub>	20	analog ground supply 2; analog front end circuitry
V <sub>DDA2</sub>	21	analog supply voltage 2; analog front end circuitry
TEST1	22	test pin 1; connected to V <sub>SSD</sub> for normal operation
SIF2	23	sound IF input 2
V <sub>ref1</sub>	24	reference voltage; analog front end circuitry
SIF1	25	sound IF input 1
CRESET	26	capacitor for power-on reset
V <sub>SSD3</sub>	27	digital ground supply 3; front end circuitry
V <sub>DDD3</sub>	28	digital supply voltage 3; front end circuitry
SCL	29	I <sup>2</sup> C-bus clock input
SDA	30	I <sup>2</sup> C-bus data input/output
SDO	31	I <sup>2</sup> S-bus serial data output



## Digital TV sound demodulator/decoder

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<b>SYMBOL</b>	<b>PIN</b>	<b>DESCRIPTION</b>
WS	32	I <sup>2</sup> S-bus word select input/output
SCK	33	I <sup>2</sup> S-bus clock input/output
SYSCLK	34	system clock output
V <sub>DDD4</sub>	35	digital supply voltage 4; demodulator circuitry
V <sub>SSD4</sub>	36	digital ground supply 4; demodulator circuitry
P1	37	first general purpose I/O pin
MONOIN	38	analog mono input
EXTIR	39	external audio input right channel
EXTIL	40	external audio input left channel
V <sub>ref2</sub>	41	analog reference voltage DAC and operational amplifiers
P2	42	second general purpose I/O pin
V <sub>DDA3</sub>	43	analog supply voltage 3; operational amplifiers
V <sub>SSA3</sub>	44	analog ground supply 3; operational amplifiers

## Digital TV sound demodulator/decoder

## TDA9874H

**6 FUNCTIONAL DESCRIPTION****6.1 Description of the demodulator and decoder section****6.1.1 SIF INPUT**

Two input pins are provided. SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC and then digitized by an 8-bit ADC running at 24.576 MHz.

**6.1.2 AGC**

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads, and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen from a table.

The AGC can be controlled via the I<sup>2</sup>C-bus. Details can be found in Sections 7.3.1, 7.3.2 and 7.4.6.

**6.1.3 MIXER**

The digitized input signal is passed on to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I<sup>2</sup>C-bus (see Sections 7.3.4 and 7.3.5). When receiving NICAM programs, a feedback signal is added to the control word of the second carrier mixer to establish a carrier-frequency loop.

**6.1.4 FM AND AM DEMODULATION**

An FM or AM input signal is passed through a band-limiting filter onto a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

**6.1.5 FM DECODING**

A two-carrier stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

**6.1.6 FM IDENTIFICATION**

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot and narrow-band detection of the identification frequencies. The result is available via the I<sup>2</sup>C-bus interface. A selection can be made via the I<sup>2</sup>C-bus for B/G, D/K and M standard, and for three different time constants that represent different trade-offs between speed and reliability of identification.

**6.1.7 NICAM DEMODULATION**

The NICAM signal is transmitted in a DQPSK code at a bit rate of 728 kbits/s. The NICAM demodulator performs DQPSK demodulation and passes the resulting bitstream and clock signal to the NICAM decoder and, for evaluation purposes, to pins.

A timing loop controls the frequency of the crystal oscillator to lock the sampling instants to the symbol timing of the NICAM data. The polarity of the control signal is selectable to support applications, in which external circuitry is used to boost the tuning voltage of the oscillator.

**6.1.8 NICAM DECODING**

The device performs all decoding functions in accordance with the "EBU NICAM 728 specification". After locking to the frame alignment word, the data are descrambled by application of the defined pseudo-random binary sequence, and the device synchronizes to the periodic frame flag bit C0.

The status of the NICAM decoder can be read-out from the NICAM Status Register by the user (see Section 7.4.2). The OSB bit indicates that the decoder has locked to the NICAM data. The VDSP bit indicates that the decoder has locked to the NICAM data and that the data is valid sound data. The C4 bit indicates that the sound conveyed by the FM mono channel is identical to the sound conveyed by the NICAM channel. The error byte contains the number of sound sample errors, resulting from parity checking, that occurred in the past 128 ms period. The Bit Error Rate (BER) is approximately 0.0000174 times the contents of the error byte.

$$\text{BER} = \frac{\text{bit errors}}{\text{total bits}} \approx \text{error byte} \times 1.74 \times 10^{-5}$$

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## Digital TV sound demodulator/decoder

## TDA9874H

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### 6.1.9 NICAM AUTO-MUTE

This function is enabled by setting bit **AMUTE LOW** (see Section 7.3.11). Upper and lower error limits may be defined by writing appropriate values to two registers in the I<sup>2</sup>C-bus section (see Sections 7.3.13 and 7.3.14). When the number of errors in a 128 ms period exceeds the upper error limit, the auto-mute function will switch the output sound from NICAM to whatever sound is on the first sound carrier (FM or AM) or to the analog mono input. When the error count is smaller than the lower error limit, the NICAM sound is restored.

The auto-mute function can be disabled by setting bit **AMUTE HIGH**. In this case clicks become audible, when the error count increases. The user will hear a signal of degrading quality.

A decision to enable/disable the auto-muting is taken by the microprocessor based on an interpretation of the application control bits **C1**, **C2**, **C3** and **C4**, and possibly any additional strategy implemented by the setmaker in the microcontroller software.

When the AM sound in NICAM L systems is demodulated in the 1st sound IF and the audio signal connected to the mono input of the TDA9874H, the controlling microprocessor has to take care of switching from NICAM reception to mono input, if auto-muting is desired. This could be achieved by setting the **AMSEL** bit **HIGH** additionally to **AMUTE** bit **LOW** (see also Section 7.3.11).

### 6.1.10 CRYSTAL OSCILLATOR

A circuit diagram of the external components of the voltage-controlled crystal oscillator is shown in Fig.7 in Chapter 9.

### 6.1.11 TEST PINS

All test pins are active **HIGH**. In normal operation of the device they can be left open-circuit, as they have internal pull-down resistors. Test functions are for manufacturing tests only and are not available to customers.

## Digital TV sound demodulator/decoder

TDA9874H

### 6.2 Description of the DSP

#### 6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch are equipped with a level adjust facility to change the signal level in a range of  $\pm 15$  dB. Adjusting the signal level is intended to compensate for the different modulation parameters of the various TV standards. It is recommended to scale all input channels to be 15 dB below full-scale ( $-15$  dB (FS)) under nominal conditions. This will create sufficient headroom to cope with overmodulation and avoids changes of the volume impression when switching from FM to NICAM or vice versa.

#### 6.2.2 NICAM PATH

The NICAM path has a switchable J17 de-emphasis.

#### 6.2.3 NICAM AUTO-MUTE

If NICAM is received, the AUTO-MUTE is enabled and the signal quality becomes poor, the digital crossbar switches automatically to FM, Channel 1 or the analog mono input, as selected by bit AMSEL. This automatic switching depends on the NICAM bit error rate. The auto-mute function can be disabled via the I<sup>2</sup>C-bus.

#### 6.2.4 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator that may occur due to carrier frequency offsets and supplies the FM monitor function with DC values, e.g. for the purpose of microprocessor controlled carrier search or fine-tuning functions.

An adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

The de-emphasis stage offers a choice of settings for the supported TV standards.

The 2 channel decoder performs the dematrixing of  $\frac{1}{2}(L + R)$  and R to L and R signals, of  $\frac{1}{2}(L + R)$  and  $\frac{1}{2}(L - R)$  to L and R signals or of Channel 1 and Channel 2 to L and R signals, as demanded by the different TV standards or user preferences.

#### 6.2.5 FM MONITOR

This function provides data words from the FM demodulator outputs and FM and NICAM signals for external use, like carrier search or fine tuning. Source selection and data read-out are performed via the I<sup>2</sup>C-bus.

#### 6.2.6 DIGITAL CROSSBAR SWITCH

Input channels come from the FM and NICAM paths, while output channels comprise I<sup>2</sup>S and the audio DACs to the analog crossbar switch. Note that there is no connection from the external analog audio inputs to the digital crossbar switch.

#### 6.2.7 DIGITAL AUDIO OUTPUT

The digital audio output interface comprises an I<sup>2</sup>S output port and a system clock output. The I<sup>2</sup>S port is equipped with a level adjust facility that can change the signal level in a  $\pm 15$  dB range in 1 dB steps. Muting is possible, too, and outputs can be disabled to improve EMC performance.

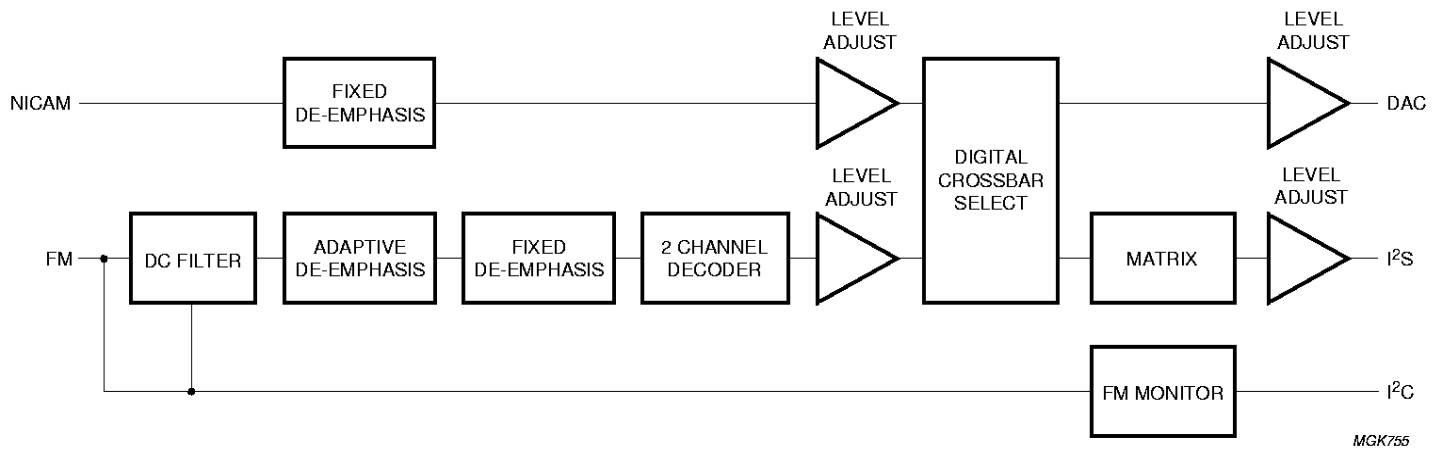
The I<sup>2</sup>S-bus output matrix provides the functions of forced mono, stereo, channel swap, Channel 1 or Channel 2.

#### 6.2.8 CHANNEL TO THE ANALOG CROSSBAR PATH

A level adjust function is provided with control positions 0 dB, +3 dB, +6 dB and +9 dB in combination with the audio DACs.

#### 6.2.9 GENERAL

The level adjust functions can provide signal gain at multiple locations. Great care has to be taken when using gain with large input signals, e.g., due to overmodulation, in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full-scale, i.e.,  $-15$  dB (FS).



MGK755

Fig.3 DSP data flow diagram.

Digital TV sound demodulator/decoder

TDA9874H

6.3 Description of the analog audio section

6.3.1 ANALOG CROSSBAR SWITCH AND ANALOG MATRIX

The TDA9874H has one external analog stereo input, one mono input and one two-channel output port. Analog source selector switches are employed to provide the desired analog signal routing capability, which is done by the analog crossbar switch section.

The basic signal routing philosophy of the TDA9874H is that each switch handles two signal channels at the same time, e.g. Left and Right, language A and B, directly at the source. For an overview of the signal flow see Fig.5.

Each source selector switch is followed by an analog matrix to perform further selection tasks, like putting a signal from one input channel, say, language A, to both output channels or for swapping left and right channel.

All switches and matrices are controlled via the I<sup>2</sup>C-bus.

6.3.2 EXTERNAL AND MONO INPUTS

The external and mono inputs accept signal levels of up to 1.4 V (RMS). By adding external series resistors to provide a suitable attenuation, the external input could be used as a SCART input. Whenever the external or mono input is selected, the output of the DAC is muted to improve the crosstalk performance.

6.3.3 DUAL AUDIO DAC

The TDA9874H comprises a two-channel audio DAC for feeding signals from the DSP section to the analog crossbar switch. These DACs have a resolution of 15 bits and employ four-fold oversampling and noise shaping.

6.3.4 AUDIO OUTPUT BUFFERS

The output buffers provide 0 dB of gain and offer a muting possibility. The post filter capacitors of the audio DACs are connected to the buffer outputs.

6.3.5 STANDBY MODE

The Standby mode (see Section 7.3.2) disables most functions and reduces power dissipation of the TDA9874H, but provides no other functionality.

Internal registers may lose their information in Standby mode. Therefore, the device needs to be initialized on returning to normal operation. This can be accomplished in the same way as after a power-on reset.

Table 6 Analog matrix functions

MODE	MATRIX OUTPUT	
	L OUTPUT	R OUTPUT
1	L input	R input
2	R input	L input
3	L input	L input
4	R input	R input

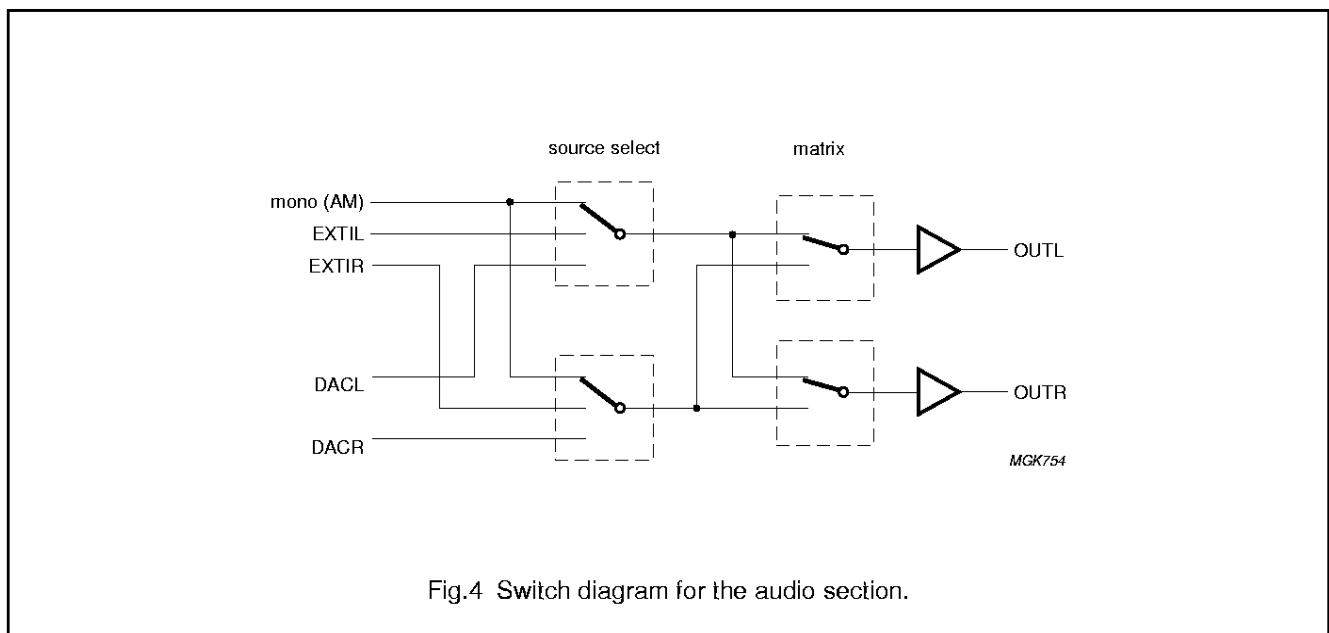


Fig.4 Switch diagram for the audio section.

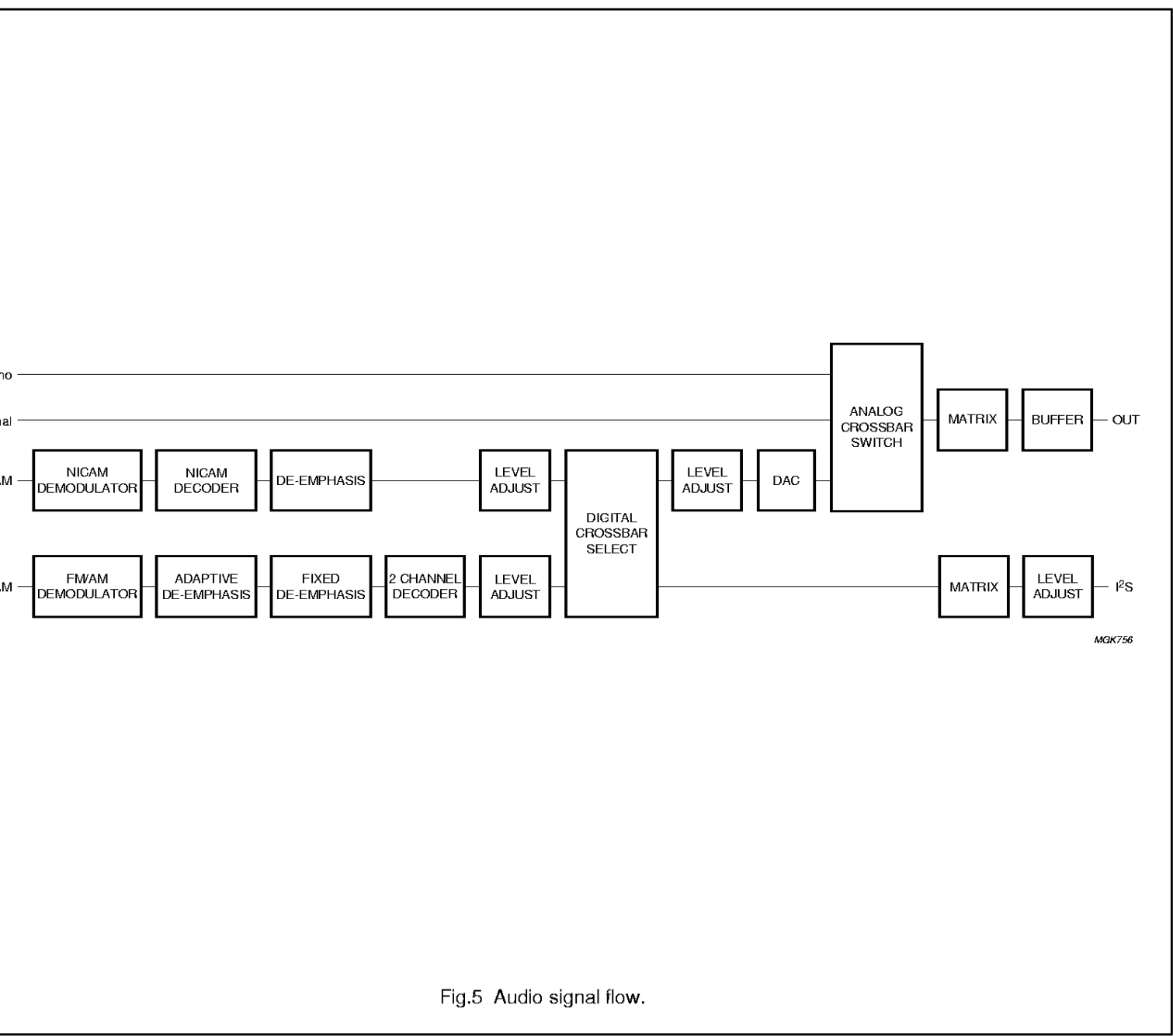


Fig.5 Audio signal flow.

Digital TV sound demodulator/decoder

TDA9874H

**7 I<sup>2</sup>C-BUS CONTROL**

**7.1 Introduction**

The TDA9874H is controlled only via the I<sup>2</sup>C-bus. Control is exercised by writing data to one or more internal registers. Status information can be read from an array of registers to let the controlling microprocessor determine whether any action is required.

The device has an I<sup>2</sup>C-bus slave transceiver in accordance with the fast-mode specification with a maximum speed of 400 kbits/s. Information about the I<sup>2</sup>C-bus can be found in brochure *"I<sup>2</sup>C-bus and how to use it"* (order number 9398 393 40011). To avoid conflicts in a real application with other ICs providing similar or complementing functions, there are four possible slave addresses available, which can be selected by pins ADDR1 and ADDR2 (see Table 7).

**Table 7** Possible slave addresses

ADDR2	ADDR1	SLAVE ADDRESS						
		A6	A5	A4	A3	A2	A1	A0
0	0	1	0	1	1	0	0	0
0	1	1	0	1	1	0	0	1
1	0	1	0	1	1	0	1	0
1	1	1	0	1	1	0	1	1

The I<sup>2</sup>C-bus interface remains operational in the Standby mode of the TDA9874H to allow the device to be reactivated via the I<sup>2</sup>C-bus.

The device will not respond to a 'general call' on the I<sup>2</sup>C-bus, i.e. when a slave address of 0000000 is sent by a master.

**7.2 Power-up state**

At power-up the device is in the following state:

- All outputs muted
- No sound carrier frequency loaded
- General purpose I/O pins ready for input (HIGH)
- Input SIF1 selected with:
  - AGC on
  - Small hysteresis.
- Demodulators for both sound carriers set to FM with:
  - Identification for B/G, D/K, identification mode 'slow'
  - Level adjust set to 0 dB
  - De-emphasis 50 μs
  - Dematrix set to mono
  - Adaptive de-emphasis on.
- OUTL and OUTR set to mono and connected to DAC
- Digital audio interface all outputs off
- Monitor set to carrier 1 DC output.

After power-up a device initialization has to be performed via the I<sup>2</sup>C-bus to put the TDA9874H into the proper mode of operation, in accordance with the desired TV standard, etc. This can be done by writing to all registers with a single I<sup>2</sup>C-bus transmission (like a refresh operation) or by writing selectively only to those registers, the contents of which need to be changed with regard to the power-up state.



Digital TV sound demodulator/decoder

TDA9874H

**7.3 Slave receiver mode**

As a slave receiver, the TDA9874H provides 24 registers for storing commands and data. Each register is accessed via a so-called subaddress. A subaddress can be thought of as a pointer to an internal memory location.

Detailed descriptions of the slave receiver registers are given in Sections 7.3.1 to 7.3.20.

**Table 8** I<sup>2</sup>C-bus; SLAVE ADDRESS/SUBADDRESS/DATA format

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA	A/NA	P
---	---------------	---	---	------------	---	------	------	---

**Table 9** Explanation of Table 8

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
A	acknowledge
SUBADDRESS	address of register to write to
DATA	data byte to be written into register
A/NA	acknowledge or not acknowledge
P	STOP condition

It is allowed to send more than one data byte per transmission to the TDA9874H. In that case, the subaddress is automatically incremented after each data byte, resulting in storing the sequence of data bytes at successive register locations, starting at SUBADDRESS. A transmission can start at any valid subaddress. Each byte that is properly stored, is acknowledged with A (acknowledge). If an attempt is made to write data to a non-existing subaddress, the device acknowledges with NA (not acknowledge), therefore telling the I<sup>2</sup>C-bus master to abort the transmission. There is no 'wrap-around' of subaddresses.

Commands and data will be processed as soon as they have been received completely. Functions requiring more than one byte will, thus, be executed only after all bytes for that function have been received. If the transmission is terminated (STOP condition) before all bytes have been received, the incomplete data for that function are ignored.

**Table 10** Format for a transmission employing auto-increment of subaddresses

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA BYTE A n data bytes with auto-increment of subaddresses	DATA	A/NA	P
---	---------------	---	---	------------	---	--	------	------	---

Data patterns sent to the various subaddresses are not checked for being illegal or not at that address, except for the level adjust functions.

Detection of a STOP condition without a preceding acknowledge bit is regarded as a bus error. In this case, the last operation will not be executed.

Overview of the slave receiver registers

ADDRESS (HEX)	DATA								FUNCTION
	7	6	5	4	3	2	1	0	
	B7	B6	B5	B4	B3	B2	B1	B0	AGC gain selection (ignored, if AGC on)
	P2OUT	P1OUT	STDBY	INIT	0	AGCSLOW	AGCOFF	SIFSEL	general configuration
	–	–	–	MCSM1	MCSM0	–	MSS1	MSS0	monitor select
	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; MS part
	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency
	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; LS part
	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency; MS part
	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency
	B7	B5	B5	B4	B3	B2	B1	B0	carrier 2 frequency; LS part
	IDMOD1	IDMOD0	IDAREA	–	CH2MOD1	CH2MOD0	CH1WIDE	CH1MODE	demodulator configuration
	ADEEM2	FMDSC23	FMDSC22	FMDSC21	ADEEM1	FMDSC13	FMDSC12	FMDSC11	FM de-emphasis
	–	–	–	–	–	FDMS2	FDMS1	FDMS0	FM dematrix
	B7	B6	B5	B4	B3	B2	B1	B0	Channel 1 output level adjust
	B7	B6	B5	B4	B3	B2	B1	B0	Channel 2 output level adjust
	–	–	TIMPOL	DOUTEN	–	AMSEL	NDEEM	AMUTE	NICAM configuration
	B7	B6	B5	B4	B3	B2	B1	B0	NICAM output level adjust
	B7	B6	B5	B4	B3	B2	B1	B0	NICAM lower error limit
	B7	B6	B5	B4	B3	B2	B1	B0	NICAM upper error limit
	1	MUTI2S	1	1	1	MUTOUT	1	1	audio mute control
	DGS1	–	–	–	DGS0	–	DOS1	DOS0	DAC output select
	–	CSM2	CSM1	CSM0	–	–	SS1	SS0	analog output select
	–	–	–	SYSCL1	SYSCL0	SYSOUT	I2SFORM	IS2OUT	digital audio interface configuration
	–	ICSM2	ICSM1	ICSM0	–	–	ISS1	ISS0	I <sup>2</sup> S output select
	B7	B6	B5	B4	B3	B2	B1	B0	I <sup>2</sup> S output level adjust

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## 7.3.1 AGC GAIN REGISTER (AGCGR)

If the Automatic Gain Control (AGC) function is switched off in the General Configuration Register (see Section 7.3.2), the contents of this register defines a fixed gain of the SIF input stage. The input voltages given are meant to generate a nearly full-scale output from the SIF ADC. If the AGC is on, the contents of this register are ignored. The default setting at power-up is 00000000. In Table 12 the stated step number corresponds with the SIF level read from subaddress 7 (see Section 7.4.6); the input voltages should be considered as approximate target values.

Table 12 AGC Gain Register (subaddress 0)

7	6	5	4	3	2	1	0	STEP	SIF INPUT VOLTAGE (mV (RMS))
B7	B6	B5	B4	B3	B2	B1	B0		
0	0	0	1	1	1	1	1	31	240
0	0	0	1	1	1	1	0	30	214
0	0	0	1	1	1	0	1	29	195
0	0	0	1	1	1	0	0	28	176
0	0	0	1	1	0	1	1	27	159
0	0	0	1	1	0	1	0	26	145
0	0	0	1	1	0	0	1	25	131
0	0	0	1	1	0	0	0	24	119
0	0	0	1	0	1	1	1	23	107
0	0	0	1	0	1	1	0	22	99
0	0	0	1	0	1	0	1	21	90
0	0	0	1	0	1	0	0	20	82
0	0	0	1	0	0	1	1	19	76
0	0	0	1	0	0	1	0	18	70
0	0	0	1	0	0	0	1	17	65
0	0	0	1	0	0	0	0	16	60
0	0	0	0	1	1	1	1	15	55
0	0	0	0	1	1	1	0	14	51
0	0	0	0	1	1	0	1	13	48
0	0	0	0	1	1	0	0	12	45
0	0	0	0	1	0	1	1	11	42
0	0	0	0	1	0	1	0	10	39
0	0	0	0	1	0	0	1	9	36
0	0	0	0	1	0	0	0	8	34
0	0	0	0	0	1	1	1	7	32
0	0	0	0	0	1	1	0	6	30
0	0	0	0	0	1	0	1	5	29
0	0	0	0	0	1	0	0	4	27
0	0	0	0	0	0	1	1	3	25
0	0	0	0	0	0	1	0	2	24
0	0	0	0	0	0	0	1	1	23
0	0	0	0	0	0	0	0	0	22

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## 7.3.2 GENERAL CONFIGURATION REGISTER (GCONR)

The default setting at power-up is 11000000.

**Table 13** General Configuration Register (subaddress 1)

7	6	5	4	3	2	1	0
P2OUT	P1OUT	STDBY	INIT	–	AGCSLOW	AGCOFF	SIFSEL

**Table 14** Description of GCONR bits

BIT	SYMBOL	DESCRIPTION
7	P2OUT	<b>General purpose I/O pins 1 and 2.</b> These bits control general-purpose input/output pins. The contents of these bits is written directly to the corresponding pins. If an input is desired, the bits must be set HIGH to allow the pins to be pulled LOW externally. Input from the pins is reflected in the Device Status Register (see Section 7.4.1). P1OUT is recommended to be used for switching an SIF trap for the adjacent picture carrier in designs that employ such a trap.
6	P1OUT	
5	STDBY	<b>Standby mode on/off.</b> STDBY = 1, puts the TDA9874H into the Standby mode. Most functions are disabled and power dissipation is somewhat reduced. STDBY = 0, the TDA9874H is in its normal mode of operation. On return from Standby mode, the device is in its Power-on reset mode and needs to be re-initialized with data defined by the setmaker.
4	INIT	<b>Initialize to default settings.</b> INIT = 1, causes initialization of TDA9874H to its default settings. This has the same effect as a power-on reset. In case there is a conflict between the default settings and any bit set HIGH in this register, the bits of this register have priority over the corresponding default setting. This bit is automatically reset to LOW after initialization has completed. When set LOW, the TDA9874H is in its normal mode of operation.
3	–	This bit is not used and should be set to a logic 0.
2	AGCSLOW	<b>AGC decay time.</b> AGCSLOW = 1, a longer decay time and larger hysteresis are selected for input signals with strong video modulation (intercarrier). This bit has only an effect, when bit AGCOFF = 0. AGCSLOW = 0, selects normal attack and decay times for the AGC and a small hysteresis. <b>Note.</b> AGCSLOW bit should be set to HIGH for best possible audio performance.
1	AGCOFF	<b>AGC on/off.</b> AGCOFF = 1, forces the AGC block to a fixed gain as defined in the AGC Gain Register (see Section 7.3.1). AGCOFF = 0, the automatic gain control function is enabled and the contents of the AGC gain register is ignored.
0	SIFSEL	<b>SIF input select.</b> SIFSEL = 1, selects pin SIF2 for input (recommended for satellite tuner). SIFSEL = 0, pin SIF1 (recommended for terrestrial TV) is selected.

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## 7.3.3 MONITOR SELECT REGISTER (MSR)

This register is used to define the signal source, the level of which is to be monitored, and the signal channel. Data can be monitored before or behind the DC filter at the FM/AM demodulator outputs. The last available data sample can be read-out in the I<sup>2</sup>C-bus slave transmitter mode (see Section 7.4.5).

Phase means the differentiated phase output of the FM demodulator and is provided, when the demodulator operates in FM mode, while magnitude is supplied in AM mode.

The default setting at power-up is 00000000.

Table 15 Monitor Select Register (subaddress 2)

7	6	5	4	3	2	1	0
–	–	–	MCSM1	MCSM0	–	MSS1	MSS0

Table 16 Description of MSR bits

BIT	SYMBOL	DESCRIPTION
7	–	These 3 bits are not used and should be set to logic 0.
6	–	
5	–	
4	MCSM1	<b>Signal channel select.</b> The state of these 2 bits determine which signal channel is selected; see Table 17.
3	MCSM0	
2	–	This bit is not used and should be set to logic 0.
1	MSS1	<b>Signal source select.</b> The state of these 2 bits determine which signal source is selected; see Table 18.
0	MSS0	

Table 17 Signal channel selection

MCSM1	MCSM0	SIGNAL CHANNEL
0	0	$\frac{\text{Channel 1} + \text{Channel 2}}{2}$
0	1	Channel 1
1	0	Channel 2

Table 18 Signal source selection

MSS1	MSS0	SIGNAL SOURCE
0	0	DC output of FM/AM demodulator
0	1	magnitude/phase output of FM/AM demodulator
1	0	FM/AM path output
1	1	NICAM path output

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7.3.4 CARRIER 1 FREQUENCY REGISTER (C1FR)

Three bytes are required to define a 24-bit frequency control word to represent the sound carrier (i.e. mixer) frequency. These three bytes are stored at subaddresses 3 to 5; subaddress 3 being the High byte. Execution of the command starts only after all bytes have been received. If an error occurs, e.g. a premature STOP condition, partial data for this function are ignored. The sound carrier frequency can be calculated in accordance with the following formula:

$$\text{data} = \frac{f_{\text{mix}}}{f_{\text{clk}}} \times 2^{24}$$

with:

- data = 24-bit frequency control word
- $f_{\text{mix}}$  = desired sound carrier frequency
- $f_{\text{clk}}$  = 12.288 MHz (clock frequency of mixer)
- $2^{24}$  = 16777216 (number of steps in a 24-bit word size).

Example: A 5.5 MHz sound carrier frequency will be generated by sending the following sequence of data bytes to the TDA9874H (data = 7509333 in decimal notation or 729555 in hexadecimal notation): 01110010 10010101 01010101.

The default setting at power-up is 00000000 for all three bytes.

**Table 19** Carrier 1 Frequency Register High byte (subaddress 3)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
B7	B6	B5	B4	B3	B2	B1	B0

**Table 20** Carrier 1 Frequency Register Middle byte (subaddress 4)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
B7	B6	B5	B4	B3	B2	B1	B0

**Table 21** Carrier 1 Frequency Register Low byte (subaddress 5)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
B7	B6	B5	B4	B3	B2	B1	B0

7.3.5 CARRIER 2 FREQUENCY REGISTER (C2FR)

The format is the same as for sound carrier 1, except subaddresses 6 to 8 are used. Subaddress 6 holds the High byte. If the Carrier 2 Frequency Register is used, it will be for either the second FM sound carrier of a terrestrial or satellite FM program or the NICAM sound carrier.

7.3.5.1 Note

While NICAM mode is used, the sound carrier 2 frequency should be set  $\pm 2$  kHz of the NICAM carrier frequency to improve carrier loop settling. For a deviation of +2 kHz this results in the following settings:

**Standard B/G, D/K and L:** 5.850 MHz + 2 kHz = 5.852 MHz = (79EAAAH).

**Standard I:** 6.552 MHz + 2 kHz = 6.554 MHz = (888AAAH).

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## 7.3.6 DEMODULATOR CONFIGURATION REGISTER (DCONR)

The default setting at power-up is 00000000.

**Table 22** Demodulator Configuration Register (subaddress 9)

7	6	5	4	3	2	1	0
IDMOD1	IDMOD0	IDAREA	–	CH2MOD1	CH2MOD0	CH1WIDE	CH1MODE

**Table 23** Description of DCONR bits

BIT	SYMBOL	DESCRIPTION
7	IDMOD1	<b>Identification mode for FM sound.</b> These bits define the integrator time of the FM identification. A valid result may be expected after twice this time has expired, at the latest. The longer the time, the more reliable the identification. See Table 24.
6	IDMOD0	
5	IDAREA	<b>Application area for FM identification.</b> IDAREA = 1, selects FM identification frequencies in accordance with the specification for Korea. IDAREA = 0, frequencies for Europe are selected (B/G and D/K standard).
4	–	This bit is not used and should be set to logic 0.
3	CH2MOD1	<b>Channel 2 receive mode.</b> These bits control the hardware for the second sound carrier in accordance with Table 25. NICAM mode employs a wider bandwidth of the decimation filters than FM mode.
2	CH2MOD0	
1	CH1WIDE	<b>Channel 1 bandwidth.</b> CH1WIDE = 1, switches the decimation filters for the first sound carrier to a wide bandwidth, so that the main sound carrier of a satellite channel with its larger deviation can be handled without additional distortion. CH1WIDE = 0, the bandwidth is narrow to cope with the intermodulation requirements of FM stereo.
0	CH1MODE	<b>Channel 1 receive mode.</b> CH1MODE = 1, selects the hardware for the first sound carrier to operate in AM mode. CH1MODE = 0, FM mode is selected. This applies to both terrestrial and satellite FM reception.

**Table 24** Identification mode

IDMOD1	IDMOD0	IDENTIFICATION MODE
0	0	slow
0	1	medium
1	0	fast
1	1	off/reset

**Table 25** Channel 2 receive mode

CH2MOD1	CH2MOD0	CHANNEL 2
0	0	FM
0	1	AM
1	0	NICAM

## 7.3.6.1 Notes

It is recommended to switch the FM sound mode identification off whenever the received program is not a terrestrial 2-carrier sound. Switching the identification off will reset the associated hardware to a defined state.

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Changing the FM identification mode during FM reception may cause a brief flickering of bit IDSTE or IDUA in the Device Status Register (see Section 7.4.1).

When Channel 2 is used to receive FM sound carriers with the current application proposal (see Chapter 9), it is recommended to set the TIMPOL bit HIGH (write subaddress 14; see Section 7.3.11) for best S/N performance.

7.3.7 FM DE-EMPHASIS REGISTER (FMDR)

This register is used to select the proper de-emphasis characteristics as appropriate for the standard of the received carrier. Bits B3 to B0 apply to sound carrier 1, bits B7 to B4 apply to sound carrier 2. In the event of A2 reception, both groups must be set to the same characteristics.

The default setting at power-up is 10001000.

Table 26 FM De-emphasis Register (subaddress 10)

7	6	5	4	3	2	1	0
ADEEM2	FMDSC23	FMDSC22	FMDSC21	ADEEM1	FMDSC13	FMDSC12	FMDSC11

Table 27 Description of FMDR bits

BIT	SYMBOL	DESCRIPTION
7	ADEEM2	<b>Adaptive de-emphasis on/off.</b> ADEEM2 = 1, activates the adaptive de-emphasis function (for Wegener-Panda 1 encoded programs), which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 μs. ADEEM2 = 0, the adaptive de-emphasis is off.
6	FMDSC23	<b>FM de-emphasis.</b> The state of these 3 bits determine the FM de-emphasis for sound carrier 2; see Table 28.
5	FMDSC22	
4	FMDSC21	
3	ADEEM1	<b>Adaptive de-emphasis on/off.</b> ADEEM1 = 1, activates the adaptive de-emphasis function (for Wegener-Panda 1 encoded programs), which is required for certain satellite FM channels. The standard FM de-emphasis must then be set to 75 μs. ADEEM1 = 0, the adaptive de-emphasis is off.
2	FMDSC13	<b>FM de-emphasis.</b> The state of these 3 bits determine the FM de-emphasis for sound carrier 1; see Table 28.
1	FMDSC12	
0	FMDSC11	

Table 28 De-emphasis

FMDSC23	FMDSC22	FMDSC21	DE-EMPHASIS <sup>(1)</sup>
FMDSC13	FMDSC12	FMDSC11	
0	0	0	50 μs
0	0	1	60 μs
0	1	0	75 μs
0	1	1	J17
1	0	0	off

Note

- 1. The FM de-emphasis gain is 0 dB at 40 Hz.



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## 7.3.8 FM DEMATRIX REGISTER (FMMR)

This register is used to select the proper dematrixing characteristics as appropriate for the standard of the received carrier and the related sound mode identification. For the dematrixing, it is assumed that the output from sound carrier 1 is on channel L input. Bits B3 to B7 are not used and should be set to logic 0.

The default setting at power-up is 00000000.

**Table 29** FM Dematrix Register (subaddress 11)

7	6	5	4	3	2	1	0
–	–	–	–	–	FDMS2	FDMS1	FDMS0

**Table 30** Description of FMMR bits

BIT	SYMBOL	DESCRIPTION
7	–	These 5 bits are not used and should be set to logic 0.
6	–	
5	–	
4	–	
3	–	
2	FDMS2	<b>Dematrixing characteristics select.</b> The state of these 3 bits select the dematrixing characteristics; see Table 31.
1	FDMS1	
0	FDMS0	

**Table 31** Selection of the dematrixing characteristics

FDMS2	FDMS1	FDMS0	L OUTPUT	R OUTPUT	MODE
0	0	0	L input	L input	forced mono
0	0	1	R input	R input	mono 2
0	1	0	L input	R input	dual
0	1	1	R input	L input	dual swapped
1	0	0	2L input – R input	R input	stereo Europe
1	0	1	$\frac{L \text{ input} + R \text{ input}}{2}$	$\frac{L \text{ input} - R \text{ input}}{2}$	stereo Korea

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## 7.3.9 CHANNEL 1 OUTPUT LEVEL ADJUST REGISTER (C1OLAR)

This register is used to correct for standard and station-dependent differences of signal levels. Table 32 applies to sound carrier 1. The default setting at power-up is 00000000.

**Table 32** Channel 1 Output Level Adjust Register (subaddress 12)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	-1
0	0	0	1	1	1	0	1	-2
0	0	0	1	1	1	0	0	-3
0	0	0	1	1	0	1	1	-4
0	0	0	1	1	0	1	0	-5
0	0	0	1	1	0	0	1	-6
0	0	0	1	1	0	0	0	-7
0	0	0	1	0	1	1	1	-8
0	0	0	1	0	1	1	0	-9
0	0	0	1	0	1	0	1	-10
0	0	0	1	0	1	0	0	-11
0	0	0	1	0	0	1	1	-12
0	0	0	1	0	0	1	0	-13
0	0	0	1	0	0	0	1	-14
0	0	0	1	0	0	0	0	-15

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7.3.10 CHANNEL 2 OUTPUT LEVEL ADJUST REGISTER (C2OLAR)

This register is used to correct for standard and station-dependent differences of signal levels. Table 33 applies to sound carrier 2 in its FM and AM modes. In the event of FM stereo or FM dual language reception, Channels 1 and 2 shall be adjusted to the same level. The default setting at power-up is 00000000.

**Table 33** Channel 2 Output Level Adjust Register (subaddress 13)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	-1
0	0	0	1	1	1	0	1	-2
0	0	0	1	1	1	0	0	-3
0	0	0	1	1	0	1	1	-4
0	0	0	1	1	0	1	0	-5
0	0	0	1	1	0	0	1	-6
0	0	0	1	1	0	0	0	-7
0	0	0	1	0	1	1	1	-8
0	0	0	1	0	1	1	0	-9
0	0	0	1	0	1	0	1	-10
0	0	0	1	0	1	0	0	-11
0	0	0	1	0	0	1	1	-12
0	0	0	1	0	0	1	0	-13
0	0	0	1	0	0	0	1	-14
0	0	0	1	0	0	0	0	-15

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## 7.3.11 NICAM CONFIGURATION REGISTER (NCONR)

The default setting at power-up is 00000000.

**Table 34** NICAM Configuration Register (subaddress 14)

7	6	5	4	3	2	1	0
–	–	TIMPOL	DOUTEN	–	AMSEL	NDEEM	AMUTE

**Table 35** Description of NCONR bits

BIT	SYMBOL	DESCRIPTION
7	–	These 2 bits are not used and should be set to logic 0.
6	–	
5	TIMPOL	<b>Timing loop polarity.</b> TIMPOL = 1, inverts the polarity. This feature can be used to compensate for the phase shift that is introduced by an external inverting amplifier at the pin $V_{\text{tune}}$ . Such an amplifier could be used to provide a larger tuning voltage swing for the VCXO. TIMPOL = 0, sets the NICAM timing loop to normal polarity.
4	DOUTEN	<b>Data output enable.</b> DOUTEN = 1, enables the output of the NICAM serial data stream from the DQPSK demodulator and of the associated clock, PCLK. DOUTEN = 0, both outputs will be 3-stated.
3	–	This bit is not used and should be set to logic 0.
2	AMSEL	<b>Auto-mute select.</b> AMSEL = 1, the auto-mute will switch between NICAM sound and the analog mono input. This bit has only an effect when the auto-mute function is enabled and when the DAC has been selected in the Analog Output Select Register (see Section 7.3.17). AMSEL = 0, the auto-mute will switch between NICAM sound and the sound on the first sound carrier (i.e. FM mono or AM).
1	NDEEM	<b>De-emphasis on/off.</b> NDEEM = 1, switches the NICAM J17 de-emphasis off. NDEEM = 0, switches the NICAM J17 de-emphasis on.
0	AMUTE	<b>Auto-muting on/off.</b> AMUTE = 1, automatic muting is disabled. This bit has only an effect, when the second sound carrier is set to NICAM. AMUTE = 0, enables the automatic switching between NICAM and the program on the first sound carrier (i.e. FM mono or AM), dependent on the NICAM bit error rate.

## 7.3.11.1 Notes

The decision of whether auto-muting is permitted shall be taken by the controlling microprocessor based on information contained in the TDA9874H's status registers. Thus, it depends on the strategy implemented in the software whether the auto-mute function is in accordance with "NICAM 728 ETS Revised for Data Applications" or any other preference.

The NICAM de-emphasis gain is 0 dB at 40 Hz.

The AMSEL bit has only an effect on the analog sound outputs (OUTL and OUTF). With regard to the digital sound output (I<sup>2</sup>S), the auto-mute will only switch between NICAM and the first sound carrier.

When carrier 2 is in FM mode, the TIMPOL bit should be set HIGH, to achieve the best S/N performance with the current oscillator application proposal (see Chapter 9).

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## 7.3.12 NICAM OUTPUT LEVEL ADJUST REGISTER (NOLAR)

This register is used to correct for standard and station-dependent differences of signal levels. Table 36 applies to both NICAM sound outputs. The default setting at power-up is 00000000.

**Table 36** NICAM Output Level Adjust Register (subaddress 15)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	-1
0	0	0	1	1	1	0	1	-2
0	0	0	1	1	1	0	0	-3
0	0	0	1	1	0	1	1	-4
0	0	0	1	1	0	1	0	-5
0	0	0	1	1	0	0	1	-6
0	0	0	1	1	0	0	0	-7
0	0	0	1	0	1	1	1	-8
0	0	0	1	0	1	1	0	-9
0	0	0	1	0	1	0	1	-10
0	0	0	1	0	1	0	0	-11
0	0	0	1	0	0	1	1	-12
0	0	0	1	0	0	1	0	-13
0	0	0	1	0	0	0	1	-14
0	0	0	1	0	0	0	0	-15

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7.3.13 NICAM LOWER ERROR LIMIT REGISTER (NLELR)

When the auto-mute function is enabled (see Section 7.3.11) and the NICAM bit error count is lower than the value contained in this register, the NICAM signal is selected (again) for reproduction. See also Section 7.3.14.

The default setting at power-up is 00010100.

**Table 37** NICAM Lower Error Limit Register (subaddress 16)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.3.14 NICAM UPPER ERROR LIMIT REGISTER (NUELR)

When the auto-mute function is enabled (see Section 7.3.11) and the NICAM bit error count is higher than the value contained in this register, the signal of the first sound carrier (i.e. FM mono or AM sound) or the analog mono input is selected for reproduction.

The difference between upper and lower error limit constitutes a hysteresis to avoid frequent switching between NICAM and the program on the first sound carrier.

The default setting at power-up is 01010000.

**Table 38** NICAM Upper Error Limit Register (subaddress 17)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.3.15 AUDIO MUTE CONTROL REGISTER (AMCONR)

Only bits 6 and 2 are used. The state of the unused bits should be set to logic 1. When any of these bits is set HIGH, the corresponding pair of output channels will be muted. A LOW bit allows normal signal output.

The default setting at power-up is 11111111.

**Table 39** Audio Mute Control Register (subaddress 18)

7	6	5	4	3	2	1	0
–	MUT1 <sup>2</sup> S	–	–	–	MUTOUT	–	–

7.3.16 DAC OUTPUT SELECT REGISTER (DACOSR)

This register is used to define the signal source to be entered into the DAC. The DAC is used for signal output from digital sources at analog outputs.

The two combinations of FM and NICAM shown in Table 42 apply to the (rare) condition that three different languages are being broadcast in an FM + NICAM system. They allow for a two-out-of-three selection for special applications. Note that the controlling microprocessor has to assure that the FM dematrix is set to the mono position.

Some extra gain can be introduced at the input to the DAC to provide a coarse level adjust function.

The default setting at power-up is 00000000.

Bits B2, B4, B5 and B6 are not used and should be set to logic 0.

**Table 40** DAC Output Select Register (subaddress 19)

7	6	5	4	3	2	1	0
DGS1	–	–	–	DGS0	–	DOS1	DOS0

**Table 41** Selection of DAC gain

DGS1	DGS0	DAC GAIN (dB)
0	0	0
0	1	3
1	0	6
1	1	9

**Table 42** Signal source left and right

DOS1	DOS0	SIGNAL SOURCE	
		LEFT	RIGHT
0	0	FM/AM	FM/AM
0	1	NICAM left	NICAM right
1	0	FM/AM	NICAM M1
1	1	FM/AM	NICAM M2

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## 7.3.17 ANALOG OUTPUT SELECT REGISTER (AOSR)

This register is used to define both the signal source to be output at the analog outputs and the output channel selector mode.

The DAC outputs are automatically muted, in case one of the analog inputs is selected for output.

The  $\frac{L+R}{2}$  position of the matrix applies only to the DAC outputs, it is not available for analog input signals.

The default setting at power-up is 00000000.

**Table 43** Analog Output Select Register (subaddress 20)

7	6	5	4	3	2	1	0
–	CSM2	CSM1	CSM0	–	–	SS1	SS0

**Table 44** Description of AOSR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is not used and should be set to logic 0.
6	CSM2	<b>Output channel selection mode.</b> These 3 bits select the output channel selection mode; see Table 45.
5	CSM1	
4	CSM0	
3	–	These 2 bits are not used and should be set to logic 0.
2	–	
1	SS1	<b>Signal source.</b> These 2 bits select the signal source; see Table 46.
0	SS0	

**Table 45** Output channel selection mode

CSM2	CSM1	CSM0	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L+R}{2}$	$\frac{L+R}{2}$

**Table 46** Signal source selection

SS1	SS0	SIGNAL SOURCE
0	0	DAC
1	0	external input
1	1	mono input

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7.3.18 DIGITAL AUDIO INTERFACE CONFIGURATION REGISTER (DAICONR)

The default setting at power-up is 00000000.

**Table 47** Digital Audio Interface Configuration Register (subaddress 21)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
–	–	–	SYSCL1	SYSCL0	SYSOUT	I <sup>2</sup> SFORM	I <sup>2</sup> SOUT

**Table 48** Description of DAICONR bits

BIT	SYMBOL	DESCRIPTION
7	–	These 3 bits are not used and should be set to logic 0.
6	–	
5	–	
4	SYSCL1	<b>System clock frequency select.</b> These 2 bits select the frequency of the system clock; see Table 49.
3	SYSCL0	
2	SYSOUT	<b>System clock output on/off.</b> SYSOUT = 1, enables the output of a system (or master) clock signal at pin SYSCLK. SYSOUT = 0, the output will be off, thereby improving EMC performance.
1	I <sup>2</sup> SFORM	<b>Serial output format.</b> I <sup>2</sup> SFORM = 1, selects an MSB-aligned, MSB-first output format, i.e. a level change at the word select pin indicates the beginning of a new audio sample. I <sup>2</sup> SFORM = 0, selects the standard I <sup>2</sup> S output format.
0	I <sup>2</sup> SOUT	<b>I<sup>2</sup>S output on/off.</b> I <sup>2</sup> SOUT = 1, enables the output of serial audio data (2 pins) plus serial bit clock and word select in a format determined by the I <sup>2</sup> SFORM bit. The TDA9874H then is an I <sup>2</sup> S-bus master. I <sup>2</sup> SOUT = 0, the outputs mentioned will be 3-stated, thereby improving EMC performance.

**Table 49** System clock frequency select

SYSCL1	SYSCL0	SYSCLK OUTPUT	FREQUENCY (MHz)
0	0	256f <sub>s</sub>	8.192
0	1	384f <sub>s</sub>	12.288
1	0	512f <sub>s</sub>	16.384
1	1	768f <sub>s</sub>	24.576



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7.3.19 I<sup>2</sup>S OUTPUT SELECT REGISTER (I<sup>2</sup>SOSR)

This register is used to define both the signal source to be output at the I<sup>2</sup>S port and the mode of the digital matrix for signal selection.

The two combinations of FM and NICAM shown in Table 53 apply to the (rare) condition that three different languages are being broadcast in an FM + NICAM system. They allow for a two-out-of-three selection for special applications. Note that the controlling microprocessor has to assure that the FM dematrix is set to the mono position.

The default setting at power-up is 00000000.

**Table 50** I<sup>2</sup>S Output Select Register (subaddress 22)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
–	ICSM2	ICSM1	ICSM0	–	–	ISS1	ISS0

**Table 51** Description of I<sup>2</sup>SOSR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is not used and should be set to logic 0.
6	ICSM2	<b>Output channel selection mode.</b> These 3 bits select the output channel selection mode; see Table 52.
5	ICSM1	
4	ICSM0	
3	–	These 2 bits are not used and should be set to logic 0.
2	–	
1	ISS1	<b>Signal source.</b> These 2 bits select the signal source; see Table 53.
0	ISS0	

**Table 52** Mode of the digital matrix for signal selection

ICSM2	ICSM1	ICSM0	L OUTPUT	R OUTPUT
0	0	0	L input	R input
0	0	1	L input	L input
0	1	0	R input	R input
0	1	1	R input	L input
1	0	0	$\frac{L + R}{2}$	$\frac{L + R}{2}$

**Table 53** Signal source left and right

ISS1	ISS0	SIGNAL SOURCE	
		LEFT	RIGHT
0	0	FM left	FM right
0	1	NICAM left	NICAM right
1	0	FM mono	NICAM M1
1	1	FM mono	NICAM M2

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7.3.20 I<sup>2</sup>S OUTPUT LEVEL ADJUST REGISTER (I<sup>2</sup>SOLAR)

This register is used to adjust the output level at the I<sup>2</sup>S port. Left and right signal channels are treated identically. The default setting at power-up is 00000000.

**Table 54** I<sup>2</sup>S output Level Adjust Register (subaddress 23)

7	6	5	4	3	2	1	0	GAIN SETTING (dB)
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	1	1	1	1	+15
0	0	0	0	1	1	1	0	+14
0	0	0	0	1	1	0	1	+13
0	0	0	0	1	1	0	0	+12
0	0	0	0	1	0	1	1	+11
0	0	0	0	1	0	1	0	+10
0	0	0	0	1	0	0	1	+9
0	0	0	0	1	0	0	0	+8
0	0	0	0	0	1	1	1	+7
0	0	0	0	0	1	1	0	+6
0	0	0	0	0	1	0	1	+5
0	0	0	0	0	1	0	0	+4
0	0	0	0	0	0	1	1	+3
0	0	0	0	0	0	1	0	+2
0	0	0	0	0	0	0	1	+1
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	not defined
0	0	0	1	1	1	1	0	-1
0	0	0	1	1	1	0	1	-2
0	0	0	1	1	1	0	0	-3
0	0	0	1	1	0	1	1	-4
0	0	0	1	1	0	1	0	-5
0	0	0	1	1	0	0	1	-6
0	0	0	1	1	0	0	0	-7
0	0	0	1	0	1	1	1	-8
0	0	0	1	0	1	1	0	-9
0	0	0	1	0	1	0	1	-10
0	0	0	1	0	1	0	0	-11
0	0	0	1	0	0	1	1	-12
0	0	0	1	0	0	1	0	-13
0	0	0	1	0	0	0	1	-14
0	0	0	1	0	0	0	0	-15

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**7.4 Slave transmitter mode**

As a slave transmitter, the TDA9874H provides 12 registers with status information and data, a part of which is for Philips internal purposes only. Each register is accessed by means of a subaddress.

Detailed descriptions of the slave transmitter registers are given in Sections 7.4.1 to 7.4.9.

**Table 55** General format for reading data from the TDA9874H

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	Sr	SLAVE ADDRESS	1	A	DATA	NAm	P
---	---------------	---	---	------------	---	----	---------------	---	---	------	-----	---

**Table 56** Explanation of Tables 55 and 57

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
A	acknowledge (by the slave)
SUBADDRESS	address of register to read from
Sr	repeated START condition
1	data direction bit (read from device)
DATA	data byte read from register
NAm	not acknowledge (by the master)
Am	acknowledge (by the master)
P	STOP condition

Reading of data can start at any valid subaddress. It is allowed to read more than 1 data byte per transmission from the TDA9874H. In that case, the subaddress is automatically incremented after each data byte, resulting in reading the sequence of data bytes from successive register locations, starting at SUBADDRESS.

**Table 57** Format of a transmission using automatic incrementing of subaddresses

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	Sr	SLAVE ADDRESS	1	A	DATA BYTE Am n data bytes with auto-increment of subaddresses	DATA	NAm	P
---	---------------	---	---	------------	---	----	---------------	---	---	---	------	-----	---

Each data byte in a read sequence, except for the last one, is acknowledged with Am. The subaddresses 'wrap around' from decimal 255 to 0. If an attempt is made to read from a non-existing subaddress, the device will send a data pattern of all ones, i.e. FF in hexadecimal notation.

Overview of the slave transmitter registers

ADDRESS (HEX)	DATA								FUNCTION
	7	6	5	4	3	2	1	0	
	P2IN	P1IN	RSSF	AMSTAT	VDSP	IDDUA	IDSTE	– <sup>(1)</sup>	device status (identification, etc.)
	C4	C3	C2	C1	OSB	CFC	S/MB	D/SB	NICAM status
	B7	B6	B5	B4	B3	B2	B1	B0	NICAM error count
	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	additional data (LSB)
	OVW	SAD	– <sup>(1)</sup>	CI1	CI2	AD10	AD9	AD8	additional data (MSB)
	B7	B6	B5	B4	B3	B2	B1	B0	level read-out (MSB)
	B7	B6	B5	B4	B3	B2	B1	B0	level read-out (LSB)
	– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	B4	B3	B2	B1	B0	SIF level
<sup>(2)</sup>	B7	B6	B5	B4	B3	B2	B1	B0	Test Register 2
<sup>(2)</sup>	B7	B6	B5	B4	B3	B2	B1	B0	Test Register 1
<sup>(2)</sup>	B7	B6	B5	B4	B3	B2	B1	B0	device identification code
<sup>(2)</sup>	B7	B6	B5	B4	B3	B2	B1	B0	software identification code

is undefined.

Registers from subaddress 252 to 255 are for Philips internal purposes only. They are considered as a set of registers for the identification of individual members and some key parameters in a family of devices.

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## 7.4.1 DEVICE STATUS REGISTER (DSR)

**Table 59** Device Status Register (subaddress 0)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
P2IN	P1IN	RSSF	AMSTAT	VDSP	IDDUA	IDSTE	–

**Table 60** Description of DSR bits

<b>BIT</b>	<b>SYMBOL</b>	<b>DESCRIPTION</b>
7	P2IN	<b>Input from Port 2.</b> This bit reflects the status of the P2 general purpose port pin; see Section 7.3.2. If P2IN = 1, then the P2 general purpose port pin is HIGH. If P2IN = 0, then the P2 general purpose port pin is LOW.
6	P1IN	<b>Input from Port 1.</b> This bit reflects the status of the P1 general purpose port pin; see Section 7.3.2. If P1IN = 1, then the P1 general purpose port pin is HIGH. If P1IN = 0, then the P1 general purpose port pin is LOW.
5	RSSF	<b>Reserve Sound Switching Flag.</b> RSSF = 1, this bit is a copy of the C4 bit in the NICAM Status Register (see Section 7.4.2). It indicates that the FM (or AM for standard L) sound matches the digital transmission and auto-muting should be enabled. RSSF = 0, auto-muting should be disabled, as analog and digital sound are different.
4	AMSTAT	<b>Auto-mute Status.</b> If this bit is HIGH, it indicates that the auto-muting function has switched from NICAM to the program of the first sound carrier (i.e. FM mono or AM in NICAM L systems).
3	VDSP	<b>Identification of NICAM sound.</b> VDSP = 1, indicates that digital transmission is a sound source. VDSP = 0, indicates the transmission is either data or a currently undefined format.
2	IDDUA	<b>Identification of FM dual sound; A2 systems.</b> If IDDUA = 1, an FM dual-language signal has been identified. When neither IDSTE nor IDDUA = 1, the received signal is assumed to be FM mono (A2 systems only).
1	IDSTE	<b>Identification of FM stereo; A2 systems.</b> If IDSTE = 1, an FM stereo signal has been identified (A2 systems only).
0	–	Value is undefined.

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7.4.2 NICAM STATUS REGISTER (NISR)

**Table 61** NICAM Status Register (subaddress 1)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
C4	C3	C2	C1	OSB	CFC	S/MB	D/SB

**Table 62** Description of NISR bits

<b>BIT</b>	<b>SYMBOL</b>	<b>DESCRIPTION</b>
7	C4	<b>NICAM application control bits.</b> These bits correspond to the control bits C1 to C4 in the NICAM transmission.
6	C3	
5	C2	
4	C1	
3	OSB	<b>Synchronization bit.</b> OSB = 1, indicates that the device has both frame and C0 (16 frame) synchronization. OSB = 0, indicates the audio output from the NICAM part is digital silence.
2	CFC	<b>Configuration change.</b> CFC = 1, indicates a configuration change at the 16 frame (C0) boundary.
1	S/MB	<b>Identification of NICAM stereo.</b> S/MB = 1, indicates stereo mode.
0	D/SB	<b>Identification of NICAM dual mono.</b> D/SB = 1, indicates dual mono mode.

7.4.2.1 Notes

The TDA9874H does not support the extended control modes. Therefore, the program of the first sound carrier (i.e. FM mono or AM) is selected for reproduction in case bit C3 is set HIGH, independent of bit AMUTE in the NICAM Configuration Register being set or not.

When a NICAM transmitter is switched off, the device will lose synchronization. In that case the program of the first sound carrier is selected for reproduction, independent of bit AMUTE being set or not.

7.4.3 NICAM ERROR COUNT REGISTER (NIECR)

Bits B7 to B0 contain the number of errors occurring in the previous 128 ms period. The register is updated every 128 ms.

**Table 63** NICAM Error Count Register (subaddress 2)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
B7	B6	B5	B4	B3	B2	B1	B0

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## 7.4.4 DATA REGISTERS (DR1 AND DR2)

The contents of these two registers provide information on the additional data bits. ADBYTE0 is stored at subaddress 3.

**Table 64** Data Register 1 (subaddress 3)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

**Table 65** Description of DR1 bits

<b>BIT</b>	<b>SYMBOL</b>	<b>DESCRIPTION</b>
7 to 0	AD7 to AD0	The lower 8 bits of the additional data word.

**Table 66** Data Register 2 (subaddress 4)

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
OVW	SAD	–	CI1	CI2	AD10	AD9	AD8

**Table 67** Description of DR2 bits

<b>BIT</b>	<b>SYMBOL</b>	<b>DESCRIPTION</b>
7	OVW	If this bit is HIGH, new additional data bits are written to the IC without the previous bits being read.
6	SAD	When SAD = 1, new additional data is written into the IC. This bit is reset, when the additional data bits are read.
5	–	Value is undefined.
4	CI1	These 2 bits are CI bits decoded by majority logic from the parity checks of the last ten samples in a frame.
3	CI2	
2	AD10	The upper 3 bits of the additional data word.
1	AD9	
0	AD8	

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7.4.5 LEVEL READ-OUT REGISTERS (LRRR AND LRRB)

These two bytes constitute a word that provides data from a location that has been specified with the FM Monitor Select Register (see Section 7.3.3). The most significant byte of the data is stored at subaddress 5.

**Table 68** Level Read-out Register A (subaddress 5)

7	6	5	4	3	2	1	0
B7 <sup>(1)</sup>	B6	B5	B4	B3	B2	B1	B0

**Note**

- 1. B7 is the most significant bit or sign bit of the word.

**Table 69** Level Read-out Register B (subaddress 6)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0 <sup>(1)</sup>

**Note**

- 1. B0 is the least significant bit of the word.

7.4.6 SIF LEVEL REGISTER (SIFLR)

When the SIF AGC is on, bits B4 to B0 of this register contain a number that gives an indication of the SIF input level. That number can be interpreted in the same way as the AGC Gain Register setting (see Section 7.3.1), i.e. if the SIF AGC were set to a fixed gain and the same number loaded into the AGC Gain Register, the current SIF input signal level would generate an SIF ADC output close to full-scale.

When the SIF AGC is off, this register returns the contents of the AGC Gain Register.

Bits B5 to B7 are not used and are undefined.

**Table 70** SIF Level Register (subaddress 7)

7	6	5	4	3	2	1	0
– <sup>(1)</sup>	– <sup>(1)</sup>	– <sup>(1)</sup>	B4	B3	B2	B1	B0

**Note**

- 1. Value is undefined.

7.4.7 TEST REGISTER 2 (TR2)

This register contains as a binary number the highest subaddress used for slave receiver registers.

The first version will have the identification 00101111.

**Table 71** Test Register 2 (subaddress 252)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.4.8 TEST REGISTER 1 (TR1)

This register contains as a binary number the highest subaddress used for slave transmitter (status) registers.

The first version will have the identification 00101111.

**Table 72** Test Register 1 (subaddress 253)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.4.9 DEVICE IDENTIFICATION CODE (DIC)

There will be several devices in the digital TV sound processor family, with TDA9874H being the second member. This byte is used to identify the individual family members.

The first version will have the identification 00000111.

**Table 73** Device Identification Code (subaddress 254)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.4.10 SOFTWARE IDENTIFICATION CODE (SIC)

It is likely that during the life time of this family of devices several versions of the DSP software will be made, e.g. to take care of new application concepts, respond to customer wishes, etc. This byte is used to identify the different releases.

The first version will have the identification 00000111.

**Table 74** Software Identification Code (subaddress 255)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0



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**8 I<sup>2</sup>S-BUS DESCRIPTION**

The digital audio interface of the TDA9874H consists of a serial audio output and associated clock signals. It can be used to supply digital audio signals from received TV programs to a suitable output device, e.g. a DAC or an AES/EBU transmitter.

Two serial audio formats are supported at the digital audio interface, i.e. the I<sup>2</sup>S-bus format and a very similar MSB-aligned format. The difference is explained in Fig.6.

In both formats the left audio channel of a stereo sample pair is output first, and is on the Serial Data line (SDO) when the Word Select line (WS) is LOW. Data is written with the trailing edge of SCK and read with the leading edge of SCK. The most significant bit is sent first.

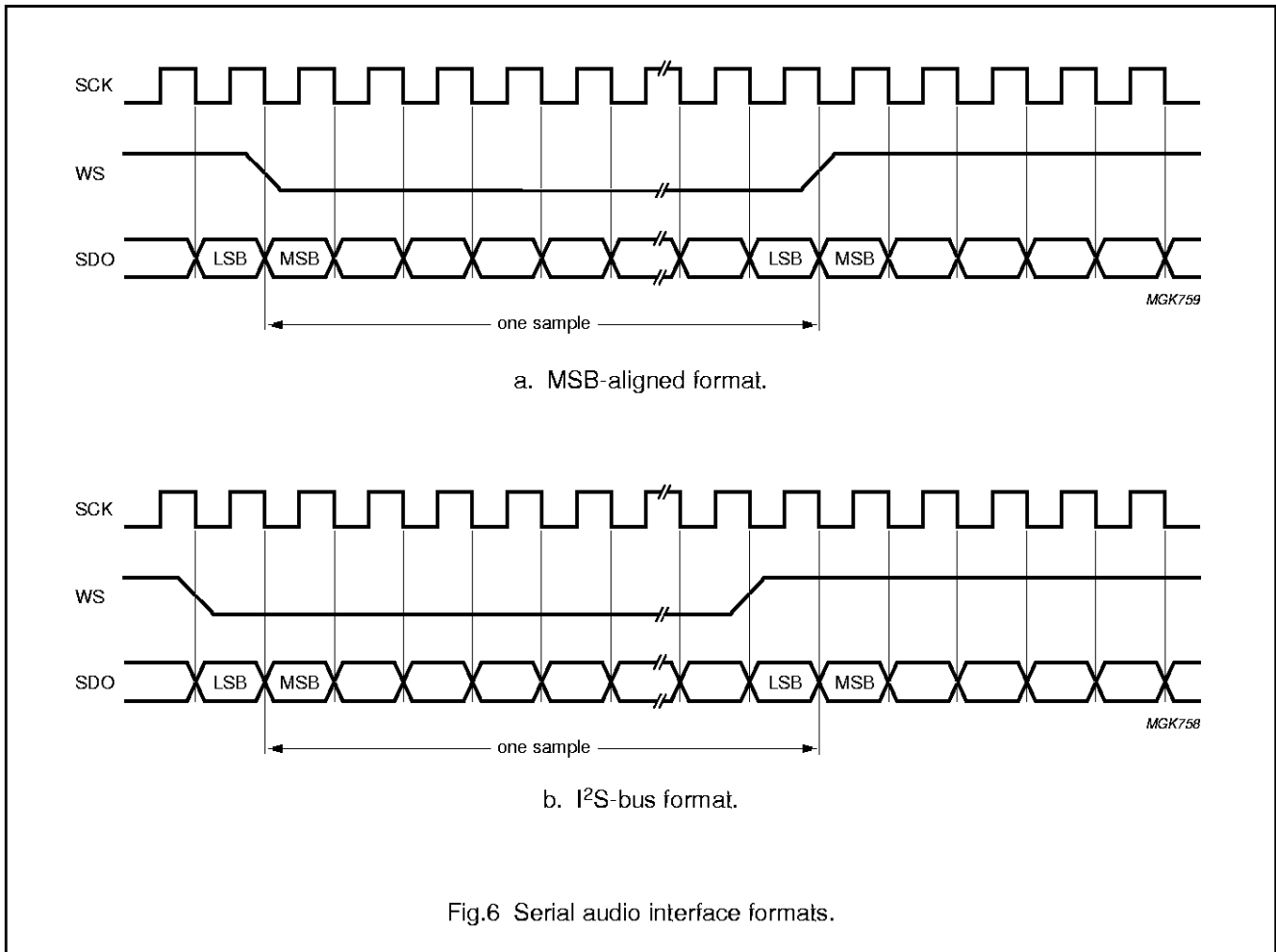
At power-up, the outputs of the digital audio interface are 3-stated to reduce EMC and allow for combinations with

other ICs. If output is desired, it has to be activated by means of an I<sup>2</sup>C-bus command.

When output is enabled, serial audio data can be taken from pin SDO. Depending on the signal source, switch and matrix positions, the output can be either mono, stereo or dual language.

The Word Select output (WS) is clocked with the audio sample frequency of 32 kHz. The Serial Clock output (SCK) is clocked at a frequency of 2.048 MHz. This means, that there are 64 clock pulses per pair of stereo output samples, or 32 clock pulses per sample. There are 18 significant bits used on the Serial Data Output (SDO).

A symmetrical system clock output (SYSCLK) is available from the TDA9874H as a master clock for external digital audio devices. At power-up, the clock is off. It can be enabled and the output frequency set via an I<sup>2</sup>C-bus command. Available output frequencies are 8.192 MHz, 12.288 MHz, 16.384 MHz and 24.576 MHz.



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9 EXTERNAL COMPONENTS

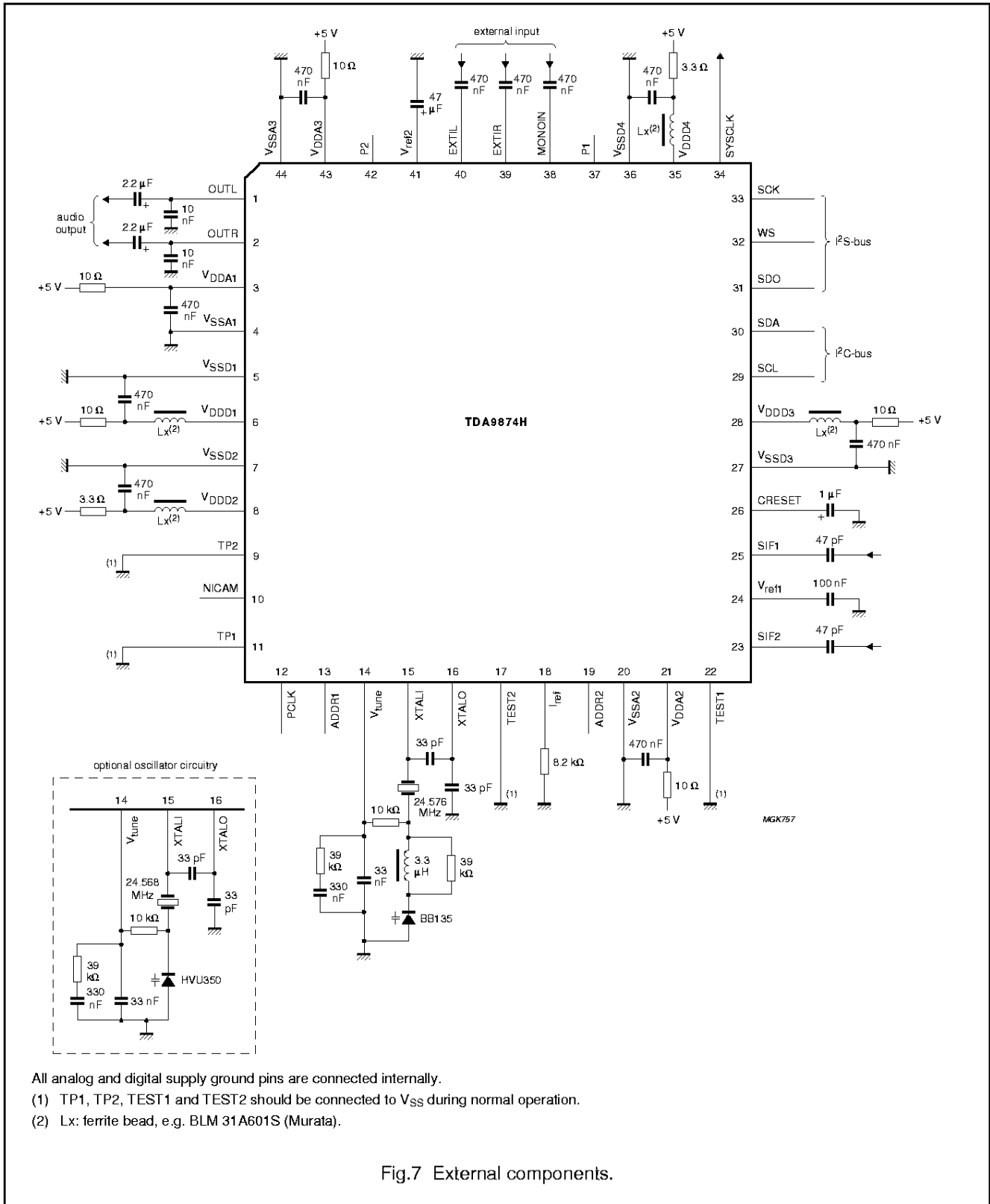


Fig.7 External components.

## Digital TV sound demodulator/decoder

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**10 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD}$	DC supply voltage		-0.5	+6.5	V
$\Delta V_{DD}$	voltage differences between two $V_{DD}$ pins		-	550	mV
$I_{IK}$	DC input clamp diode current	$V_i < -0.5$ V or $V_i > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$I_{OK}$	DC output clamp diode current output type 4 mA	$V_o < -0.5$ V or $V_o > V_{DD} + 0.5$ V	-	$\pm 20$	mA
$I_o$	DC output source or sink current output type 4 mA	$-0.5$ V $< V_o < V_{DD} + 0.5$ V	-	$\pm 20$	mA
$I_{DDD}, I_{SSD}$	DC $V_{DDD}$ or $V_{SSD}$ current per digital supply pin		-	$\pm 62$	mA
$I_{DDA}, I_{SSA}$	DC $V_{DDA}$ or $V_{SSA}$ current per analog supply pin		-	$\pm 28$	mA
$I_{lu(prot)}$	latch-up protection current		100	-	mA
P	power dissipation per output		-	100	mW
$P_{tot}$	total power dissipation		-	0.9	W
$T_{stg}$	storage temperature		-55	+125	°C
$T_{amb}$	operating ambient temperature		-20	+70	°C
$V_{es}$	electrostatic handling	note 1	2000	-	V
		note 2	200	-	V

**Notes**

- Human body model: C = 100 pF; R = 1.5 k $\Omega$ .
- Machine model: C = 200 pF; L = 0.75  $\mu$ H; R = 0  $\Omega$ .

**11 THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

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**12 CHARACTERISTICS**

$V_{DD} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; settings in accordance with B/G standard; FM deviation  $\pm 50\text{ kHz}$ ;  $f_{mod} = 1\text{ kHz}$ ; FM sound parameters in accordance with system A2; NICAM in accordance with "EBU specification";  $1\text{ k}\Omega$  measurement source resistance for AF inputs;  $V_{SIF} = 300\text{ mV}$  (peak-to-peak);  $AGCOFF = 0$ ;  $AGCSLOW = 1$ ; level and gain settings according to note 2 with external components of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Digital supplies</b>						
$V_{DDD1}$	digital supply voltage 1		4.5	5.0	5.5	V
$V_{SSD1}$	digital ground supply 1		-	0.0	-	V
$I_{DDD1}$	digital supply current 1	$V_{DDD1} = 5.5\text{ V}$	8	12	16	mA
		$V_{DDD1} = 5.0\text{ V}$	7	10	14	mA
$V_{DDD2}$	digital supply voltage 2		4.5	5.0	5.5	V
$V_{SSD2}$	digital ground supply 2		-	0.0	-	V
$I_{DDD2}$	digital supply current 2	$V_{DDD2} = 5.5\text{ V}$	25	32	37	mA
		$V_{DDD2} = 5.0\text{ V}$	22	28	33	mA
$V_{DDD3}$	digital supply voltage 3		4.5	5.0	5.5	V
$V_{SSD3}$	digital ground supply 3		-	0.0	-	V
$I_{DDD3}$	digital supply current 3	$V_{DDD3} = 5.5\text{ V}$	7	12	16	mA
		$V_{DDD3} = 5.0\text{ V}$	6	11	15	mA
<b>Demodulator supplies and references</b>						
$V_{DDA2}$	analog supply voltage 2, demodulator part		4.5	5.0	5.5	V
$V_{SSA2}$	analog ground supply 2, demodulator part		-	0.0	-	V
$I_{DDA2}$	analog supply current 2, demodulator part	$V_{DDA} = 5.5\text{ V}$	20	24	28	mA
		$V_{DDA} = 5.0\text{ V}$	17	21.5	25	mA
$V_{DDD4}$	digital supply voltage 4		4.5	5.0	5.5	V
$V_{SSD4}$	digital ground supply 4		-	0.0	-	V
$I_{DDD4}$	digital supply current 4	$V_{DDD2} = 5.5\text{ V}$	40	50	60	mA
		$V_{DDD2} = 5.0\text{ V}$	34	44	54	mA
$V_{ref1}$	analog reference voltage 1, demodulator part	with respect to $V_{DDA2}/V_{SSA2}$	35	50	65	%
$I_{ref(sink)}$	$V_{ref1}$ sink current		170	220	260	$\mu\text{A}$
<b>Audio supplies and references</b>						
$V_{DDA3}$	analog supply voltage 3, operational amplifiers		4.5	5.0	5.5	V
$V_{SSA3}$	analog ground supply 3, operational amplifiers		-	0.0	-	V
$I_{DDA3}$	analog supply current 3, operational amplifiers	$V_{DDA} = 5.5\text{ V}$	1.3	1.8	2.4	mA
		$V_{DDA} = 5.0\text{ V}$	1.2	1.7	2.3	mA
$V_{DDA1}$	analog supply voltage 1, audio DAC part		4.5	5.0	5.5	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>SSA1</sub>	analog ground supply 1, audio DAC part		–	0.0	–	V
I <sub>DDA1</sub>	analog supply current 1, audio DAC part	V <sub>DDA</sub> = 5.5 V; digital silence	1.2	2.1	3.1	mA
		V <sub>DDA</sub> = 5.0 V; digital silence	1.1	1.9	2.8	mA
V <sub>ref2</sub>	reference voltage 2, audio DACs and operational amplifiers	with respect to V <sub>DDA3</sub> /V <sub>SSA3</sub>	–	50	–	%
Z <sub>(Vref2-VDDA3)</sub>	impedance V <sub>ref2</sub> to V <sub>DDA3</sub>		–	20	–	kΩ
Z <sub>(Vref2-VSSA3)</sub>	impedance V <sub>ref2</sub> to V <sub>SSA3</sub>		–	20	–	kΩ
<b>Digital inputs and outputs</b>						
INPUTS						
<i>CMOS level input, high drive, pull-down (TEST1, TEST2, TP1 and TP2)</i>						
V <sub>IL</sub>	LOW-level input voltage		–	–	1.6	V
V <sub>IH</sub>	HIGH-level input voltage		3.0	–	–	V
C <sub>i</sub>	input capacitance		–	–	10	pF
Z <sub>i</sub>	input impedance		–	50	–	kΩ
<i>CMOS level input, hysteresis, high drive, pull-up (CRESET)</i>						
V <sub>IL</sub>	LOW-level input voltage		–	–	1.0	V
V <sub>IH</sub>	HIGH-level input voltage		4.0	–	–	V
V <sub>hys</sub>	hysteresis voltage		–	0.33V <sub>DD</sub>	–	V
C <sub>i</sub>	input capacitance		–	–	10	pF
Z <sub>i</sub>	input impedance		–	50	–	kΩ
INPUTS/OUTPUTS						
<i>I<sup>2</sup>C level input with Schmitt trigger, open-drain output stage (SCL and SDA)</i>						
V <sub>IL</sub>	LOW-level input voltage		–	–	1.6	V
V <sub>IH</sub>	HIGH-level input voltage		3.0	–	–	V
V <sub>hys</sub>	hysteresis voltage		–	0.33V <sub>DD</sub>	–	V
I <sub>LI</sub>	input leakage current		–	–	±10	μA
C <sub>i</sub>	input capacitance		–	–	10	pF
V <sub>OL</sub>	LOW-level output voltage		–	–	0.5	V
C <sub>L</sub>	load capacitance	active pull-up	–	–	400	pF
		passive pull-up	–	–	200	pF
<i>TTL/CMOS level, high drive, 4 mA 3-state output stage, pull-up (PCLK, NICAM, ADDR1, ADDR2, P1, P2, SCK, WS and SDO)</i>						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.8	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	–	–	V
C <sub>i</sub>	input capacitance		–	–	10	pF
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = +3 mA	–	–	0.5	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –3 mA	2.9	–	–	V
C <sub>L</sub>	load capacitance	active pull-up	–	–	50	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_i$	input impedance		–	50	–	$k\Omega$
<b>OUTPUTS</b>						
<i>4 mA 3-state output stage (SYSCLK)</i>						
$V_{OL}$	LOW-level output voltage	$I_{OL} = +2 \text{ mA}$	–	–	0.5	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -2 \text{ mA}$	2.9	–	–	V
$C_L$	load capacitance		–	–	50	pF
$I_{LIZ}$	3-state leakage current	$V_i = 0 \text{ to } V_{DD}$	–	–	$\pm 10$	$\mu\text{A}$
<b>SIF1 and SIF2 analog inputs</b>						
$V_{SIF(p-p)}$	composite SIF input voltage range (peak-to-peak value)	note 5	60	–	700	mV
$f_i$	input frequency		4	–	9.2	MHz
$R_i$	input resistance		10	13	16	$k\Omega$
$C_i$	input capacitance		–	7.5	11	pF
$\Delta f_{FM}$	FM deviation	B/G standard; THD < 1%	$\pm 100$	–	–	kHz
$\Delta f_{FM(FS)}$	FM deviation full-scale level	terrestrial FM; level adjust 0 dB	$\pm 150$	–	–	kHz
$C/N_{FM}$	FM carrier $C/N_c$ ratio	$N_{FM}$ bandwidth = 6 MHz; white noise for S/N = 40 dB; "CCIR468-2"; quasi peak	–	77	–	$\frac{\text{dB}_{FM}}{\text{Hz}}$
$C/N_N$	NICAM carrier $C/N_c$ ratio	$N_c$ bandwidth = 6 MHz; bit error rate = $10^{-3}$ ; white noise	–	66	–	$\frac{\text{dB}_N}{\text{Hz}}$
<b>Demodulator performance</b>						
$V_{o(nom)}(\text{RMS})$	nominal level output voltage (RMS value)	note 2	400	500	600	mV
THD + N	total harmonic distortion + noise	from FM source to any output with low-pass 30 kHz/3 dB; $V_o = 1 \text{ V (RMS)}$	–	0.3	0.5	%
		from NICAM source to any output with low-pass 30 kHz/3 dB; $V_o = 1 \text{ V (RMS)}$	–	0.1	0.3	%
S/N	signal-to-noise ratio	SC1 from FM source to any output; $V_o = 1 \text{ V (RMS)}$ ; "CCIR468-2"; quasi peak; TIMPOL bit HIGH	61	65	–	dB
		SC2 from FM source to any output; $V_o = 1 \text{ V (RMS)}$ ; "CCIR468-2"; quasi peak; TIMPOL bit HIGH	57	60	–	dB
		NICAM source; $V_o = 1 \text{ V (RMS)}$ ; "CCIR468-2"; quasi peak	NICAM in accordance with "EBU specification"; note 1			

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$B_{(-3dB)}$	-3 dB bandwidth	from FM source to any output	14.5	15	-	kHz
		from NICAM source to any output	14.5	15	-	kHz
$f_{resp}$	frequency response 20 Hz to 14 kHz	from FM/NICAM to any output; reference 1 kHz	-2	-	+1	dB
$\alpha_{cd(dual)}$	dual signal channel separation	note 6	65	70	-	dB
$\alpha_{cs(stereo)}$	stereo channel separation	note 7	40	45	-	dB
$\alpha_{AM}$	AM suppression for FM	AM: 1 kHz, 30% modulation; reference: 1 kHz, 50 kHz deviation	50	-	-	dB
$dm_{AM}$	AM demodulation	SIF level 100 mV (RMS); 54% AM; 1 kHz AF; "CCIR468"; quasi peak	-	36	-	dB
<b>IDENTIFICATION FOR FM SYSTEMS</b>						
$m_{pilot(ident)}$	pilot modulation for identification		25	50	75	%
$C/N_{pilot(ident)}$	pilot sideband C/N for identification start		-	32	-	dB Hz
$hys_{(tun)}$	hysteresis		-	-	2	dB
$f_{ident}$	identification window	B/G stereo				
		slow mode	116.85	-	118.12	Hz
		medium mode	116.11	-	118.89	Hz
		fast mode	114.65	-	120.46	Hz
		B/G dual				
		slow mode	273.44	-	274.81	Hz
medium mode	272.07	-	276.20	Hz		
fast mode	270.73	-	277.60	Hz		
$t_{on(ident)}$	total identification time on	slow mode	-	-	2	s
		medium mode	-	-	1	s
		fast mode	-	-	0.5	s
$t_{off(ident)}$	total identification time off	slow mode	-	-	2	s
		medium mode	-	-	1	s
		fast mode	-	-	0.5	s
<b>Mono and external inputs</b>						
$V_{i(nom)(rms)}$	nominal level input voltage (RMS value)	note 2	-	500	-	mV
$V_{i(cl)(rms)}$	clipping level input voltage (RMS value)	THD < 3%; note 3	1250	1400	-	mV
$R_i$	input resistance	note 3	28	35	42	k $\Omega$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Analog audio outputs</b>						
$V_{o(\text{clip})(\text{rms})}$	clipping level output voltage (RMS value)	THD < 3%	1400	–	–	mV
$R_o$	output resistance		150	250	375	$\Omega$
$R_{L(\text{AC})}$	AC load resistor		10	–	–	k $\Omega$
$R_{L(\text{DC})}$	DC load resistor		10	–	–	k $\Omega$
$C_{o(L)}$	output load capacitor		–	10	12	nF
$V_{\text{offset}(\text{DC})}$	static DC offset voltage		–	30	70	mV
$\alpha_{\text{mute}}$	mute suppression	nominal input signal from any source; $f_i = 1$ kHz; note 2	80	–	–	dB
$B_{\text{line}}$	bandwidth	from external and mono source; –3 dB bandwidth	20	–	–	kHz
$G_{\text{ro}}$	roll-off gain at 14.5 kHz	from any source	–3	–2	–	dB
PSRR	power supply ripple rejection	$f_{\text{ripple}} = 70$ Hz; $V_{\text{ripple}} = 100$ mV (peak); $C_{\text{Vref}} = 47$ $\mu$ F; signal from I <sup>2</sup> S	40	45	–	dB
<b>Audio performance</b>						
THD + N	total harmonic distortion + noise	$V_{\text{in/out}} = 1$ V (RMS); $f_i = 1$ kHz; bandwidth 20 Hz to 20 kHz; from external/mono input to output copy	–	0.1	0.3	%
S/N	signal-to-noise ratio	reference voltage $V_0 = 1.4$ V (RMS); $f_i = 1$ kHz; "CCIR468"; quasi peak; from external/mono input to output copy	78	90	–	dB
$\alpha_{\text{ct}}$	crosstalk attenuation	between any analog input pairs; $f_i = 1$ kHz	70	–	–	dB
$\alpha_{\text{cs}}$	channel separation	between left and right of external input pair	65	–	–	dB
		between left and right of output pair	60	–	–	dB
<b>VCXO and clock generation</b>						
VCXO						
<i>Crystal input</i>						
$C_i$	input capacitance		–	–	10	pF
$V_{\text{bias}(\text{DC})}$	DC bias voltage	$R_i = 100$ k $\Omega$	3.5	3.63	3.7	V
<i>Crystal output</i>						
$V_{\text{osc}(\text{p-p})}$	oscillation amplitude (peak-to-peak value)		–	1.4	–	V
$V_{\text{bias}(\text{DC})}$	DC bias voltage		2.3	2.53	2.8	V
$G_m$	mutual conductance at 24.576 MHz		16.6	17.6	18.8	mS



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_o$	output capacitance		–	–	10	pF
CRYSTAL SPECIFICATION (FUNDAMENTAL MODE)						
$f_{\text{xtal}}$	crystal frequency	note 4	–	24.576	–	MHz
$C_L$	load capacitance		–	20	–	pF
$C_1$	series capacitance		–	20	–	fF
$C_0$	parallel capacitance		–	–	7	pF
S	pulling sensitivity	$C_L$ changed from 18 to 16 pF	–	25	–	$\frac{10^{-6}}{\text{pF}}$
$R_{s(\text{eq})}$	equivalent series resistance	at nominal frequency	–	–	30	$\Omega$
$R_{s(\text{eq})(\text{UM})}$	equivalent series resistance of unwanted mode		$2R_R$	–	–	$\Omega$
$T_{\text{amb}}$	operating ambient temperature		–20	+25	+70	$^{\circ}\text{C}$
$X_J$	adjustment tolerance		–	–	$\pm 30$	$10^{-6}$
$X_D$	drift	across temperature range	–	–	$\pm 30$	$10^{-6}$
$X_A$	ageing		–	–	$\pm 5$	$\frac{10^{-6}}{\text{year}}$

**Notes**

- Audio performance is limited by the dynamic range of the NICAM 728 system. Due to companding, the quantization noise is never lower than –62 dB with respect to the input level.
- Definition of levels and level setting (see Tables 75 and 76):
  - The full-scale level for analog audio signals is  $V_{\text{FS}} = 1.4 \text{ V (RMS)}$ . The nominal level at the digital crossbar switch is defined at –15 dB (FS).
  - Nominal audio input levels: extern, mono: 500 mV (RMS); –9 dB (FS).
- If the supply voltage for the TDA9874H is switched off, because of the ESD protection circuitry all audio input pins are short-circuited.
- The Philips crystal (order number 9922 520 20106) is suited for this application.
- The demodulation/decoding is still functional above and below the limits given.
- FM source; in dual mode only A (respectively B) signal modulated; measured at B (respectively A) channel output;  $V_o = 1 \text{ V (RMS)}$  of modulated channel.
- FM source; in stereo mode only L (respectively R) signal modulated; measured at R (respectively L) channel output;  $V_o = 1 \text{ V (RMS)}$  of modulated channel.

Level setting FM, AM and NICAM  
 = 1.4 V (RMS), FS means full scale.

	<b>TRANSMITTER NOMINAL MODULATION DEPTH</b>	<b>NOMINAL LEVEL AT DEMODULATOR OUTPUT</b>	<b>LEVEL ADJUST SETTING</b>	<b>NOMINAL LEVEL AT CROSSBAR</b>	<b>DAC GAIN SETTING</b>	<b>NOMINAL OUTPUT VOLTAGE <math>V_o</math></b>
	15 kHz deviation	-24 dB (FS)	+9 dB	-15 dB (FS) (spread of $\pm 0.5$ dB due to different transmitter references)	+6 dB	500 mV (RMS)
	27 kHz deviation	-19 dB (FS)	+4 dB			
	54%	-19 dB (FS)	+4 dB			
	-11.2 dB (FS)	-18 dB (FS)	+3 dB			
	-15.8 dB (FS)	-23 dB (FS)	+8 dB			

Level setting SAT FM  
 = 1.4 V (RMS), FS means full scale.

	<b>TRANSMITTER MAXIMUM MODULATION DEPTH</b>	<b>NOMINAL LEVEL AT DEMODULATOR OUTPUT</b>	<b>LEVEL ADJUST SETTING</b>	<b>MAXIMUM LEVEL AT CROSSBAR</b>	<b>DAC GAIN SETTING</b>	<b>MAXIMUM OUTPUT VOLTAGE <math>V_o</math></b>
	50 kHz deviation	-13 dB (FS)	+4 dB	-9 dB (FS)	+6 dB	1 V (RMS)
	85 kHz deviation	-9 dB (FS)	0 dB			

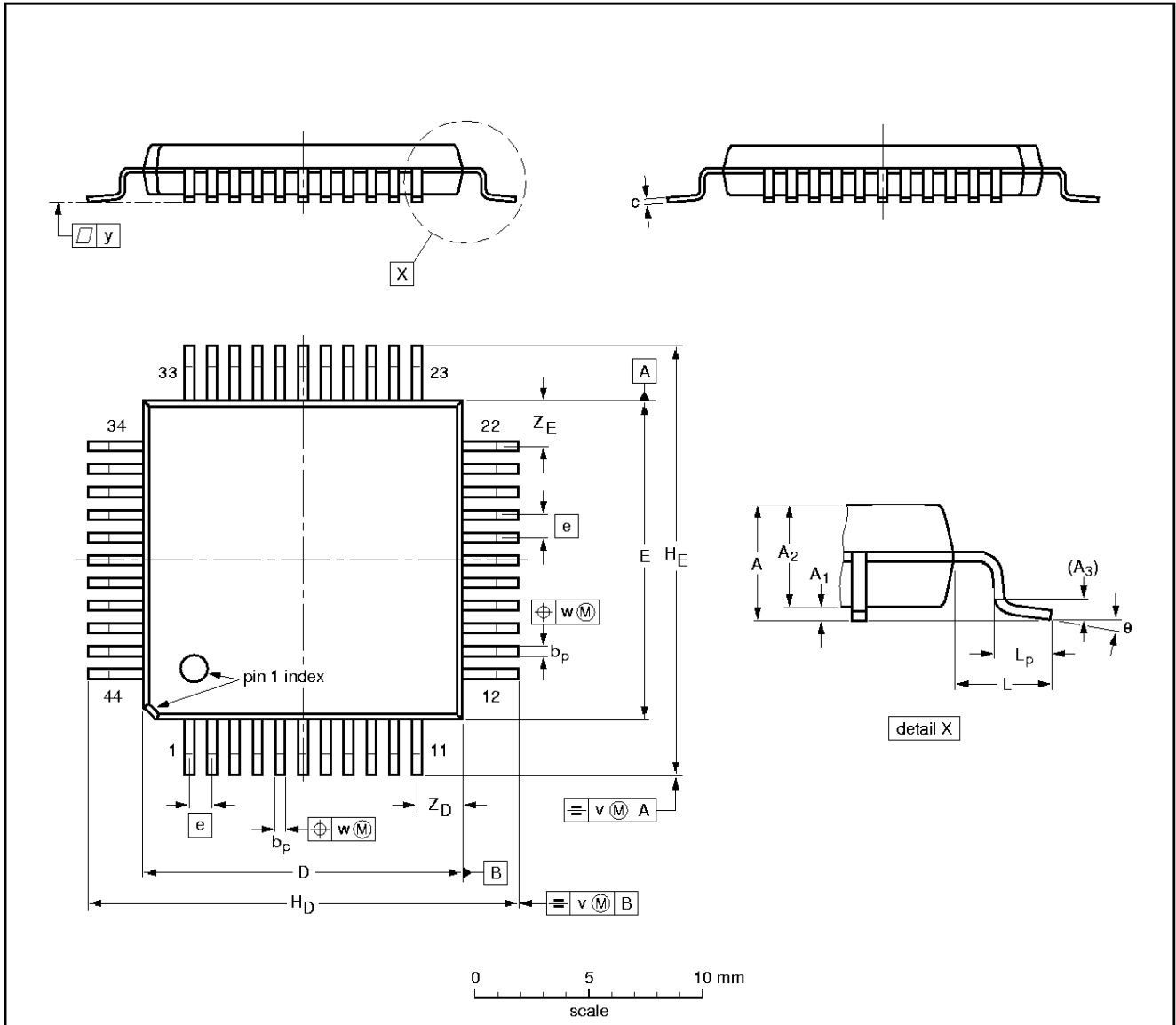
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13 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm

SOT205-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sub>max.</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT205-1	133E01A				95-02-04 97-08-01

## Digital TV sound demodulator/decoder

## TDA9874H

**14 SOLDERING****14.1 Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (order code 9398 652 90011).

**14.2 Reflow soldering**

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

**14.3 Wave soldering**

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**CAUTION**

**Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.**

**If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**14.4 Repairing soldered joints**

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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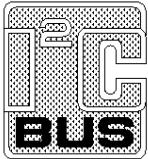
**15 DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**16 LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

**17 PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS**

	<p>Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.</p>
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**NOTES**

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**NOTES**

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Printed in The Netherlands

545104/1200/01/pp56

Date of release: 1998 Apr 27

Document order number: 9397 750 02597

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