

## CURRENT MODE PWM CONTROLLER

### FEATURES

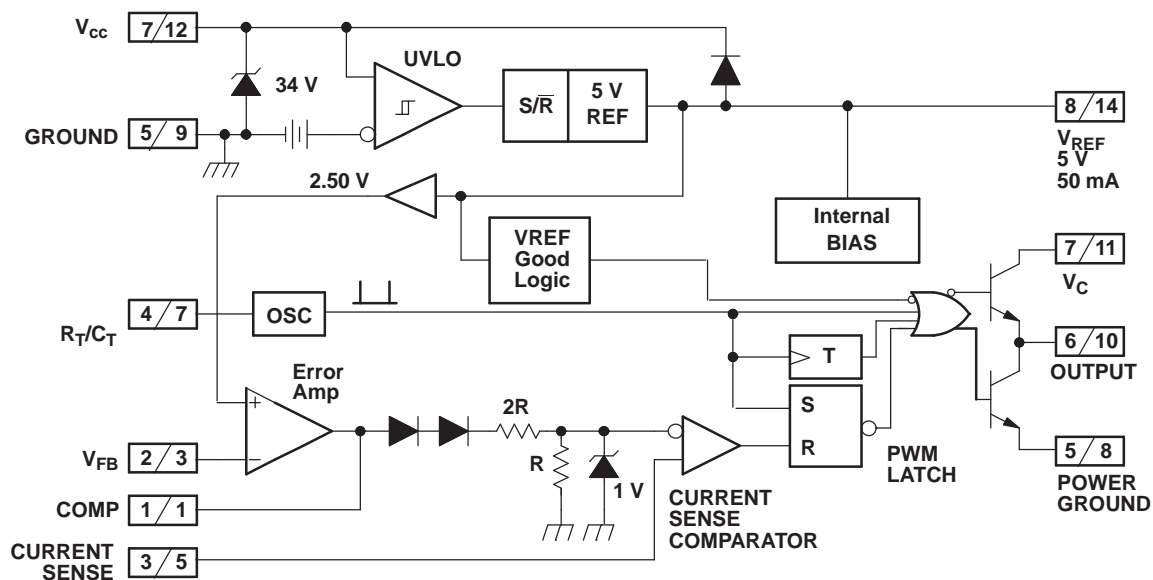
- Optimized For Off-line and DC-to-DC Converters
- Low Start-Up Current (<1 mA)
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500-kHz Operation
- Low  $R_O$  Error Amp

### DESCRIPTION

The UC1842/3/4/5 family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of  $16 V_{ON}$  and  $10 V_{OFF}$ , ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4 V and 7.6 V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

### BLOCK DIAGRAM



Note 1: **A/B** A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.

Note 2: Toggle flip flop used only in 1844 and 1845.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

		UNIT
Supply voltage	Low impedance source	30 V
	$I_{CC} < 30 \text{ mA}$	Self Limiting
Output current		$\pm 1 \text{ A}$
Output energy (capacitive load)		5 $\mu\text{J}$
Analog inputs (Pins 2, 3)		-0.3 V to 6.3 V
Error amp output sink current		10 mA
Power dissipation	$T_A \leq 25^\circ\text{C}$ (DIL-8)	1 W
	$T_A \leq 25^\circ\text{C}$ (SOIC-14)	725 mW
	$T_A \leq 25^\circ\text{C}$ (SOIC-8)	650 mW
Storage temperature range		-65°C to 150°C
Junction temperature range		-55°C to 150°C
Lead temperature (soldering, 10 seconds)		300°C

(1) All voltages are with respect to Pin 5. All currents are positive into the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

**CONNECTION DIAGRAMS**



NC – No internal connection



## THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PACKAGE		$\theta_{JC}$	$\theta_{JA}$
DIL-8	J	28 <sup>(1)</sup>	125-160
	N	25	110 <sup>(2)</sup>
SOIC-8	D8	42	84-160 <sup>(2)</sup>
SOIC-14	D14	35	50-120 <sup>(2)</sup>
CFP-14	W	5.49°C/W	175.4C/W
PLCC-20	Q	34	43-75 <sup>(2)</sup>

(1)  $\theta_{JC}$  data values stated were derived from MIL-STD-1835B.

(2) Specified  $\theta_{JA}$  (junction to ambient) is for devices mounted to 5 in<sup>2</sup> FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in<sup>2</sup>. Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with 100 x 100-mil probe land area at the end of each trace.

## DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A \leq 25^\circ\text{C}$	$T_A \leq 70^\circ\text{C}$ POWER RATING	$T_A \leq 85^\circ\text{C}$ CPO WER RATING	$T_A \leq 125^\circ\text{C}$ POWER RATING
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for  $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$  for the UC184X;  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$  for the UC284X;  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$  for the 384X;  $V_{CC} = 15\text{ V}^{(1)}$ ;  $R_T = 10\text{ k}\Omega$ ;  $C_T = 3.3\text{ nF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>REFERENCE SECTION</b>								
Output Voltage	$T_J = 25^\circ\text{C}$ , $I_O = 1\text{ mA}$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25\text{ V}$		6	20		6	20	mV
Load Regulation	$1 \leq I_O \leq 20\text{ mA}$		6	25		6	25	
Temp. Stability	See <sup>(2)(3)</sup>		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, load, temperature <sup>(2)</sup>	4.9		5.1	4.82		5.18	V
Output Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$ , $T_J = 25^\circ\text{C}^{(2)}$		50			50		$\mu\text{V}$
Long Term Stability	$T_A = 125^\circ\text{C}$ , 1000 Hrs <sup>(2)</sup>		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
<b>OSCILLATOR SECTION</b>								
Initial Accuracy	$T_J = 25^\circ\text{C}^{(4)}$	47	52	57	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{ V}$		0.2%	1%		0.2%	1%	
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}^{(2)}$		5%			5%		
Amplitude	$V_{PIN\ 4}$ peak-to-peak <sup>(2)</sup>		1.7			1.7		V

(1) Adjust  $V_{CC}$  above the start threshold before setting at 15 V.

(2) These parameters, although specified, are not 100% tested in production.

(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF(max)} - V_{REF(min)}}{T_{J(max)} - T_{J(min)}}$$

$V_{REF(max)}$  and  $V_{REF(min)}$  are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(4) Output frequency equals oscillator frequency for the UC1842 and UC1843.

Output frequency is one half oscillator frequency for the UC1844 and UC1845.

## ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  for the UC184X;  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for the UC284X;  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$  for the 384X;  $V_{CC} = 15\text{ V}$ ;  $R_T = 10\text{ k}\Omega$ ;  $C_T = 3.3\text{ nF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ERROR AMP SECTION</b>								
Input Voltage	$V_{PIN\ 1} = 2.5\text{ V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	$\mu\text{A}$
$A_{VOL}$	$2 \leq V_O \leq 4\text{ V}$	65	90		65	90		dB
Unity Gain Bandwidth	$T_J = 25^{\circ}\text{C}$ <sup>(5)</sup>	0.7	1		0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{ V}$	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2} = 2.7\text{ V}$ , $V_{PIN\ 1} = 1.1\text{ V}$	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2} = 2.3\text{ V}$ , $V_{PIN\ 1} = 5\text{ V}$	-0.5	-0.8		-0.5	-0.8		
$V_{OUT\ High}$	$V_{PIN\ 2} = 2.3\text{ V}$ , $R_L = 15\text{ k}\Omega$ to ground	5	6		5	6		V
$V_{OUT\ Low}$	$V_{PIN\ 2} = 2.7\text{ V}$ , $R_L = 15\text{ k}\Omega$ to Pin 8		0.7	1.1		0.7	1.1	
<b>CURRENT SENSE SECTION</b>								
Gain	See <sup>(6)</sup> / <sup>(7)</sup>	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1} = 5\text{ V}$ <sup>(6)</sup>	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{ V}$ <sup>(5)</sup> / <sup>(6)</sup>		70			70		dB
Input Bias Current			-2	-10		-2	-10	$\mu\text{A}$
Delay to Output	$V_{PIN\ 3} = 0\text{ V}$ to $2\text{ V}$ <sup>(5)</sup>		150	300		150	300	ns
<b>OUTPUT SECTION</b>								
Output Low Level	$I_{SINK} = 20\text{ mA}$		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 200\text{ mA}$		1.5	2.2		1.5	2.2	
Output High Level	$I_{SOURCE} = 20\text{ mA}$	13	13.5		13	13.5		
	$I_{SOURCE} = 200\text{ mA}$	12	13.5		12	13.5		
Rise Time	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{ nF}$ <sup>(5)</sup>		50	150		50	150	ns
Fall Time	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{ nF}$ <sup>(5)</sup>		50	150		50	150	
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	
<b>PWM SECTION</b>								
Maximum Duty Cycle	X842/3	95%	97%	100%	95%	97%	100%	
	X844/5	46%	48%	50%	47%	48%	50%	
Minimum Duty Cycle				0%			0%	
<b>TOTAL STANDBY CURRENT</b>								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3} = 0\text{ V}$		11	17		11	17	
$V_{CC}$ Zener Voltager	$I_{CC} = 25\text{ mA}$	30	34		30	34		V

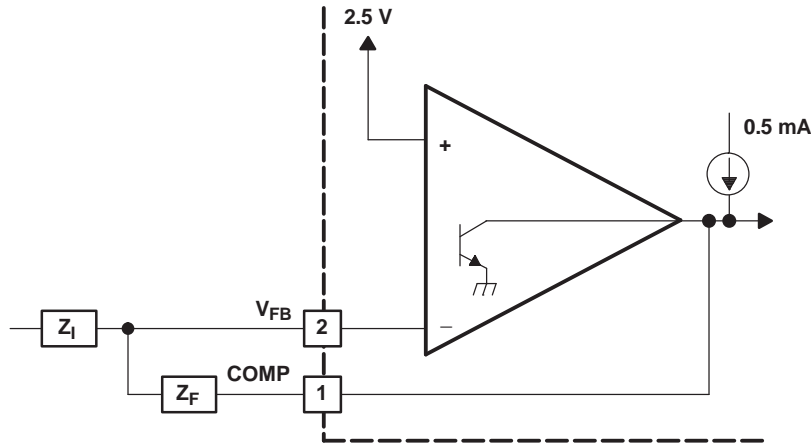
(5) These parameters, although specified, are not 100% tested in production.

(6) Parameter measured at trip point of latch with  $V_{PIN\ 2} = 0$ .

(7) Gain defined as:  $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$ ,  $0 \leq V_{PIN\ 3} \leq 0.8\text{ V}$

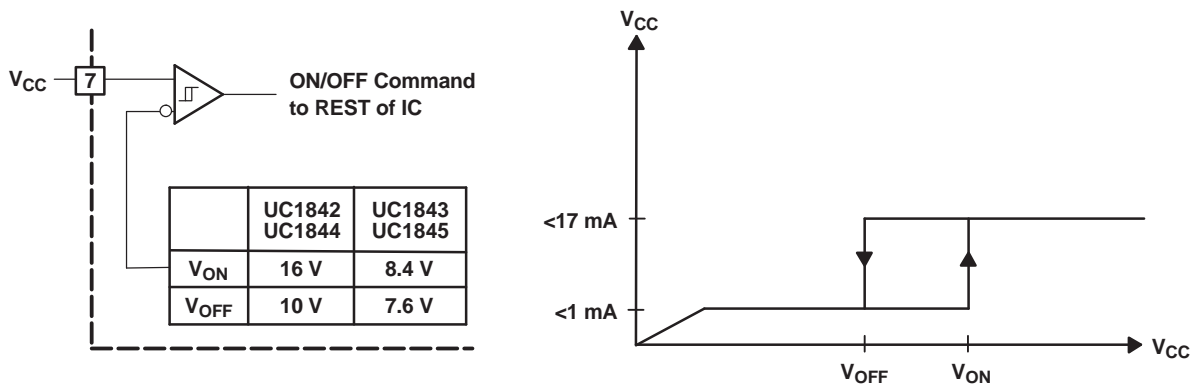
## ERROR AMP CONFIGURATION

Error amp can source or sink up to 0.5 mA.



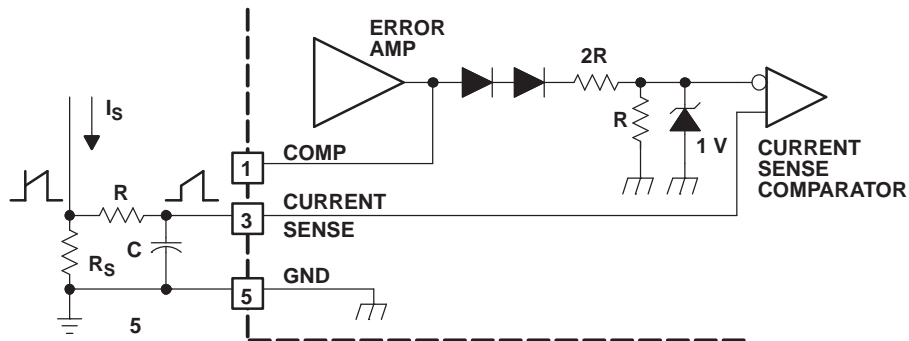
## UNDER-VOLTAGE LOCKOUT

During under-voltage lock-out, the output drive is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.



## CURRENT SENSE CIRCUIT

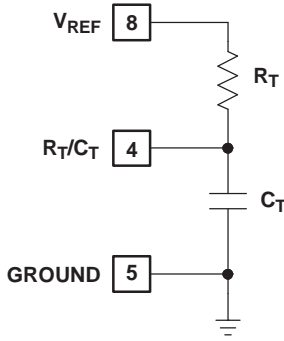
A small RC filter may be required to suppress switch transients.



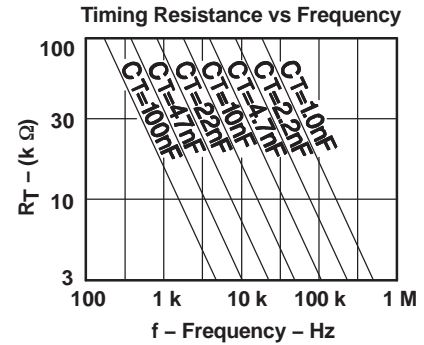
Peak Current ( $I_s$ ) is Determined By The Formula

$$I_{S\text{MAX}} = \frac{1.0 \text{ V}}{R_S}$$

**OSCILLATOR SECTION**



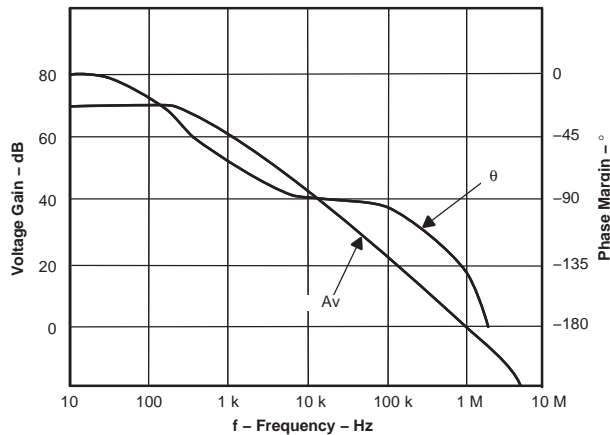
For  $R_T > 5 \text{ K} f \sim \frac{1.72}{R_T C_T}$



**OUTPUT SATURATION CHARACTERISTICS**

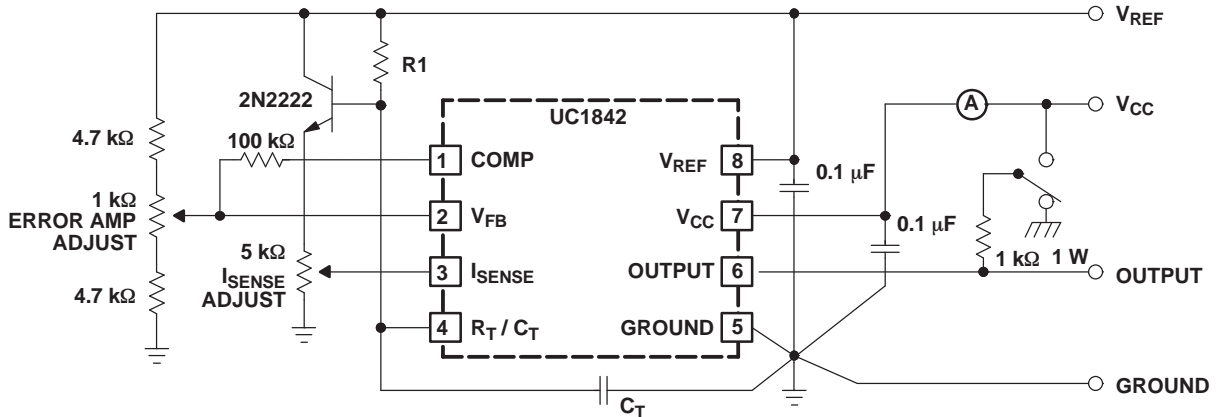


**ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE**



## OPEN-LOOP LABORATORY FIXTURE

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

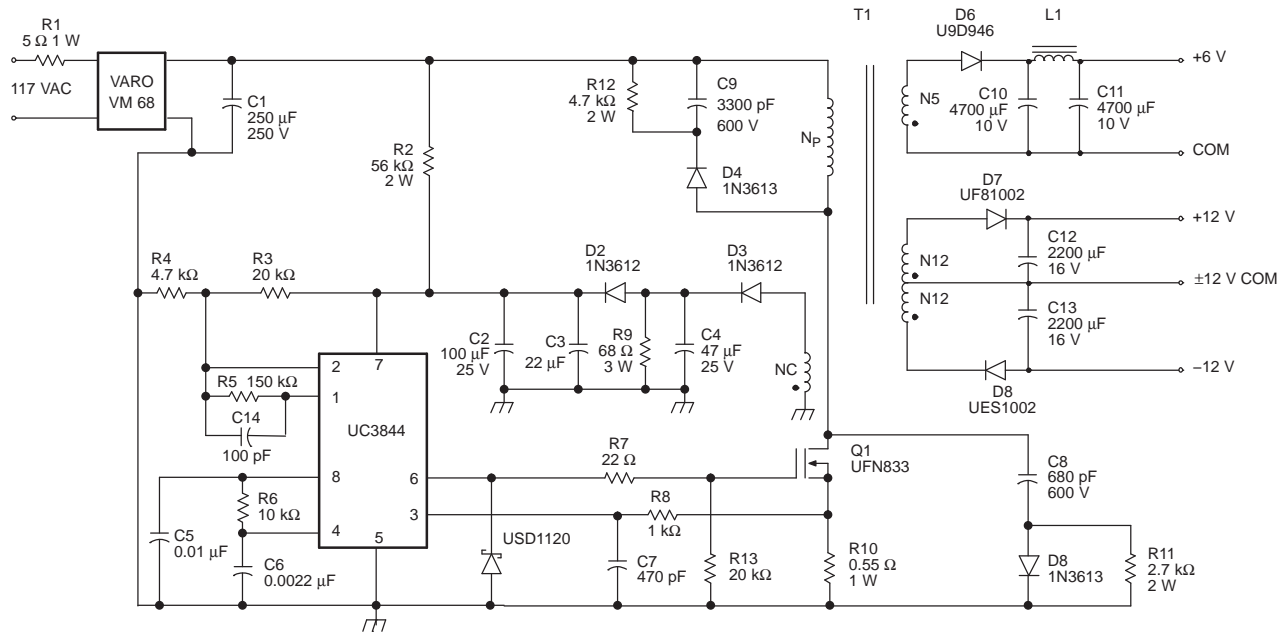


## SHUTDOWN TECHNIQUES

Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling  $V_{CC}$  below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.



## OFFLINE FLYBACK REGULATOR

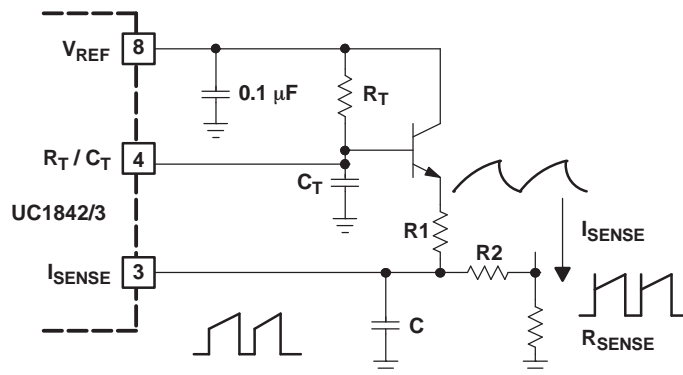


### Power Supply Specifications

1. Input Voltages
  - a. 5VAC to 130VA (50 Hz/60 Hz)
2. Line Isolation: 3750 V
3. Switchng Frequency: 40 kHz
4. Efficiency at Full Load 70%
5. Output Voltage:
  - a. +5 V,  $\pm 5\%$ ; 1A to 4A load  
Ripple voltage: 50 mV P-P Max
  - b. +12 V,  $\pm 3\%$ ; 0.1A to 0.3A load  
Ripple voltage: 100 mV P-P Max
  - c. -12 V,  $\pm 3\%$ ; 0.1A to 0.3A load  
Ripple voltage: 100 mV P-P Max

### SLOPE COMPENSATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8670401PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670401PA UC1842	<a href="#">Samples</a>
5962-8670401VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670401VPA UC1842	<a href="#">Samples</a>
5962-8670401VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670401VXA UC1842L QMLV	<a href="#">Samples</a>
5962-8670401XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670401XA UC1842L/ 883B	<a href="#">Samples</a>
5962-8670402PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670402PA UC1843	<a href="#">Samples</a>
5962-8670402XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670402XA UC1843L/ 883B	<a href="#">Samples</a>
5962-8670403PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670403PA UC1844	<a href="#">Samples</a>
5962-8670403VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670403VPA UC1844	<a href="#">Samples</a>
5962-8670403VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670403VXA UC1844L QMLV	<a href="#">Samples</a>
5962-8670403XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670403XA UC1844L/ 883B	<a href="#">Samples</a>
5962-8670404DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type		5962-8670404DA UC1845W/883B	<a href="#">Samples</a>
5962-8670404PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670404PA UC1845	<a href="#">Samples</a>
5962-8670404VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type		8670404VPA UC1845	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8670404VXA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670404VXA UC1845L QMLV	<a href="#">Samples</a>
5962-8670404XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670404XA UC1845L/ 883B	<a href="#">Samples</a>
UC1842J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1842J	<a href="#">Samples</a>
UC1842J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670401PA UC1842	<a href="#">Samples</a>
UC1842L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670401XA UC1842L/ 883B	<a href="#">Samples</a>
UC1842W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1842W	<a href="#">Samples</a>
UC1843J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1843J	<a href="#">Samples</a>
UC1843J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670402PA UC1843	<a href="#">Samples</a>
UC1843L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1843L	<a href="#">Samples</a>
UC1843L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670402XA UC1843L/ 883B	<a href="#">Samples</a>
UC1843W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1843W	<a href="#">Samples</a>
UC1844J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1844J	<a href="#">Samples</a>
UC1844J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670403PA UC1844	<a href="#">Samples</a>
UC1844L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670403XA UC1844L/ 883B	<a href="#">Samples</a>
UC1845J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1845J	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1845J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670404PA UC1845	<a href="#">Samples</a>
UC1845L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1845L	<a href="#">Samples</a>
UC1845L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8670404XA UC1845L/ 883B	<a href="#">Samples</a>
UC1845W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1845W	<a href="#">Samples</a>
UC1845W883B	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type		5962-8670404DA UC1845W/883B	<a href="#">Samples</a>
UC2842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842D	<a href="#">Samples</a>
UC2842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842 D8	<a href="#">Samples</a>
UC2842D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842 D8	<a href="#">Samples</a>
UC2842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842 D8	<a href="#">Samples</a>
UC2842D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842 D8	<a href="#">Samples</a>
UC2842DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842D	<a href="#">Samples</a>
UC2842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842D	<a href="#">Samples</a>
UC2842J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-40 to 85		
UC2842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2842N	<a href="#">Samples</a>
UC2842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2842N	<a href="#">Samples</a>
UC2843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843D	<a href="#">Samples</a>
UC2843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843 D8	<a href="#">Samples</a>
UC2843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843 D8	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843 D8	<a href="#">Samples</a>
UC2843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843 D8	<a href="#">Samples</a>
UC2843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843D	<a href="#">Samples</a>
UC2843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843D	<a href="#">Samples</a>
UC2843DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843D	<a href="#">Samples</a>
UC2843J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-40 to 85		
UC2843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2843N	<a href="#">Samples</a>
UC2843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2843N	<a href="#">Samples</a>
UC2844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844D	<a href="#">Samples</a>
UC2844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844 D8	<a href="#">Samples</a>
UC2844D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844 D8	<a href="#">Samples</a>
UC2844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844 D8	<a href="#">Samples</a>
UC2844D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844 D8	<a href="#">Samples</a>
UC2844DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844D	<a href="#">Samples</a>
UC2844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844D	<a href="#">Samples</a>
UC2844DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844D	<a href="#">Samples</a>
UC2844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2844N	<a href="#">Samples</a>
UC2844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2844N	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	<a href="#">Samples</a>
UC2845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845 D8	<a href="#">Samples</a>
UC2845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845 D8	<a href="#">Samples</a>
UC2845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845 D8	<a href="#">Samples</a>
UC2845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845 D8	<a href="#">Samples</a>
UC2845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	<a href="#">Samples</a>
UC2845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	<a href="#">Samples</a>
UC2845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845D	<a href="#">Samples</a>
UC2845J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-40 to 85		
UC2845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2845N	<a href="#">Samples</a>
UC2845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2845N	<a href="#">Samples</a>
UC3842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842D	<a href="#">Samples</a>
UC3842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842 D8	<a href="#">Samples</a>
UC3842D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842 D8	<a href="#">Samples</a>
UC3842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842 D8	<a href="#">Samples</a>
UC3842D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842 D8	<a href="#">Samples</a>
UC3842DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842D	<a href="#">Samples</a>
UC3842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842D	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3842N	<a href="#">Samples</a>
UC3842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3842N	<a href="#">Samples</a>
UC3843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D	<a href="#">Samples</a>
UC3843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D8	<a href="#">Samples</a>
UC3843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D8	<a href="#">Samples</a>
UC3843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D8	<a href="#">Samples</a>
UC3843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D8	<a href="#">Samples</a>
UC3843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D	<a href="#">Samples</a>
UC3843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D	<a href="#">Samples</a>
UC3843DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843D	<a href="#">Samples</a>
UC3843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3843N	<a href="#">Samples</a>
UC3843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3843N	<a href="#">Samples</a>
UC3843QTR	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	0 to 70		
UC3844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D	<a href="#">Samples</a>
UC3844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D8	<a href="#">Samples</a>
UC3844D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D8	<a href="#">Samples</a>
UC3844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D8	<a href="#">Samples</a>
UC3844D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D8	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3844DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D	<a href="#">Samples</a>
UC3844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D	<a href="#">Samples</a>
UC3844DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844D	<a href="#">Samples</a>
UC3844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3844N	<a href="#">Samples</a>
UC3844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3844N	<a href="#">Samples</a>
UC3845AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	0 to 70	UC3845AJ	<a href="#">Samples</a>
UC3845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	<a href="#">Samples</a>
UC3845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D8	<a href="#">Samples</a>
UC3845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D8	<a href="#">Samples</a>
UC3845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D8	<a href="#">Samples</a>
UC3845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D8	<a href="#">Samples</a>
UC3845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	<a href="#">Samples</a>
UC3845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	<a href="#">Samples</a>
UC3845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845D	<a href="#">Samples</a>
UC3845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3845N	<a href="#">Samples</a>
UC3845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3845N	<a href="#">Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1842, UC1842-SP, UC1843, UC1844, UC1844-SP, UC1845, UC1845-SP, UC3842, UC3843, UC3844, UC3845, UC3845AM :**

● Catalog: [UC3842](#), [UC1842](#), [UC3843](#), [UC3844](#), [UC1844](#), [UC3845](#), [UC1845](#), [UC3842M](#), [UC3845A](#)

● Military: [UC1842](#), [UC1843](#), [UC1844](#), [UC1845](#)

● Space: [UC1842-SP](#), [UC1843-SP](#), [UC1844-SP](#), [UC1845-SP](#)

NOTE: Qualified Version Definitions:



- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2845DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3845DTR	SOIC	D	14	2500	333.2	345.9	28.6

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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