# PRELIMINARY DATA SHEET

# gm5221-LF-BC
# Integrated Multimedia LCD Controller

GENESIS MICROCHIP CONFIDENTIAL

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# 1 Overview

The gm5200 family devices are an all-in-one LCD monitor controllers supporting resolutions up to SXGA (1280x1024). The gm5221 leverages Genesis patented advanced image-processing technology as well as a proven integrated ADC/PLL and an Ultra-Reliable DVI™ compliant digital receiver to provide excellent image quality. gm5221 also integrates a microcontroller, an OSD controller, and dual LVDS transmitters.

## 1.1 gm5221 System Design Example

Figure 1 below shows a typical dual interface LCD monitor system based on the gm5221. Designs based on the gm5221 have reduced system cost, simplified hardware and firmware design and increased reliability because only a minimal number of components are required in the system.

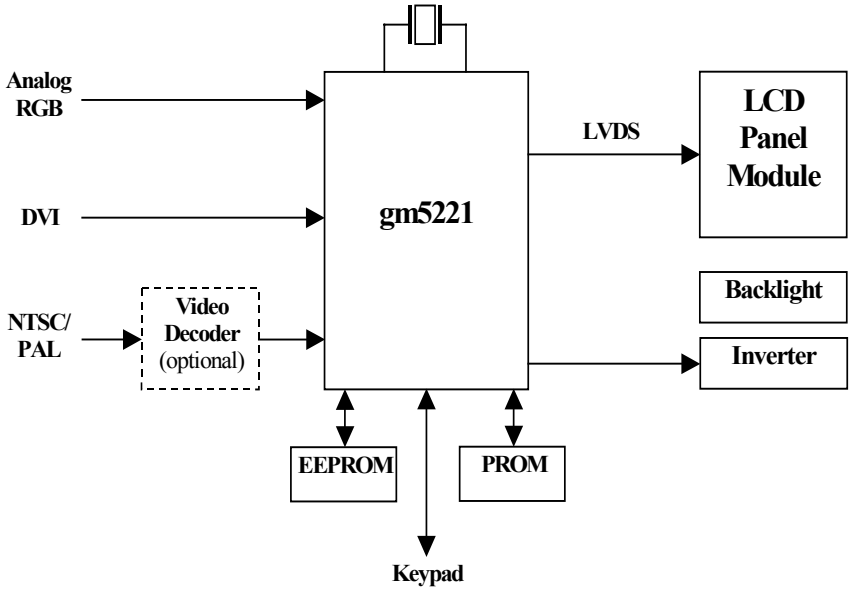


**Figure 1. gm5221 System Design Example**

## 1.2 gm5221 Features

- **Intelligent Image Processing™**
  - Fully programmable zoom ratios
  - High-quality shrink capability from UXGA resolution
  - Programmable coefficients for variable sharpness control
  - RealRecovery™ provides full color recovery image for refresh rates higher than those supported by the LCD panel
- **Analog RGB Input Port**
  - Supports up to 162 MHz (SXGA 75Hz / UXGA 60Hz)
  - On-chip high-performance PLLs (single reference crystal required)
  - Composite-sync and Sync-on-Green (SOG) support
  - Input format detection
  - Phase and image positioning
- **Ultra-Reliable DVI-Compliant Input Port**
  - Operating up to 165 MHz (up to UXGA 60Hz)
  - Direct connect to all DVI 1.0-compliant transmitters
  - High-bandwidth Digital Content Protection (HDCP) **Note:** HDCP function is available H version only.
- **CCIR-656 8-bit Video Input Port**
  - Supporting NTSC / PAL interlaced and progressive
  - Direct connect to commercially available video decoders
  - Spatial de-interlacing
- **Advanced Color Management**
  - Programmable gamma correction (CLUT)
  - TV color controls including hue and saturation controls
  - Full color matrix allows end-users to experience the same colors as viewed on CRTs and other displays (e.g. sRGB compliance)
  - Advanced Active Color Management ™ (ACM-II) provide flesh-tone compensation and image enhancement
  - Adaptive Contrast and Color™ (ACC) ensures full dynamic range is used in video content
- **On-chip Versatile OSD Controller**
  - On-chip RAM for high-quality programmable menus
  - 1, 2 and 4-bit per pixel character cells
  - Horizontal and vertical stretch of OSD menus
  - Blinking, transparency and blending
  - Supports two independent OSD menu rectangles
  - Proportional fonts
- **Embedded X86 On-chip Microcontroller**
  - High-performance X86 MCU with on-chip RAM and ROM
  - External parallel ROM or serial SPI ROM interface
  - Unified memory architecture simplifies chip programming
  - 23 general-purpose inputs/outputs (GPIOs) available
  - 2-wire serial bus master to control NVRAM, video decoder
  - Two DDC2Bi ports with DMA buffer to internal RAM
  - Four PWM outputs for analog backlight control, audio, etc.
  - General-purpose ADC's for keypad and temperature sensing
  - Integrated reset circuit
  - Slow clock mode for 50mW sleep mode power consumption
  - JTAG debug / ICE support for firmware debugging
- **Built-in Test Pattern Generator**
  - Simplifies manufacturing / test
- **Energy Spectrum Management (ESM™)**
  - Digital clock spectrum management
  - Eliminates EMI suppression components and shielding
- **Built-in LVDS Transmitters**
  - Four channel 6/8-bit LVDS transmitter
  - Support for 8 or 6-bit panels with high-quality dithering
  - Single / double wide up to SXGA 75Hz output
  - Pin swap, odd / even swap and red / blue group swap of RGB outputs for flexibility in board layout
- **Highly integrated System-on-a-Chip**
  - All system clocks synthesized from a single external crystal
  - 50mW power saving mode
  - 5-Volt tolerant inputs
  - Two Layer PCB support
  - On-chip reset feature to eliminate external reset component
  - Integrated Schmitt trigger for HSYNC and VSYNC

### PACKAGE

- 208-pin PQFP
- 3.3V IO and 1.8V core power supplies

# 2 gm5221 Pinout

The gm5221 devices are packaged in a 208-pin Plastic Quad Flat Pack (PQFP).

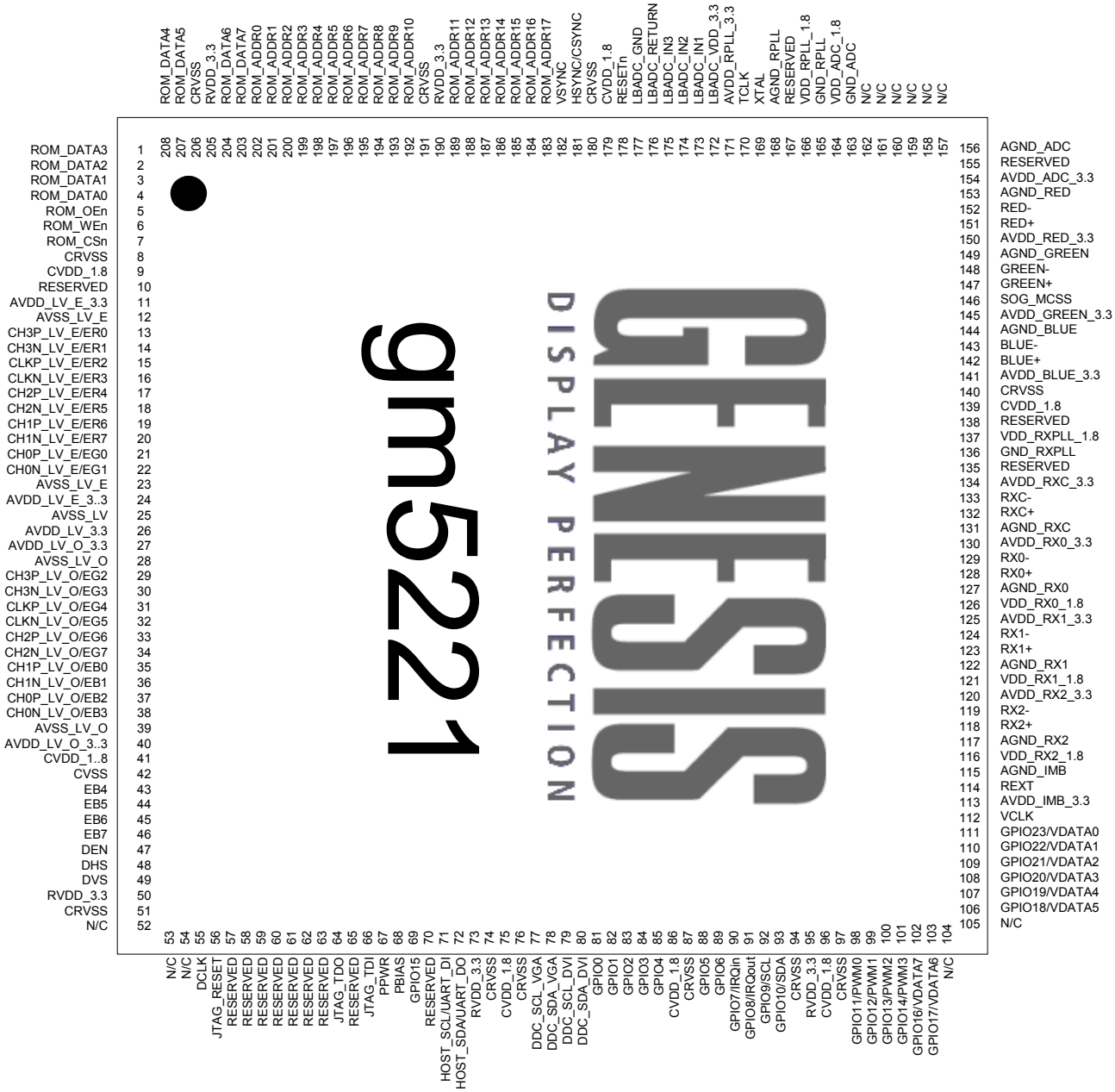


**Figure 2. gm5221 Pin Out Diagram**

# 3 gm5221 Pin List

**I/O Legend: A** = Analog, **I** = Input, **O** = Output, **P** = Power, **G** = Ground, **N/C** = No connect inside chip.

**Table 1. Analog Input Port**

| Pin Name | No | I/O | Description |
|---|---|---|---|
| AVDD_BLUE_3.3 | 141 | AP | Analog power (3.3V) for the blue channel. Must be bypassed with capacitor to AGND_BLUE pin on system board. |
| BLUE+ | 142 | AI | Positive analog input for Blue channel. |
| BLUE- | 143 | AI | Negative analog input for Blue channel. |
| AGND_BLUE | 144 | AG | Analog ground for the blue channel. Must be directly connected to the analog system ground plane. |
| AVDD_GREEN_3.3 | 145 | AP | Analog power (3.3V) for the green channel. Must be bypassed with capacitor to AGND_GREEN pin on system board. |
| SOG_MCSS | 146 | I | Dedicated Sync-on-Green pin.<br>**NOTE**: This pin requires the same AC-couple capacitor (if applicable) like the regular RGB input pins. See 4.3.5 |
| GREEN+ | 147 | AI | Positive analog input for Green channel. |
| GREEN- | 148 | AI | Negative analog input for Green channel.<br>**NOTE**: For SOG support this pin should be pulled down to GND through a 1MΩ resistor. See 4.3.5 |
| AGND_GREEN | 149 | AG | Analog ground for the green channel. Must be directly connected to the analog system ground plane. |
| AVDD_RED_3.3 | 150 | AP | Analog power (3.3V) for the red channel. Must be bypassed with capacitor to AGND_RED pin on system board. |
| RED+ | 151 | AI | Positive analog input for Red channel. |
| RED- | 152 | AI | Negative analog input for Red channel. |
| AGND_RED | 153 | AG | Analog ground for the red channel. Must be directly connected to the analog system ground plane. |
| AVDD_ADC_3.3 | 154 | AG | Analog power (3.3V) for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be bypassed with capacitor to AGND_ADC pin on system board. |
| AGND_ADC | 156 | AG | Analog ground for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be directly connected to analog system ground plane. |
| GND1_ADC | 163 | AG | Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane |
| VDD1_ADC_1.8 | 164 | AP | Digital power (1.8V) for ADC encoding logic. Must be bypassed with capacitor to GND1_ADC pin on system board. |
| HSYNC/CSYNC | 181 | I | ADC input horizontal sync or composite sync input.<br>[Input, Schmitt trigger with 1V hysteresis and 1.65V threshold, 5V-tolerant] |
| VSYNC | 182 | I | ADC input vertical sync.<br>[Input, Schmitt trigger with 1V hysteresis and 1.65V threshold, 5V-tolerant] |

**Table 2. DVI Input Port**

| Pin Name | No | I/O | Description |
|---|---|---|---|
| AVDD_IMB_3.3 | 113 | AP | Analog VDD (3.3V) for internal biasing circuits. Must be bypassed with capacitors |
| REXT | 114 | AI | External termination resistor.<br>A 1% 250Ω resistor should be connected from this pin to AVDD_IMB. |
| AGND_IMB | 115 | AG | Analog GND for internal biasing circuits. Must be connected directly to the ground plane. |
| VDD_RX2_1.8 | 116 | AP | VDD (1.8V) for TMDS input pair 2.<br>Must be bypassed with external capacitor to GND_RX2. |
| AGND_RX2 | 117 | AG | Analog GND for TMDS input pair 2. Must be connected directly to the analog ground plane. |
| RX2+ | 118 | AI | TMDS input pair 2 |
| RX2- | 119 | AI | TMDS input pair 2 |
| AVDD_RX2_3.3 | 120 | AP | Analog VDD (3.3V) for TMDS input pair 2. Must be bypassed with capacitor to AGND_RX2. |
| VDD_RX1_1.8 | 121 | AP | VDD (1.8V) for TMDS input pair 2. Must be bypassed with external capacitor to GND_RX1. |
| AGND_RX1 | 122 | AG | Analog GND for TMDS input pair 1. Must be connected directly to the analog ground plane. |
| RX1+ | 123 | AI | TMDS input pair 1 |

| Pin Name | No | I/O | Description |
|---|---|---|---|
| RX1- | 124 | AI | TMDS input pair 1 |
| AVDD_RX1_3.3 | 125 | AP | Analog VDD (3.3V) for TMDS input pair 2. Must be bypassed with to AGND_RX1. |
| VDD_RX0_1.8 | 126 | AP | VDD (1.8V) for TMDS input pair 2. Must be bypassed with external capacitor to GND_RX0. |
| AGND_RX0 | 127 | AG | Analog GND for TMDS input pair 0. Must be connected directly to the analog ground plane. |
| RX0+ | 128 | AI | TMDS input pair 0 |
| RX0- | 129 | AI | TMDS input pair 0 |
| AVDD_RX0_3.3 | 130 | AP | Analog VDD (3.3V) for TMDS input pair 2. Must be bypassed with capacitor to AGND_RX0. |
| AGND_RXC | 131 | AG | Analog GND for TMDS input clock pair. Must be connected directly to the analog ground plane. |
| RXC+ | 132 | AI | TMDS input clock pair |
| RXC- | 133 | AI | TMDS input clock pair |
| AVDD_RXC_3.3 | 134 | AP | Analog VDD (3.3V) for TMDS input clock pair.<br>Must be bypassed with 100pF capacitor to AGND_RXC. |
| GND_RXPLL | 136 | AG | Analog GND for the TMDS receiver internal PLL.<br>Must be connected directly to the analog ground plane. |
| VDD_RXPLL_1.8 | 137 | AP | Analog VDD (1.8V) for the TMDS receiver internal PLL.<br>Must be bypassed with a capacitor to AGND_RXPLL. |
| CLK_OUT | 138 | AO | Reserved. Leave unconnected. |

**Table 3. RCLK PLL Pins**

| Pin Name | No | I/O | Description |
|---|---|---|---|
| GND_RPLL | 165 | AG | Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane. |
| VDD_RPLL_1.8 | 166 | AP | Digital power (1.8V) for ADC digital logic. Must be bypassed with capacitor to GND1_ADC. |
| AGND_RPLL | 168 | AG | Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane. |
| XTAL | 169 | AO | Crystal oscillator output. |
| TCLK | 170 | AI | Reference clock (TCLK) from the 14.3MHz crystal oscillator. |
| AVDD_RPLL_3.3 | 171 | AP | Analog VDD (3.3V) |

**Table 4. Input Video Port**

| Pin Name | No | I/O | Description |
|---|---|---|---|
| VCLK | 112 | I | Video port data clock input. Up to 75Mhz<br>[Input, 5V-tolerant] |
| GPIO23/VDATA0<br>GPIO22/VDATA1<br>GPIO21/VDATA2<br>GPIO20/VDATA3<br>GPIO19/VDATA4<br>GPIO18/VDATA5<br>GPIO17/VDATA6<br>GPIO16/VDATA7 | 111<br>110<br>109<br>108<br>107<br>106<br>103<br>102 | IO | Input YUV data in 8-bit BT656 or GPIO23:16 if VPORT is disabled.<br>[Bi-Directional, 5V-tolerant] |

**Table 5. System Interface**

| Pin Name | No | I/O | Description |
|---|---|---|---|
| GPIO0<br>GPIO1<br>GPIO2<br>GPIO3<br>GPIO4<br>GPIO5<br>GPIO6 | 81<br>82<br>83<br>84<br>85<br>88<br>89 | IO | General-purpose input/output signals<br>[Bi-directional, Schmitt trigger, 5V-tolerant] |
| GPIO7/IRQin<br>GPIO8/IRQout | 90<br>91 | | General-purpose input/output signal [Bi-directional, Schmitt trigger, 5V-tolerant] or OCM interrupt and chip status. |
| GPIO9/SCL<br>GPIO10/SDA | 92<br>93 | IO | General-purpose input/output signals [Bi-directional, Schmitt trigger, 5V-tolerant] or master device on serial interface bus. |
| GPIO11/PWM0<br>GPIO12/PWM1<br>GPIO13/PWM2<br>GPIO14/PWM3 | 98<br>99<br>100<br>101 | IO | General-purpose input/output signal or PWM signals.<br>[Bi-directional, Schmitt trigger, 5V-tolerant] |
| GPIO15 | 69 | IO | General-purpose input/output signal [Bi-directional, Schmitt trigger, 5V-tolerant] |
| DDC_SCL_VGA<br>DDC_SDA_VGA | 77<br>78 | IO | DDC2Bi clock for VGA Port<br>DDC2Bi data for VGA Port [internal 10KΩ pull-up resistor] |
| DDC_SCL_DVI<br>DDC_SDA_DVI | 79<br>80 | IO | DDC2Bi and HDCP clock for DVI Port<br>DDC2Bi and HDCP data for DVI Port [internal 10KΩ pull-up resistor] |
| RESETn | 178 | IO | Hardware Reset (active low) [Schmitt trigger, 5v-tolerant]<br>Connect to ground with 0.01uF (or larger) capacitor. See section, Chip Initialization, for detail |
| LBADC_VDD_3.3 | 172 | AP | Analog 3.3V power supply for general-purpose ADC |
| LBADC_IN1 | 173 | AI | LBADC channel 1 |
| LBADC_IN2 | 174 | AI | LBADC channel 2 |
| LBADC_IN3 | 175 | AI | LBADC channel 3 |
| LBADC_RETURN | 176 | AG | Analog Ground (signal return path) for LBADC channels 1, 2 and 3 |
| LBADC_GND | 177 | AG | Ground |
| HOST_SCL/UART_DI | 71 | IO | Host input clock or 186 UART Data In or JTAG clock signal.<br>[Input, Schmitt trigger, 5V-tolerant] |
| HOST_SDA/UART_DO | 72 | IO | Host input data or 186 UART Data Out or JTAG mode signal.<br>[Bi-directional, Schmitt trigger, slew rate limited, 5V-tolerant] |
| JTAG_TDI | 66 | IO | JTAG data input signal. |
| JTAG_TDO | 64 | IO | JTAG data output signal. |
| JTAG_RESET | 56 | IO | JTAG reset signal. |

**Table 6. LVDS Display Interface**

| Pin Name | No | I/O | Description |
|---|---|---|---|
| AVDD_LV_E_3.3 | 11 | AP | Digital Power for LVDS outputs. Connect to digital 3.3V supply. |
| AVSS_LV_E | 12 | AG | Ground for LVDS outputs. |
| CH3P_LV_E | 13 | O | |
| CH3N_LV_E | 14 | O | |
| CLKP_LV_E | 15 | O | |
| CLKN_LV_E | 16 | O | |
| CH2P_LV_E | 17 | O | |
| CH2N_LV_E | 18 | O | |
| CH1P_LV_E | 19 | O | |
| CH1N_LV_E | 20 | O | |
| CH0P_LV_E | 21 | O | |
| CH0N_LV_E | 22 | O | |
| AVSS_LV_E | 23 | AG | Ground for LVDS outputs. |
| AVDD_LV_E_3.3 | 24 | AP | Digital Power for LVDS outputs. Connect to digital 3.3V supply. |
| AVSS_LV | 25 | AG | Ground for LVDS outputs. |
| AVDD_LV_3.3 | 26 | AP | Analog Power for LVDS outputs. Connect to analog 3.3V supply. |
| AVDD_LV_O_3.3 | 27 | AP | Digital Power for LVDS outputs. Connect to digital 3.3V supply. |
| AVSS_LV_O | 28 | AG | Ground for LVDS outputs. |
| CH3P_LV_O | 29 | O | |
| CH3N_LV_O | 30 | O | |
| CLKP_LV_O | 31 | O | |
| CLKN_LV_O | 32 | O | |
| CH2P_LV_O | 33 | O | |
| CH2N_LV_O | 34 | O | |
| CH1P_LV_O | 35 | O | |
| CH1N_LV_O | 36 | O | |
| CH0P_LV_O | 37 | O | |
| CH0N_LV_O | 38 | O | |
| AVSS_LV_O | 39 | AG | Ground for LVDS outputs. |
| AVDD_LV_O_3.3 | 40 | AP | Digital Power for LVDS outputs. Connect to digital 3.3V supply. |
| PPWR | 67 | O | Panel Power Control [Tri-state output, 5V- tolerant] |
| PBIAS | 68 | O | Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant] |
| RESERVED | 43 | O | Reserved. Leave unconnected. |
| RESERVED | 44 | O | Reserved. Leave unconnected. |
| RESERVED | 45 | O | Reserved. Leave unconnected. |
| RESERVED | 46 | O | Reserved. Leave unconnected. |
| RESERVED | 47 | O | Reserved. Leave unconnected. (Display Enable for TTL interface) |
| RESERVED | 48 | O | Reserved. Leave unconnected. (Display Horizontal Sync for TTL interface) |
| RESERVED | 49 | O | Reserved. Leave unconnected. (Display Vertical Sync for TTL interface) |

**Table 7. TTL Display Interface**

| Pin Name | No | I/O | Description | |
|---|---|---|---|---|
| | | | For 8-bit panels | For 6-bit panels |
| AVDD_LV_E_3.3 | 11 | AP | Analog Power for TTL outputs. Connect to analog 3.3V supply. | |
| AVSS_LV_E | 12 | AG | Ground | |
| ER0 | 13 | O | Red channel bit 0 | Not used. |
| ER1 | 14 | O | Red channel bit 1 | Not used. |
| ER2 | 15 | O | Red channel bit 2 | Red channel bit 0 |
| ER3 | 16 | O | Red channel bit 3 | Red channel bit 1 |
| ER4 | 17 | O | Red channel bit 4 | Red channel bit 2 |
| ER5 | 18 | O | Red channel bit 5 | Red channel bit 3 |
| ER6 | 19 | O | Red channel bit 6 | Red channel bit 4 |
| ER7 | 20 | O | Red channel bit 7 | Red channel bit 5 |
| EG0 | 21 | O | Green channel bit 0 | Not used. |
| EG1 | 22 | O | Green channel bit 1 | Not used. |
| AVSS_LV_E | 23 | AG | Ground for TTL outputs. | |
| AVDD_LV_E_3.3 | 24 | AP | Digital Power for TTL outputs. Connect to digital 3.3V supply. | |
| AVSS_LV | 25 | AG | Ground for TTL outputs. | |

| Pin Name | No | I/O | Description<br>For 8-bit panels | For 6-bit panels |
|---|---|---|---|---|
| AVDD_LV_3.3 | 26 | AP | Digital Power for TTL outputs. Connect to digital 3.3V supply. | |
| AVDD_LV_O_3.3 | 27 | AP | Digital Power for TTL outputs. Connect to digital 3.3V supply. | |
| AVSS_LV_O | 28 | AG | Ground for TTL outputs. | |
| EG2 | 29 | O | Green channel bit 2 | Green channel bit 0 |
| EG3 | 30 | O | Green channel bit 3 | Green channel bit 1 |
| EG4 | 31 | O | Green channel bit 4 | Green channel bit 2 |
| EG5 | 32 | O | Green channel bit 5 | Green channel bit 3 |
| EG6 | 33 | O | Green channel bit 6 | Green channel bit 4 |
| EG7 | 34 | O | Green channel bit 7 | Green channel bit 5 |
| EB0 | 35 | O | Blue channel bit 0 | Not used. |
| EB1 | 36 | O | Blue channel bit 1 | Not used. |
| EB2 | 37 | O | Blue channel bit 2 | Blue channel bit 0 |
| EB3 | 38 | O | Blue channel bit 3 | Blue channel bit 1 |
| AVSS_LV_O | 39 | AG | Ground | |
| AVDD_LV_O_3.3 | 40 | AP | Digital Power for TTL outputs. Connect to digital 3.3V supply. | |
| EB4 | 43 | O | Blue channel bit 4 | Blue channel bit 2 |
| EB5 | 44 | O | Blue channel bit 5 | Blue channel bit 3 |
| EB6 | 45 | O | Blue channel bit 6 | Blue channel bit 4 |
| EB7 | 46 | O | Blue channel bit 7 | Blue channel bit 5 |
| DEN | 47 | O | Display Enable. | |
| DHS | 48 | O | Display Horizontal Sync. | |
| DVS | 49 | O | Display Vertical Sync. | |
| DCLK | 55 | O | Display Pixel Clock | |
| PPWR | 67 | O | Panel Power Control [Tri-state output, 5V- tolerant] | |
| PBIAS | 68 | O | Panel Bias Control (backlight enable) [Tri-state output, 5V- tolerant] | |

**Note:** TTL bus is single pixel per clock only.

# 4 Functional Description

A functional block diagram is illustrated below. Each of the functional units shown is described in the following sections.

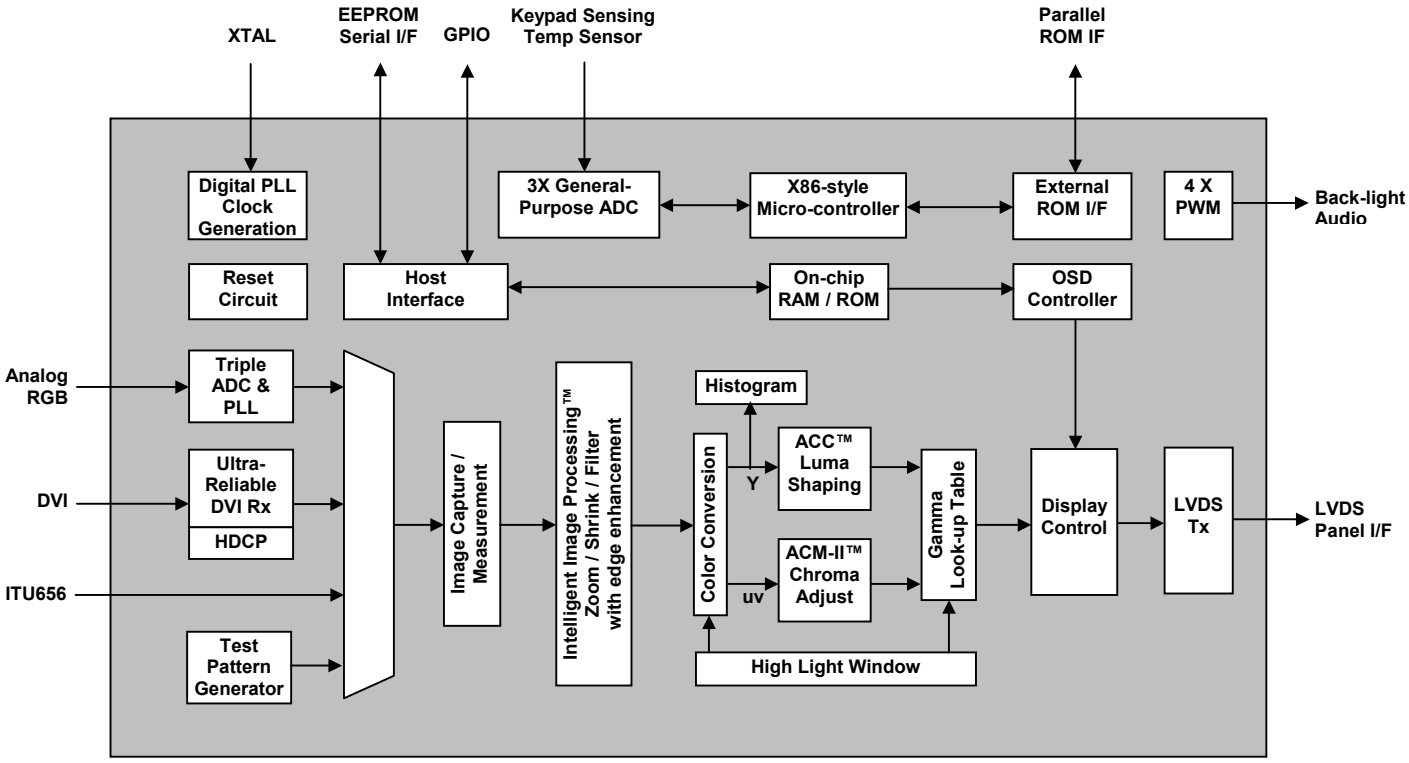


**Figure 3. gm5221 Functional Block Diagram**

## 4.1 Clock Generation

The gm5221 features three clock inputs. All additional clocks are internal clocks derived from one or more of these:

1. Crystal Input Clock (TCLK and XTAL). This is the input pair to an internal crystal oscillator and corresponding logic. A 14.3 MHz TV crystal is recommended. Other crystal frequencies may be used, but require custom programming. This is illustrated in Figure 4 below.
2. DVI Differential Input Clock (RC+ and RC-)
3. Video Clock (VCLK)

### 4.1.1 Using the Internal Oscillator with External Crystal

An external crystal is used with an internal clock oscillator to provide a clock reference for the device. 14, 20, and 24 MHz crystals are supported.

The oscillator circuit is designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the chip. An Automatic Gain Control (AGC) is used to insure startup and operation over a wide range of conditions. The oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

The state of the ROM_ADDR13 pin is sampled at reset (see section 4.14). If the pin is left unconnected (internal pull-down) then internal oscillator is enabled. In this mode a crystal resonator is connected between TCLK and the XTAL with the appropriately sized loading capacitors $C_{L1}$ and $C_{L2}$. The size of $C_{L1}$ and $C_{L2}$ are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the device and the printed circuit board traces. The loading capacitors are terminated to the analog VDD power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

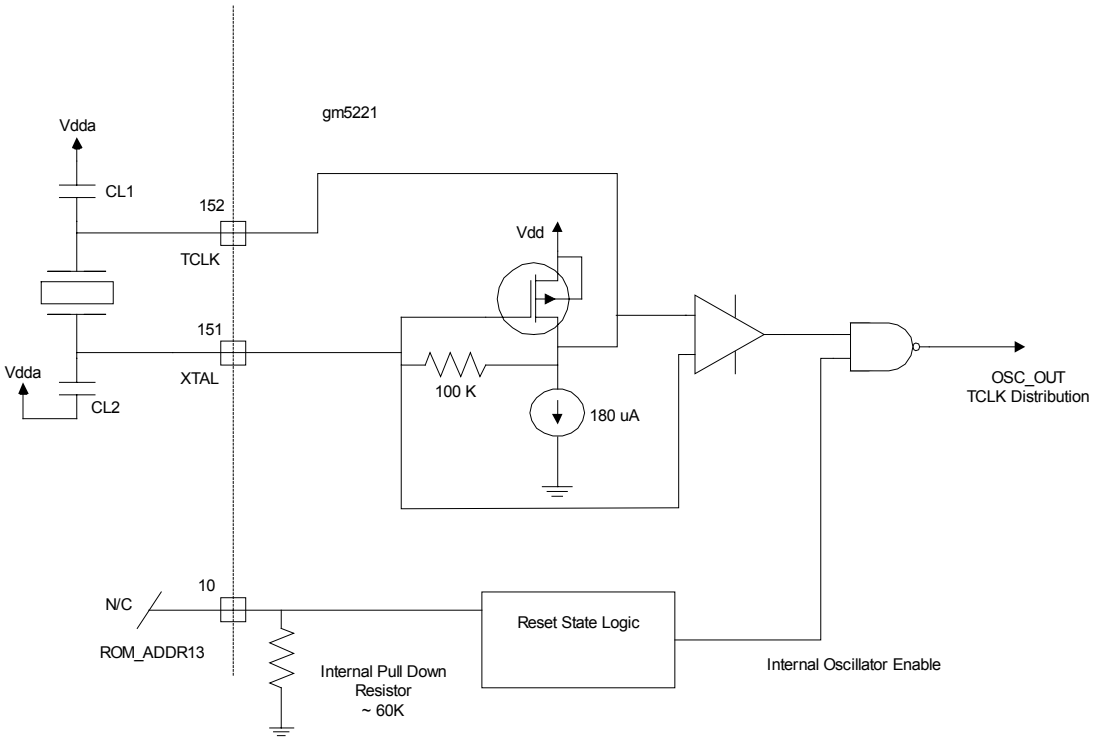


**Figure 4. Using the Internal Oscillator with External Crystal**

The TCLK oscillator uses a Pierce Oscillator circuit. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2 volts above ground (see Figure 5). The peak-to-peak voltage of the output can range from 250 mV to 1000 mV depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. The output of the comparator is buffered and then distributed to the internal circuits.

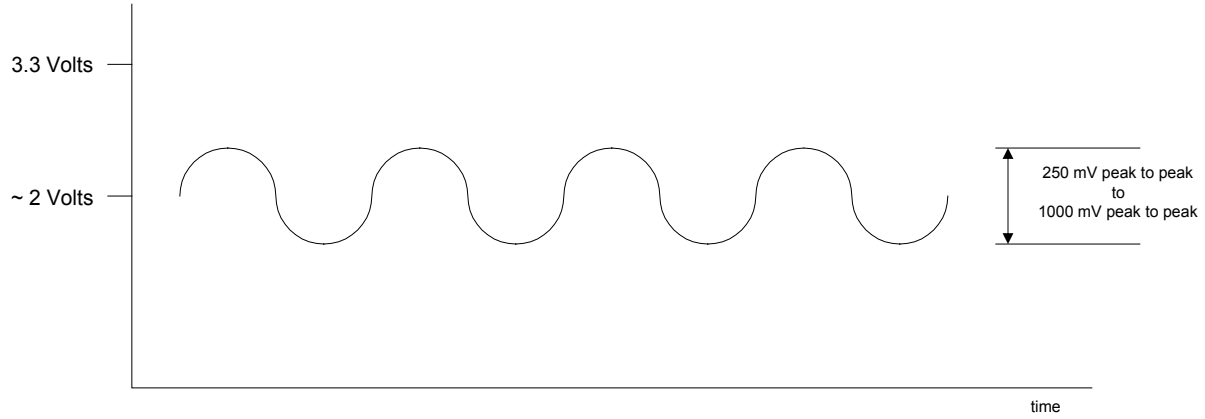


**Figure 5. Internal Oscillator Output**

One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal as shown in Figure 6. The loading capacitance ($C_{load}$) on the crystal is the combination of $C_{L1}$ and $C_{L2}$ and is calculated by $C_{load} = ((C_{L1} * C_{L2}) / (C_{L1} + C_{L2})) + C_{shunt}$. The shunt capacitance $C_{shunt}$ is the effective capacitance between the XTAL and TCLK pins. For the gm5221 this is approximately 9 pF. $C_{L1}$ and $C_{L2}$ are a parallel combination of the external loading capacitors ($C_{ex}$), the PCB board capacitance ($C_{pcb}$), the pin capacitance ($C_{pin}$), the pad capacitance ($C_{pad}$), and the ESD protection capacitance ($C_{esd}$). The capacitances are symmetrical so that $C_{L1} = C_{L2} = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}$. The correct value of $C_{ex}$ must be calculated based on the values of the load capacitances. Approximate values are provided in Figure 6.

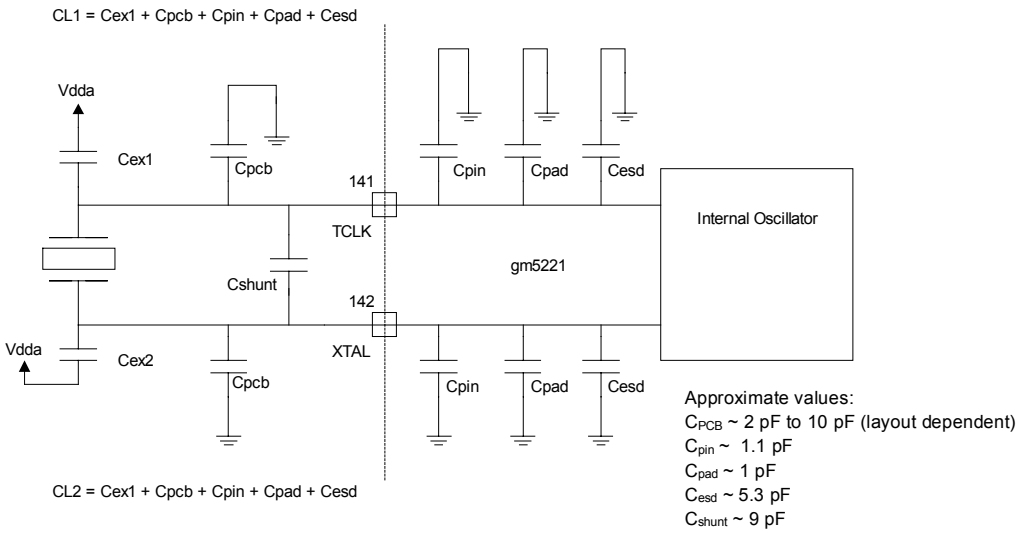


**Figure 6. Sources of Parasitic Capacitance**

Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of $C_{load}$ that is specified by the manufacturer

should not be exceeded because of potential start up problems with the oscillator. Additionally, the crystal should be a parallel resonate-cut and the value of the equivalent series resistance must be less then 90 Ω.

### 4.1.2 Clock Synthesis

The gm5221 synthesizes additional clocks using PLLs as follows:

1) **T_CLK** - Main Timing Clock is the output of the chip internal crystal oscillator. T_CLK is derived from the TCLK/XTAL pad input.
2) **R_CLK** - Reference Clock synthesized by RCLK PLL using T_CLK or EXTCLK as the reference. RCLK PLL output port is not to exceed 4 standard loads.
3) **DVI_CLK** - DVI Output Clock synthesized by DVI receiver PLL using RC+/RC-as the reference.
4) **S_CLK** - Input Source Clock synthesized by SDDS PLL using input HS as the reference. The SDDS also uses the R_CLK to drive internal digital logic.
5) **D_CLK** - Display Clock synthesized by DDDS PLL using IP_CLK as the reference. The DDDS also uses the R_CLK to drive internal digital logic.
6) **F_CLK** - Fixed Frequency Clock synthesized by FDDS. Used as OCM_CLK domain driver.
7) **ADC_DEL_ACLK** - ADC Output Clock is a delayed A_CLK. The analog ADC performs the delay adjustment.

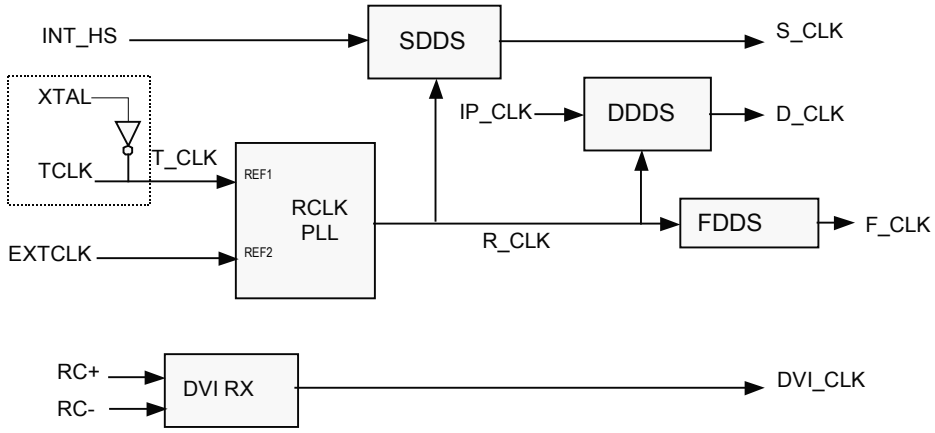


**Figure 7. Internally Synthesized Clocks**

The on-chip clock domains are selected from the synthesized clocks as shown in Figure 8 below. These include:

1) **IP_CLK** - Input Clock Domain
2) **OCM_CLK** - Host Interface and On-chip Micro-controller Clock
3) **DP_CLK** – Scaling Filter and Display Pixel Clock

4) **IFM_CLK** - Source Timing Measurement Domain

5) **A_CLK** - ADC Clock Domain

The clock selection for each domain as shown in the figure below is controlled using the CLOCK_CONFIG register.

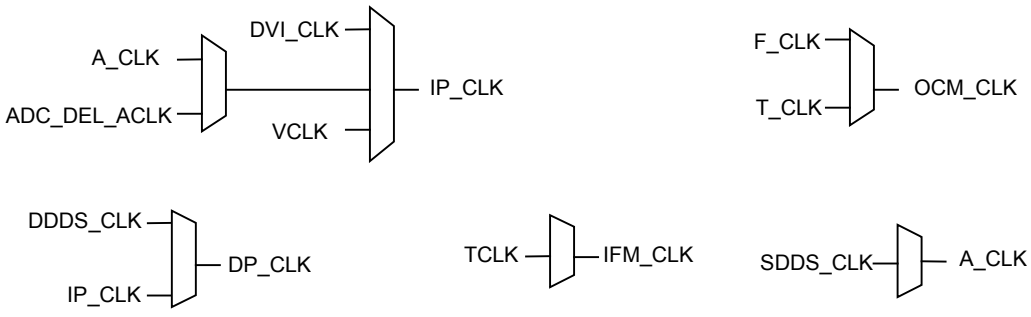


**Figure 8. On-chip Clock Domains**

## 4.2 Chip Initialization

### 4.2.1 Hardware Reset

The gm5221 device integrated a Reset Pulse generator, so that a Reset IC is not required externally.

Hardware Reset is performed by an internal Reset Pulse generator, or by holding the RESETn pin low for a minimum of 150ms. The Reset Pulse is around 150ms in duration, a low-true output on pin RESETn. A TCLK input (see Clock Options above) must be applied during and after the reset. When the reset period is complete and RESETn is de-asserted, the power-up sequence is as follows:

1. Reset all registers of all types to their default state (this is 00h unless otherwise specified in the gm5221 Register Listing).
2. Force each clock domain into reset. This continues for 64 local clock domain cycles following the de-assertion of RESETn.
3. Operate the OCM_CLK domain at the TCLK frequency.
4. Preset the RCLK PLL to output ~200MHz clock (assumes 14.3MHz TCLK crystal frequency).

Figure 9 below shows the relationship between RESETn and 3.3V AVDD power rail (AVDD_3.3): Tr is the reset active period, and Tp is the hold time of push button that grounds RESETn pin.

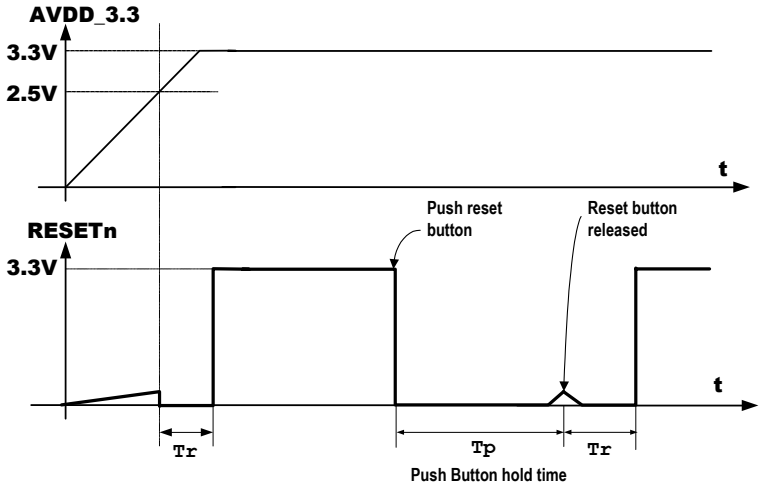


**Figure 9. Reset Pulse vs. +3.3V_AVDD power line**

Where

**Table 8. RESET Time**

| RESETn active period (Tr) specification | | |
|---|---|---|
| | Min | Max |
| **Tr** | 100 | 160 |

The reset threshold for the 3.3V AVDD power rail is 2.5V, and a glitch filter in the reset circuitry will ignore the AVDD_3.3 glitch if the glitch duration is less than 100 ns. However, if AVDD_3.3 voltage drops below 2.5V **and** the glitch duration is more than 100ns, the RESETn will be asserted to reset the chip. Figure 10 below illustrates the AVDD_3.3V glitch that will cause RESETn to be asserted.

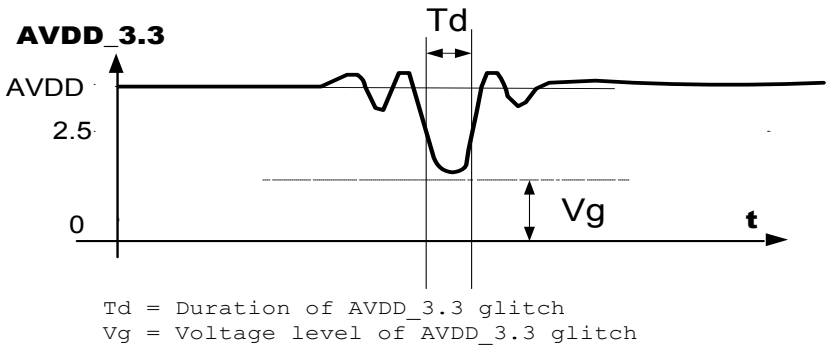


**Figure 10. Glitch in 3.3V AVDD**

**Table 9. Requirement for RESETn due to Glitch in AVDD_3.3V**

| Requirement for RESETn due to AVDD_3.3V glitch | | |
|---|---|---|
| | Min | Max |
| **Td** | 100ns | |
| **Vg** | | 2.5V |

Note: The RESETn pin should be connected to ground with a 0.01uF capacitor to avoid spontaneous reset conditions.

### 4.2.2 Power Sequencing

At any time during the power-up sequence the actual voltage of the 3.3V RVDD power supply should always be equal to or higher than the actual voltage of the 1.8V CVDD power supply. In mathematical terms, $V_{RVDD} >= V_{CVDD}$ at all times. This is illustrated in 0.

In addition, the system designer must ensure that the 1.8V core VDD supply must be active for at least 1ms before the rising edge of the chip RESETn signal during the chip power-up sequence. The rising edge of RESETn signal is used to latch the bootstrap configurations, so its correct timing relationship to the core VDD is critical for correct chip operation.

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{RVDD-CVDD}$(for all t>0) | 0V | | |
| $T_{CVDD->RESETn}$ | 150ms | | |

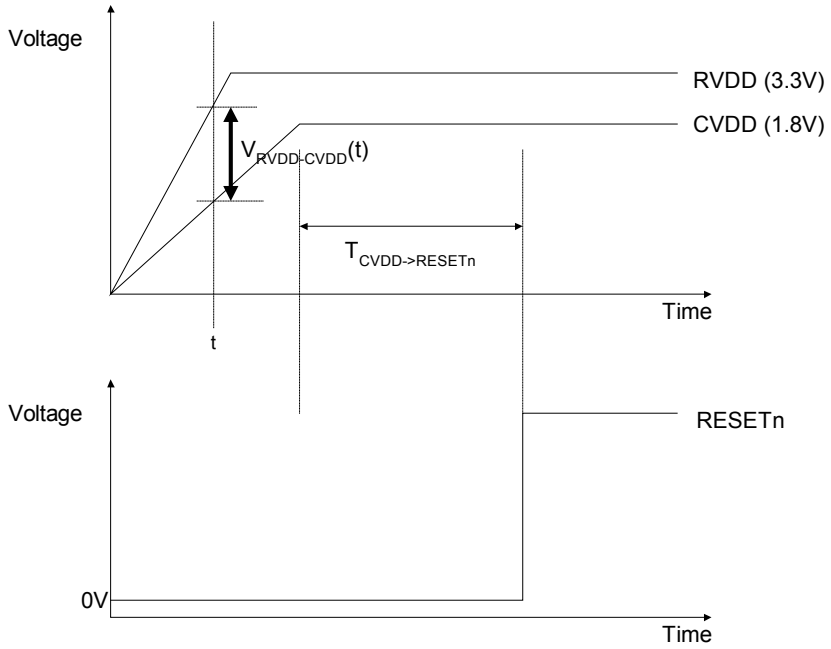


**Figure 11. Correct Power Sequencing**

## 4.3 Analog to Digital Converter (ADC)

### 4.3.1 ADC Pin Connection

The analog RGB signals are connected to the gm5221 as described below:

**Table 10. Pin Connection for RGB Input with HSYNC/VSYNC**

| Pin Name | ADC Signal Name |
|---|---|
| Red+ | Red |
| Red- | Terminate as illustrated in Figure 12. |
| SOG_MCS | Dedicated Sync-on-Green pin |
| Green+ | Green |
| Green- | Terminate as illustrated in Figure 12. |
| Blue+ | Blue |
| Blue- | Terminate as illustrated in Figure 12. |
| HSYNC | Horizontal Sync. Terminate as illustrated in Figure 12. |
| VSYNC | Vertical Sync. Terminate as with HSYNC illustrated in Figure 12. |

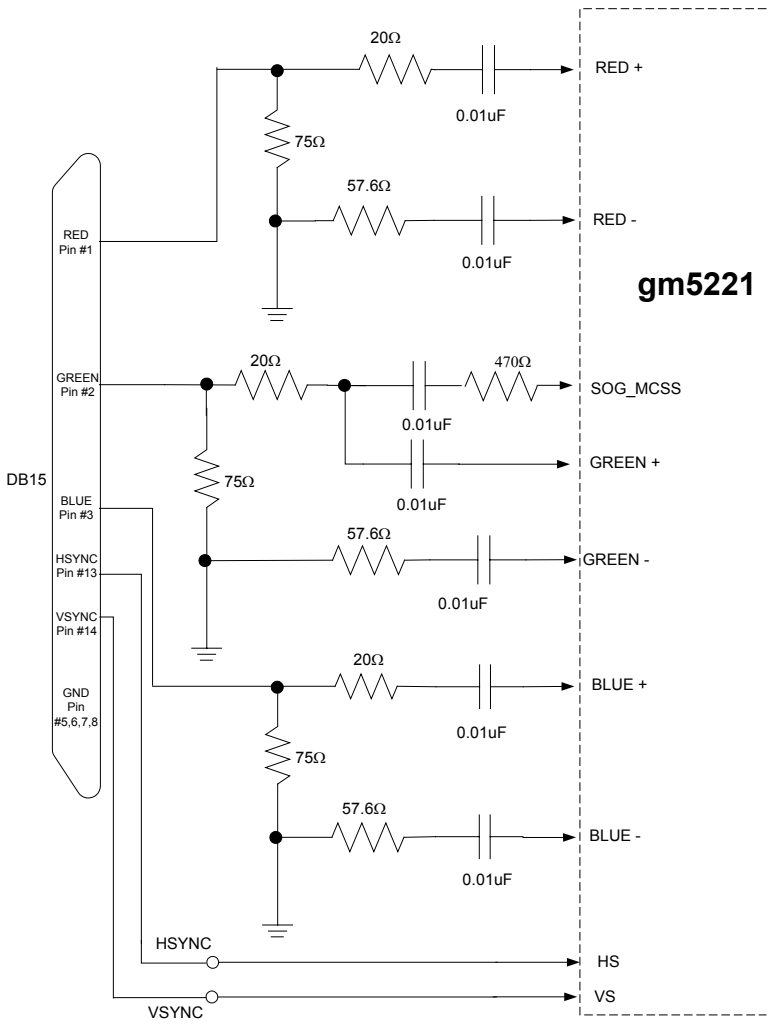


**Figure 12. Example ADC Signal Terminations**

Note that if Sync-On-Green (SoG) or Sync-On-Y (SoY) is not required then SOG_MCSS pin should be left unconnected.

Note that it is important to follow the recommended layout guidelines (see the system layout guidelines).

Also note that the ADC can be used to sample analog signals in the YPbPr color space. In this case the digital color controls are used to convert these signals to the RGB color domain for display on the LCD panel.

### 4.3.2 ADC Characteristics

The table below summarizes the characteristics of the ADC:

**Table 11. ADC Characteristics**

| | MIN | TYP | MAX | NOTE |
|---|---|---|---|---|
| Track & Hold Amp Bandwidth | | | 290 MHz | Guaranteed by design. Note that the Track & Hold Amp Bandwidth is programmable. 290 MHz is the maximum setting. |
| Full Scale Adjust Range at RGB Inputs | 0.55 V | | 0.90 V | |
| Full Scale Adjust Sensitivity | | +/- 1 LSB | | Measured at ADC Output.<br>Independent of full scale RGB input. |
| Zero Scale Adjust Sensitivity | | +/- 1 LSB | | Measured at ADC Output. |
| Sampling Frequency (Fs) | 10 MHz | | 162.5 MHz | |
| Differential Non-Linearity (DNL) | | +/-0.5 LSB | +/-0.9 LSB | Fs = 135 MHz |
| No Missing Codes | | | | Guaranteed by test. |
| Integral Non-Linearity (INL) | | +/- 1.5 LSB | | Fs =135 MHz |
| Channel to Channel Matching | | +/- 0.5 LSB | | |

Note that input formats with resolutions or refresh rates higher than that supported by the LCD panel are supported as recovery modes only. This is called RealRecovery™. For example, it may be necessary to shrink the image. This may introduce image artifacts. However, the image is clear enough to allow the user to change the display properties.

The ADC has a built in clamp circuit for AC-coupled inputs. By inserting series capacitors (about 10 nF), the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

### 4.3.3 Clock Recovery Circuit

The SDDS (Source Direct Digital Synthesis) clock recovery circuit generates the clock used to sample analog RGB data (ACLK or source clock). This circuit is locked to HSYNC of the incoming video signal.

Patented digital clock synthesis technology makes the clock circuits resistant to temperature/voltage drift. Using DDS (Direct Digital Synthesis) technology, the clock recovery circuit can generate any ACLK clock frequency within the range of 10MHz to 165MHz.

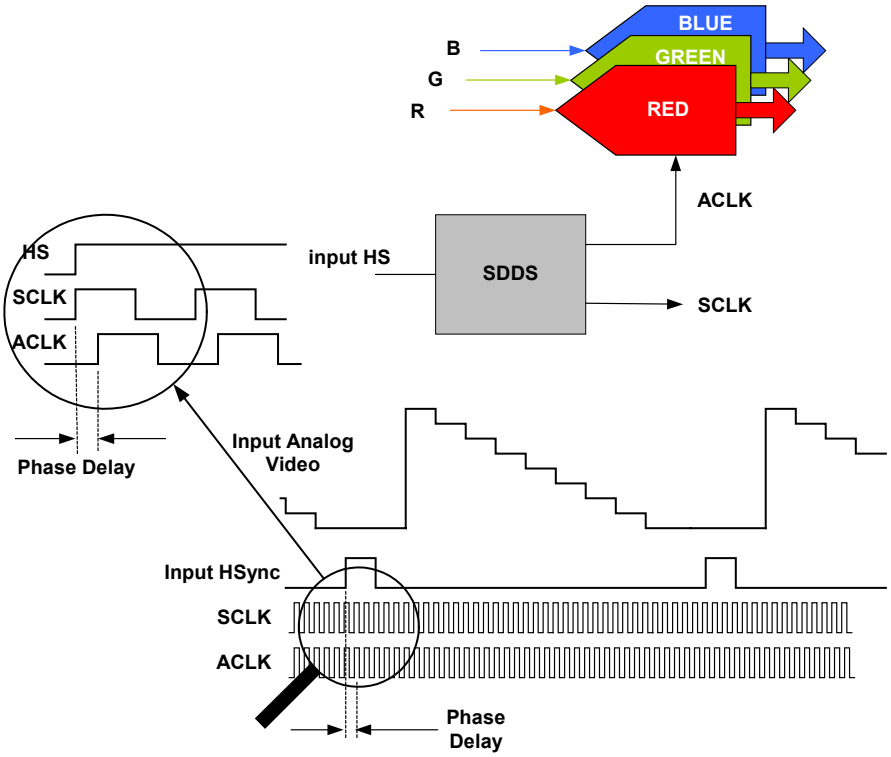


**Figure 13. gm5221 Clock Recovery**

### 4.3.4 Sampling Phase Adjustment

The programmable ADC sampling phase is adjusted by delaying the (input HSYNC aligned) SCLK to produce the ADC clock (ACLK) inside the SDDS. The phase delay is programmable in 64 steps as a fraction of the ACLK period. The accuracy of the sampling phase is checked and the result read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

### 4.3.5 SOG and CSYNC support

The gm5221 has the capability to support the following types of SOG and CSYNC inputs without having to use external components. The signals below show the Negative types of SOG and CSYNC signals. The gm5221 can also support the Positive types.

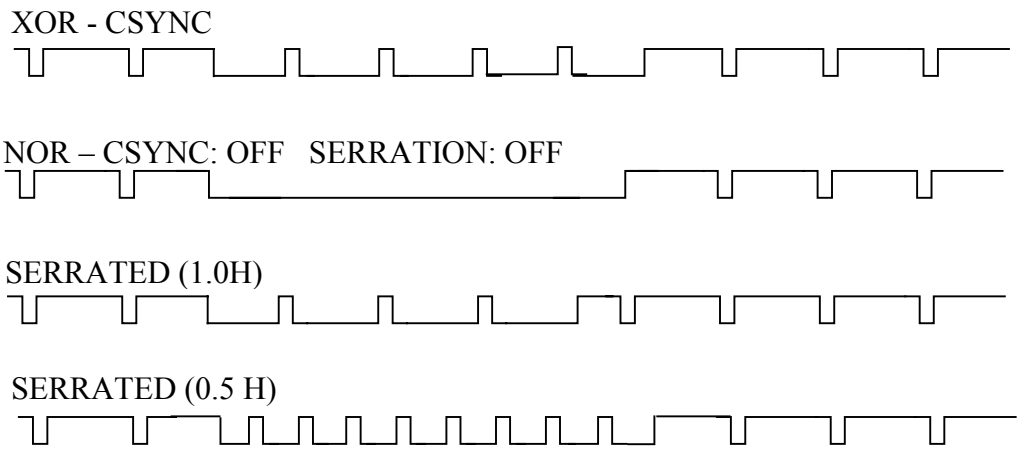


**Figure 14. Supported SOG and CSYNC signals**

## 4.4 Ultra-Reliable Digital Visual Interface Receiver (DVI Rx)

The Ultra-Reliable DVI™ receiver block of the gm5221 is compliant with DVI 1.0 single link specifications. Digital Visual Interface (DVI) is a standard. This block supports an input clock frequency ranging from 20 MHz to 165 MHz.

### 4.4.1 DVI Receiver Characteristics

Please note that it is very important to follow the recommended layout guidelines for these signals.

**Table 12. DVI Receiver Characteristics**

| | MIN | TYP | MAX | NOTE |
|---|---|---|---|---|
| **DC Characteristics** | | | | |
| Differential Input Voltage | 150mV | | 1200mV | |
| Input Common Mode Voltage | AVDD –300m V | | AVDD -37mV | |
| Behavior when Transmitter Disable | AVDD -10mV | | AVDD +10mV | |
| **AC Characteristics** | | | | |
| Input clock frequency | 20 MHz | | 165 MHz | |
| Input differential sensitivity (Peak-to-peak) | 150mV | | | |
| Max differential input (peak-to-peak) | | | 1560 mV | |
| Allowable Intra-Pair skew at Receiver | | | 250 ps | Input clock = 160 MHz |
| Allowable Inter-Pair skew at Receiver | | | 4.0 ns | |

Through register programming, the receiver unit may be placed in one of three states:

- **Active:** The receiver block is fully on and running.
- **Standby:** RC (clock) channel and the data channel carrying syncs remain active. Data and other control signals are not decoded.

- **Off:** The receiver block is powered down.

### 4.4.2 High-Bandwidth Digital Content Protection (HDCP)

**NOTE:** This section applies to the HDCP enabled version gm5221H only. HDCP is disabled in the non-HDCP enabled version gm5221.

The HDCP system allows authentication of a video receiver by a video transmitter, decryption of transmitter-encoded video data by the receiver, and periodic renew-ability of authentication during transmission. The gm5221 implements circuitry to allow full support of the HDCP 1.0 protocol for DVI inputs.

For enhanced security, Genesis provides a means of storing and accessing the secret key given to individual monitor units in an encrypted format.

Further details of the protocol and theory of the system can be found in the *High-bandwidth Digital Content Protection System* specification (see www.digital-cp.com).

## 4.5 ITU656 Video Input Port

The ITU656 video input port connects to commercially available NTSC or PAL video decoders. ITU-BT-656 video format consists of pixel clock and 8 bits of data. No separate HSYNC, VSYNC signals are required. The internal 656 decoder extracts these from the embedded timing data.

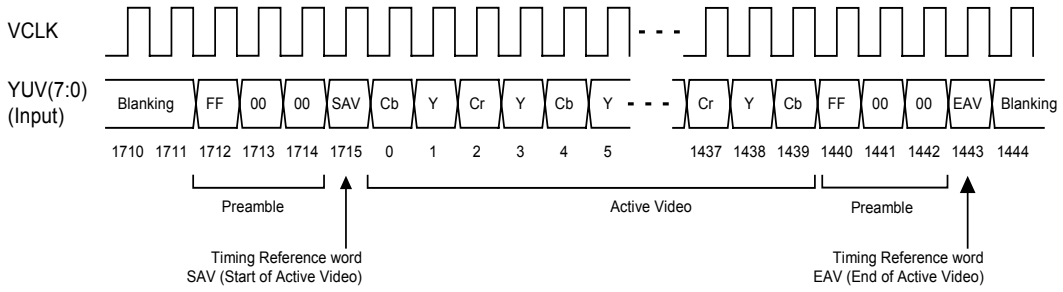


**Figure 15. ITU-R BT656 Input Format**

YCbCr input to the gm5221 is always automatically clamped to restrict the input data to ITU-R BT601 levels:

- Y Bottom clamping: Y data < 16 is clamped to 16.
- Y Top clamping: Y data > 235 is clamped to 235.
- CbCr Bottom clamping: CbCr data < 16 is clamped to 16.
- CbCr Top clamping: CbCr data > 240 is clamped to 240.

## 4.6 Test Pattern Generator (TPG)

gm5221 contains a number of preset test patterns, some of which are shown in Figure 16. There are also parameter based test patterns for generating ramps and grids. Once programmed, the gm5221 test pattern generator can replace a video source (e.g. a PC) during factory calibration and test. This simplifies the test

procedure and eliminates the possibility of image noise being injected into the system from the source. The foreground and background colors are programmable. In addition, the gm5221 OSD controller can be used to produce other patterns.

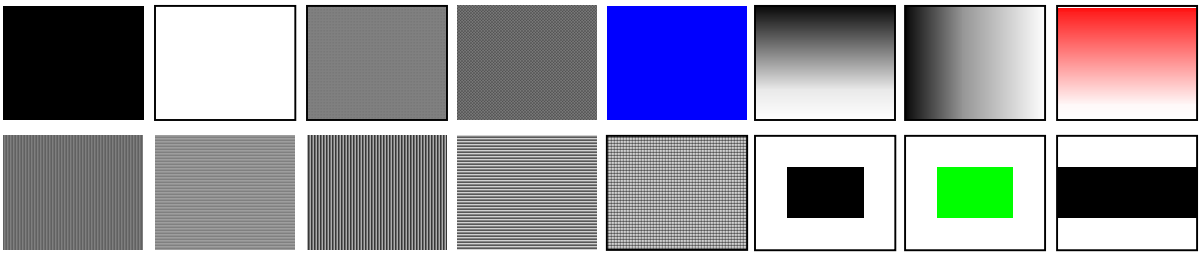

**Figure 16. Some of gm5221 Built-in Test Patterns**

## 4.7 Input Format Measurement

The gm5221 has an Input Format Measurement block (the IFM) providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input format. It is also capable of detecting the field type of interlaced formats.

The IFM features a programmable reset, separate from the regular gm5221 soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating while gm5221 is running in power down mode.

Horizontal measurements are measured in terms of the selected IFM_CLK (either TCLK or RCLK/4), while vertical measurements are measured in terms of HSYNC pulses.

### 4.7.1 HSYNC / VSYNC Delay

The active input region captured by the gm5221 is specified with respect to internal HSYNC and VSYNC. By default, internal syncs are equivalent to the HSYNC and VSYNC at the input pins and thus force the captured region to be bounded by external HSYNC and VSYNC timing. However, the gm5221 provides an internal HSYNC and VSYNC delay feature that removes this limitation.

This HSYNC and VSYNC delay is used for image positioning of ADC input data. HSYNC is delayed by a programmed number of selected input clocks.

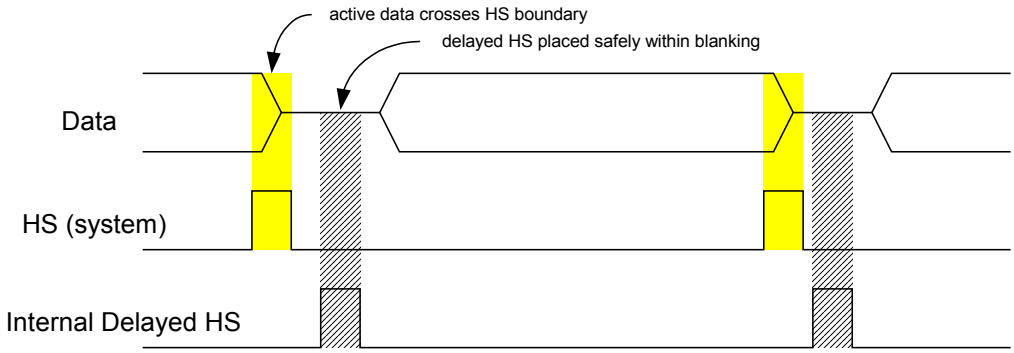


**Figure 17. Active Data Crosses HSYNC Boundary**

### 4.7.2 Horizontal and Vertical Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock period (either TCLK or RCLK/4.). Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC.

Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

### 4.7.3 Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert both the system and the on-chip microcontroller. The microcontroller sets a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

### 4.7.4 Watchdog

The watchdog monitors input VSYNC / HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), a register bit is set. When any VSYNC period exceeds the programmed timing threshold (in terms of HSYNC pulses), a second register bit is set. An interrupt can also be programmed to occur.

### 4.7.5 Internal Odd/Even Field Detection (For Interlaced Inputs to ADC Only)

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a “window” relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

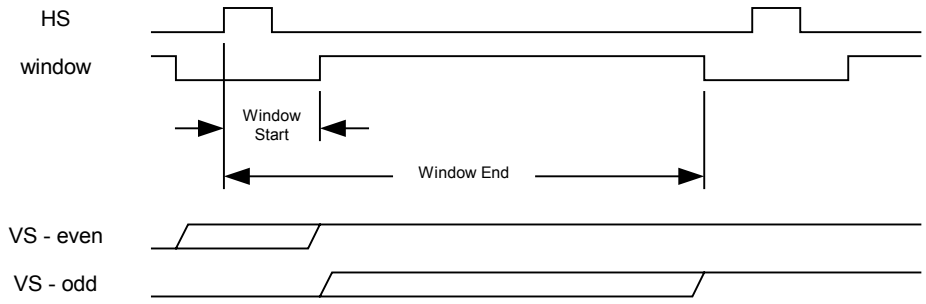


**Figure 18. ODD/EVEN Field Detection**

### 4.7.6 Input Pixel Measurement

The gm5221 provides a number of pixel measurement functions intended to assist in configuring system parameters such as pixel clock, SDDS sample clocks per line and phase setting, centering the image, or adjusting the contrast and brightness.

### 4.7.7 Image Phase Measurement

This function measures the sampling phase quality over a selected active window region. This feature may be used when programming the source DDS to select the proper phase setting.

### 4.7.8 Image Boundary Detection

The gm5221 performs measurements to determine the image boundary. This information is used when programming the Active Window and centering the image.

### 4.7.9 Image Auto Balance

The gm5221performs MIN and MAX pixel value measurements on the input data that is used to adjust brightness and contrast.

## 4.8 Intelligent Image Processing™ Zoom/Shrink/Sharpening Filter

### 4.8.1 Variable Zoom Scaling

The scaling engine uses an advanced third generation multi-tap, non-linear scaling engine, which uses FIR filter technique and can accept nearly any input resolution and can scale it to any output resolution, in a range from one-half reduction to a 256-fold expansion. Scaling is highly configurable, with options to scale in both horizontal and vertical directions with different methods. The scalar must scale nearly any signal input to accommodate nearly any panel input. Moreover, it provides high quality scaling of real time video and graphics images. An input field/frame is scalable in both the vertical and horizontal dimensions.

Interlaced fields may be spatially de-interlaced by vertically scaling and repositioning the input fields to align with the output display's pixel map.

### 4.8.2 Horizontal and Vertical Shrink

A shrink function may be performed on the input data. This is an arbitrary horizontal/vertical reduction to between (50% + 1 pixel/line) to 100% of the input. For example, this allows UXGA 1600x1200 pixels to be displayed as SXGA 1280x1024. For example, this is useful to allow the user to use Windows Display Properties to reduce the screen resolution if it is higher than that of the display.

### 4.8.3 Programmable Sharpening Filter

The coefficients used in the scaling engine are programmable and can be used to perform sharpening. For example, font edges can be enhanced in text or spreadsheet applications, or motion video images can be sharpened. This is available at any scale factor, or when scaling is not required (i.e. 1:1 mode).

## 4.9 Advanced Digital Color Controls

The digital color controls consist of the components shown in Figure 19.

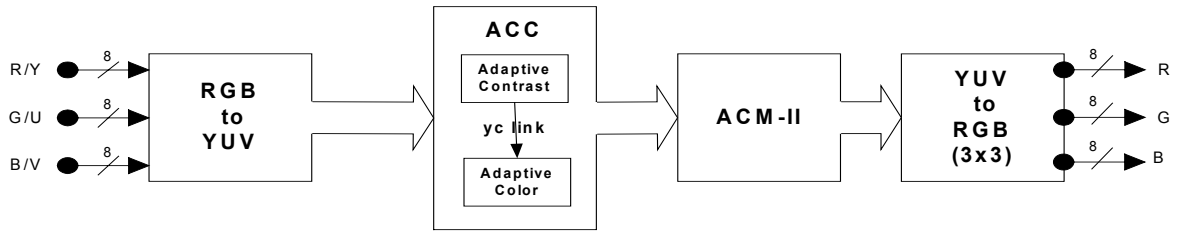


**Figure 19. Digital Color Controls**

### 4.9.1 Adaptive Contrast and Color (ACC)

Most video content is tailored for display on CRTs or in movie theatres. However, CRT monitors have a wider dynamic range than LCD monitors. Therefore, it is desirable to enhance the dynamic range when video is displayed using LCD monitors.

ACC enhances the contrast of the image to account for this. This makes dark colors darker, and bright colors brighter. In addition, the contrast enhancement is adaptive. That is, dark scenes are transformed in a way that preserves color resolution of darker colors and bright scenes are transformed in a way that preserves the color resolution of brighter colors. This is done by calculating a running average of the luminance content of the image, divided up into three ranges. This histogram is then used to select the weighting coefficients between three different luminance transfer functions. The running average may be applied over a programmable number of frames.

ACC can be applied within a highlight window or over the full display area.

### 4.9.2 Active Color Management–II (ACM-II)

Active Color Management provides TV style control of global color parameters like hue, saturation and contrast, and local color changes such as skin tone adjustment, green enhance, or blue stretch. It can be applied within a highlight window or over the full display area.

### 4.9.3 Gamma Look-Up-Table (LUT)

An 8 to 10-bit look-up table (LUT) for each input color channel is intended for Gamma correction and to compensate for a non-linear response of the LCD panel. A 10-bit output results in an improved color depth control. The 10-bit output is then dithered down to 8 bits (or 6 bits) per channel at the display. The LUT is user-programmable to provide an arbitrary transfer function. Gamma correction occurs after the zoom / shrink scaling block. If bypassed, the LUT does not require programming.

### 4.9.4 Color Standardization and sRGB Support

Internet shoppers may be very picky about what color they experience on the display. gm5221 RealColor™ digital color controls can be used to make the color response of an LCD monitor compliant with standard color definitions, such as sRGB. sRGB is a standard for color exchange proposed by Microsoft and HP (see www.srgb.com). gm5221 RealColor controls can be used to make LCD monitors sRGB compliant, even if the native response of the LCD panel itself is not. For more information on sRGB compliance using Genesis devices please refer to the sRGB application brief C5115-APB-02A.

### 4.9.5 Video Windowing

Often video content (e.g. movie from DVD) is displayed in a portion of the display while the operating system's desktop appears in the remainder. In this case it is desirable to have different color controls in the various regions of the display. For example, the user may desire that the desktop is sRGB compliant while performing hue or saturation adjustments in the region containing the video content. To perform such adjustments the 3x3 color controls and the gamma tables may be separately controlled inside and outside a defined rectangle. The coordinates of the rectangle may be provided by the operating system (and communicated using DDC2Bi) or selected by the user (using the OSD).

## 4.10 Display Output Interface

The Display Output Port provides data and control signals that permit the gm5221 to connect to a variety of flat panel devices using an LVDS interface. The output interface is configurable for single or dual wide LVDS in 18 or 24-bit RGB pixels format. All display data and timing signals are synchronous with the DCLK display clock. The integrated LVDS transmitter is programmable to allow the data and control signals to be mapped into any sequence depending on the specified receiver format. DC balanced operation is supported as described in the Open LDI standard.

### 4.10.1 Display Synchronization

The gm5221 supports the following display synchronization modes:

- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation.
- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

### 4.10.2 Display Timing Programming

Horizontal values are programmed in single-pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

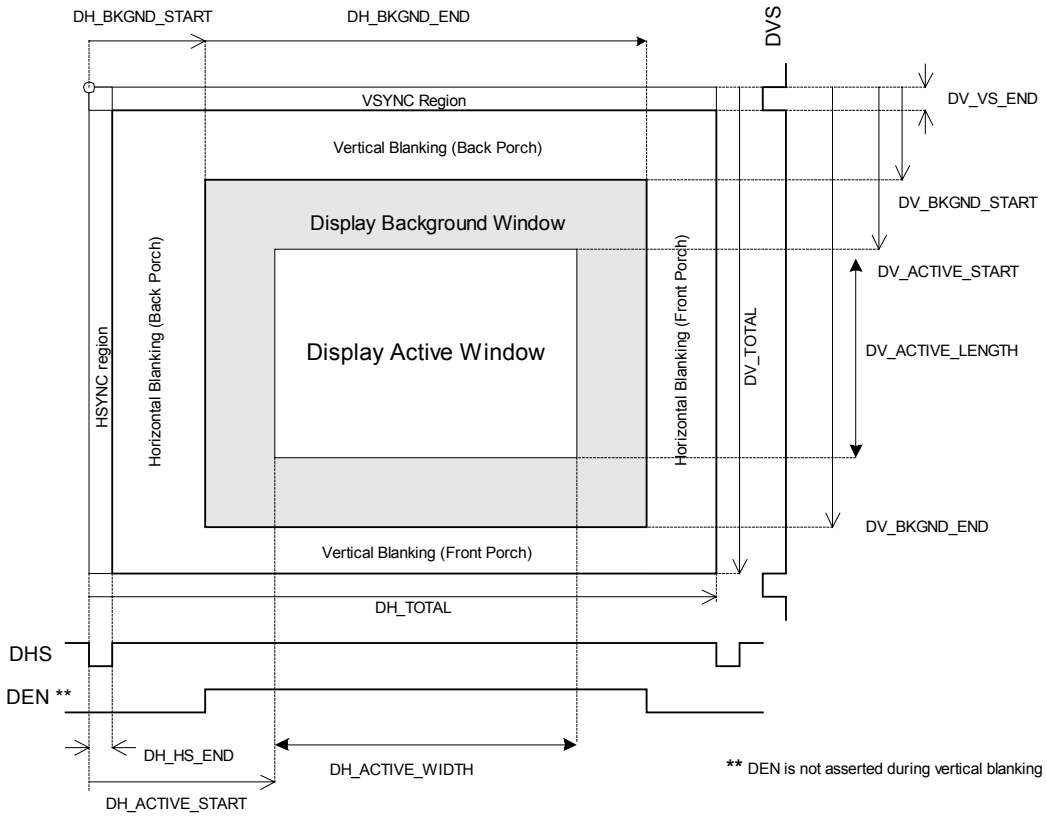


**Figure 20. Display Windows and Timing**

### 4.10.3 Output Dithering

The Gamma LUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels. In this way it is possible to display 16.7 million colors on a LCD panel with 6-bit column drivers.

The benefit of dithering is that the eye tends to average neighboring pixels and a smooth image free of contours is perceived. Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. Two dithering algorithms are available: random or ordered dithering. Ordered dithering is recommended when driving a 6-bit panel.

All gray scales are available on the panel output whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

### 4.10.4 Dual Four-Channel LVDS Transmitter

gm5221 implements the industry standard flexible four channel dual LVDS transmitter. The LVDS transmitter can support the following:

- Single pixel mode
- 24-bit panel mapping to the LVDS channels
- 18-bit panel mapping to the LVDS channels
- Programmable channel swapping (the clocks are fixed)
- Programmable channel polarity swapping
- Supports up to SXGA 75Hz output

**Table 13. Supported LVDS 24-bit Panel Data Mappings**

| | |
|---|---|
| Channel 0 | R0, R1, R2, R3, R4, R5, G0 |
| Channel 1 | G1, G2, G3, G4, G5, B0, B1 |
| Channel 2 | B2, B3, B4, B5, PHS, PVS, PDE |
| Channel 3 | R6, R7, G6, G7, B6, B7, RES |

| | |
|---|---|
| Channel 0 | R2, R3, R4, R5, R6, R7, G2 |
| Channel 1 | G3, G4, G5, G6, G7, B2, B3 |
| Channel 2 | B4, B5, B6, B7, PHS, PVS, PDE |
| Channel 3 | R0, R1, G0, G1, B0, B1, RES |

**Table 14. Supported LVDS 18-bit Panel Data Mapping**

| | |
|---|---|
| Channel 0 | R0, R1, R2, R3, R4, R5, G0 |
| Channel 1 | G1, G2, G3, G4, G5, B0, B1 |
| Channel 2 | B2, B3, B4, B5, PHS, PVS, PDE |
| Channel 3 | Disabled for this mode |

### 4.10.5 Single Pixel TTL Output

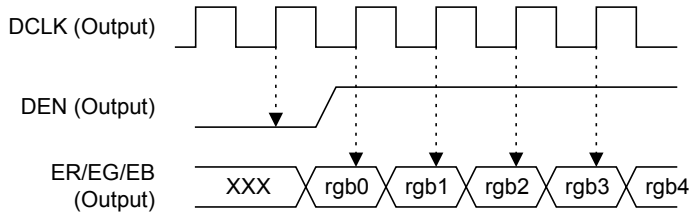


**Figure 21. Single Pixel Width Display Data**

### 4.10.6 Panel Power Sequencing (PPWR, PBIAS)

The gm5221 has two dedicated outputs PPWR and PBIAS to control LCD power sequencing once data and control signals are stable. The timing of these signals is fully programmable.

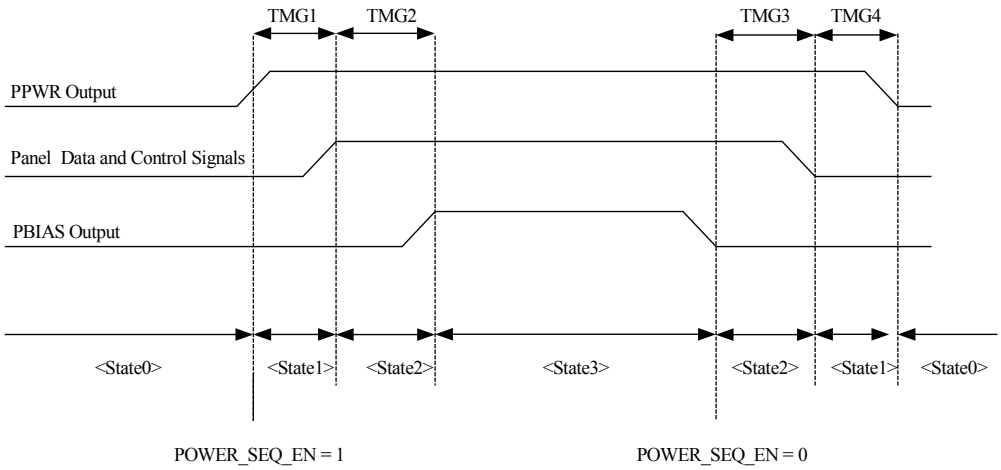


**Figure 22. Panel Power Sequencing**

## 4.11 Energy Spectrum Management (ESM)

High spikes in the EMI power spectrum may cause LCD monitor products to violate emissions standards. The gm5221 has many features that can be used to reduce electromagnetic interference (EMI). These include drive strength control and clock spectrum modulation. These features help to eliminate the costs associated with EMI reducing components and shielding.

## 4.12 On-Screen Display (OSD)

The gm5221 has a fully programmable, high-quality OSD controller. The graphics are divided into "cells" of programable size. The cells are stored in an on-chip static RAM (16K bytes) and can be stored as 1-bit per pixel data, 2-bit per pixel data or 4-bit per pixel data.

Some general features of the gm5221 OSD controller include:

- **Two OSD Rectangles –** The OSD can appear in two separately defined rectangular regions.
- **OSD Position –** The OSD menu can be positioned anywhere on the display region. The reference point is Horizontal and Vertical Display Background Start (DH_BKGND_START and DV_BKGND_START).
- **OSD Stretch –** The OSD image can be stretched horizontally and/or vertically by a factor of two. Pixel and line replication is used to stretch the image.
- **OSD Blending** – Sixteen levels of blending are supported for selected colors in the character-mapped.

### 4.12.1 On-Chip OSD SRAM

The on-chip static RAM (16K bytes) stores the cell map, cell definitions, and attribute map. The OSD SRAM is shared by the on-chip microcontroller as part of its normal addressable memory space.

In memory, the cell map is organized as an array of words, each defining the attributes of one visible character on the screen starting from upper left of the visible character array. These attributes specify which character to display, whether it is stored as 1, 2 or 4 bits per pixel, the foreground and background colors, blinking, etc.

Registers are used to define the visible area of the OSD image. For example, Figure 23 shows an example of a cell map.

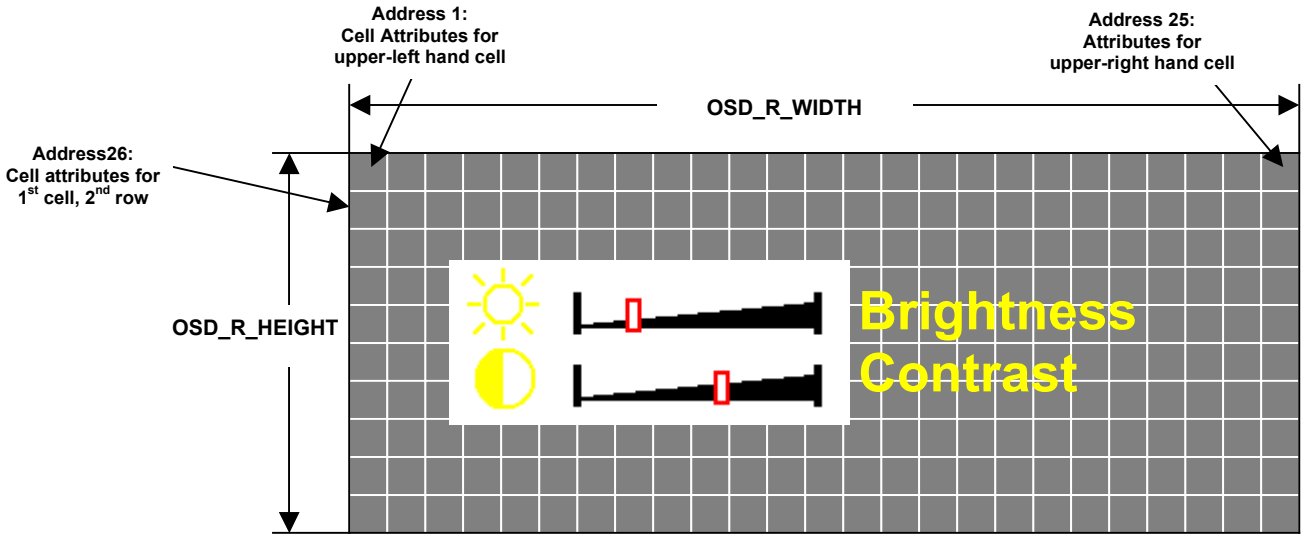


**Figure 23. OSD Cell Map**

Cell definitions are stored as bit map data. On-chip registers point to the start of 1-bit per pixel definitions, 2-bit per pixel definitions and 4-bit per pixel definitions respectively.

Note that the cell map and the cell definitions share the same on-chip RAM. Thus, the size of the cell map can be traded off against the number of different cell definitions. In particular, the size of the OSD image and the number of cell definitions must fit in RA<.

### 4.12.2 Color Look-up Table (LUT)

Each pixel of a displayed cell is resolved to an 8-bit color code. This selected color code is then transformed to a 24-bit value using a 256 x 24-bit look up table.

## 4.13 On-Chip Microcontroller (OCM)

The OCM executes a firmware program running from external ROM. A parallel port with separate address and data busses is available for this purpose. Alternatively, a serial peripheral interface (SPI) may be used with a serial FLASH ROM and a cache controller inside gm5221. This port connects directly to standard, commercially available ROM or programmable FLASH ROM devices. Normally 64KB or 128KB of ROM is required.

### 4.13.1 Compiling firmware

To program the gm5221 the content of the external ROM is generated using Genesis software development tools G-Wizard and OSD-Workbench. G-Wizard is a GUI-based tool for capturing system information such as panel timing, support modes, system configuration, etc. OSD-Workbench is a GUI based tool for defining OSD menus and functionality.

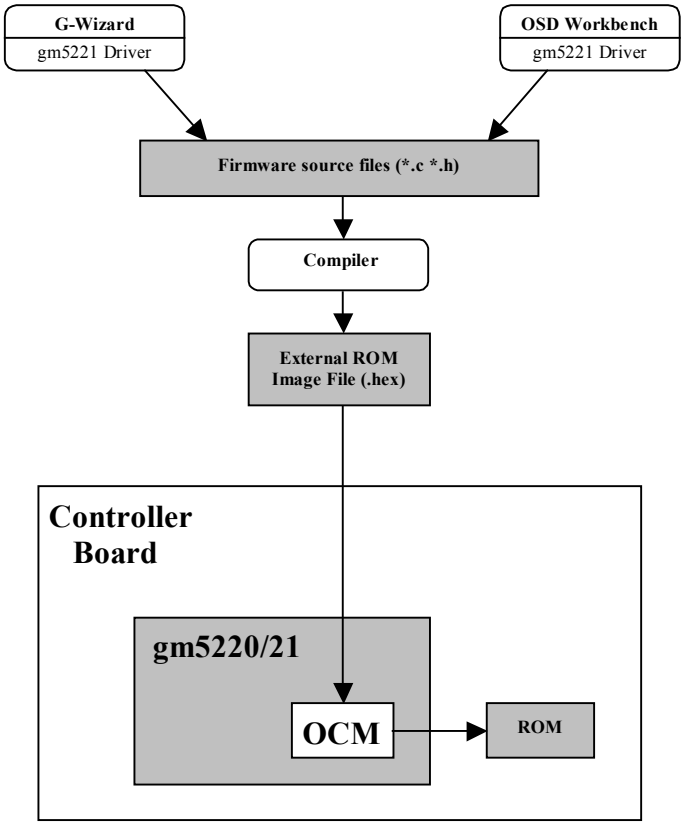


**Figure 24. Programming the OCM**

Genesis recommends using Paradigm compiler (http://www.devtools.com) to compile the firmware source code into a hex file. This hex file is then downloaded into the external ROM using In-System-Programming (Genesis debug software G-Probe communicates with the OCM which in turn programs a FLASH ROM in the system using the ROM_WEn signal) or using commercially available ROM programmers.

### 4.13.2 Embedded Bootstrap Function

gm5221 is equipped with an embedded ROM bootstrap function from which to boot when external ROM is not present or it does not contain data. It is always recommended to boot from embedded ROM (see description of ROM_ADDR16 in Table 16).

The bootstrap function works in the following way. The embedded ROM firmware first looks for a 'signature' in external ROM (either parallel ROM or serial ROM depending on the programming of ROM_ADDR15 – see Table 16). The 'signature' is the ASCII values for the character string "xROM" starting at address 0x800F0. If this signature is found then it performs a CRC check. If CRC is valid then it jumps to external ROM address 0x80100.

If the signature is not present (or bootstrap value of ROM_ADDR7 is one) then the embedded firmware does not jump to external ROM. In this case it runs in its own loop that supports debugging commands (using G-Probe debugging software available from Genesis) over either the UART port (see section 4.13.6) or the DDC2Bi port (see section 4.13.5).

Note that the bootstrap values of ROM_ADDR7 and ROM_ADDR8 (see Table 16) can be used to override the signature checking. In addition, a DDC2Bi command (as configured using bootstrap value of ROM_ADDR12 – see Table 16) can be used to override the signature checking.

### 4.13.3 In-System-Programming (ISP) of External FLASH ROM

The gm5221 has hardware to program FLASH ROM devices. In particular, the ROM_WEn pin can be connected to the write enable of the FLASH ROM. The embedded boot firmware (see section 4.13.2 above) performs the writes.

### 4.13.4 UART Interface

The gm5221 OCM has an integrated Universal Asynchronous Remote Terminal (UART) port that can be used as a factory debug port. In particular, the UART can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System-Programming).

### 4.13.5 DDC2Bi Interface

Hardware support is provided for DDC2Bi communication over the DDC channel of either the analog or DVI input ports. The specification for the DDC2Bi standard can be obtained from VESA (www.vesa.org). The DDC2Bi port can be used as a factory debug port or for field programming. In particular, the DDC2Bi port can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System-Programming).

The factory programming or test station connects to the gm5221 through the Direct Data Channel (DDC) of the DSUB15 or DVI connectors. For example, the PC can make gm5221 display test patterns (see section 4.5). A camera can be used to automate the calibration of the LCD panel.

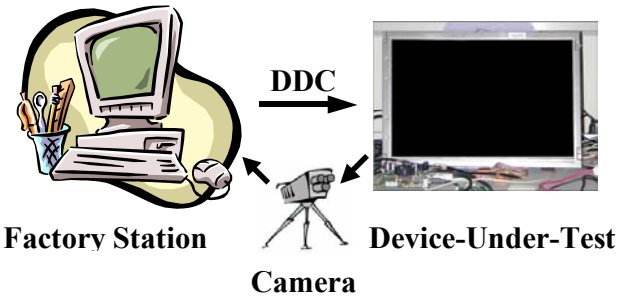


**Figure 25. Factory Calibration and Test Environment**

Two pairs of pins are available for DDC2Bi communication. For DDC2Bi communication over the analog VGA connector pins DDC_SCL_VGA and DDC_SDA_VGA should be connected to the DDC clock and data pins of the analog DSUB15 VGA connector. For DDC2Bi communication over the DVI connector pins DDC_SCL_DVI and DDC_SDA_DVI should be connected to the DDC clock and data pins of the DVI connector. The gm5221 contains serial to parallel conversion hardware that is then accessed by firmware for interpretation and execution of the DDC2Bi command set.

Note that DDC2Bi can only be activated on only one of the inputs at a time. The port activated by default is specified using the bootstrap value of ROM_ADDR12 (see Table 16). Firmware may change this default setting using an on-chip register.

### 4.13.6 JTAG Interface

A JTAG interface is provided to allow in-circuit firmware debugging. This is done using a JTAG port. This port is available on the following signals:

- JTAG_RESET
- JTAG_TDO
- JTAG_TDI
- HOST_SCL (JTAG_CLK)
- HOST_SDA (JTAG_MODE)

Also, a 2-wire to JTAG bridge circuit is provided to allow JTAG commands to be issued using only two pins HOST_SCL and HOST_SDA.

### 4.13.7 General Purpose Inputs and Outputs (GPIO)

The gm5221 has 23 potential general-purpose input/output (GPIO) pins. Not all may be available depending on shared functionality of particular pins. These are used by the OCM to communicate with other devices in the system such as keypad buttons, NVRAM, LED's, audio DAC, etc. Each GPIO has independent direction control and open drain enable for reading and writing. Note that the GPIO pins have alternate functionality as described in Table 15.

**Table 15. GPIO and Alternate Functions**

| Pin Name | Pin Number | Alternate function |
|---|---|---|
| GPIO0 | 81 | No alternative functions. |
| GPIO1 | 82 | |
| GPIO2 | 83 | |
| GPIO3 | 84 | |
| GPIO4 | 85 | |
| GPIO5 | 88 | |
| GPIO6 | 89 | |
| GPIO7/IRQin | 90 | Can be used to trigger an OCM interrupt. |
| GPIO8/IRQout | 91 | Level reflects an on-chip status change. |
| GPIO9/SCL | 92 | Data and clock lines for master 2-wire serial interface to NVRAM, or other devices such as video |
| GPIO10/SDA | 93 | decoder or audio amplifier. |
| GPIO11/PWM0 | 98 | General purpose PWM outputs (back light intensity control, etc.) |
| GPIO12/PWM1 | 99 | |
| GPIO13/PWM2 | 100 | |
| GPIO14/PWM3 | 101 | |
| GPIO16/VDATA7 | 102 | NTSC/PAL Video input port. |
| GPIO17/VDATA6 | 103 | |
| GPIO18/VDATA5 | 106 | |
| GPIO19/VDATA4 | 107 | |
| GPIO20/VDATA3 | 108 | |
| GPIO21/VDATA2 | 109 | |
| GPIO22/VDATA1 | 110 | |
| GPIO23/VDATA0 | 111 | |

### 4.13.8 Low-Bandwidth ADC (LBADC)

A general-purpose ADC is integrated to allow for functions such as keypad scanning or for monitoring system temperature or voltage sensors. The ADC has 8 bits of resolution, and can perform a conversion in 13 TCLK periods (approximately 1 µsec). An analog multiplexer selects one of three analog input pins as the input to the ADC.

### 4.13.9 Low Power State

The gm5221 provides a low power state in which the clocks to selected parts of the chip may be disabled. In addition, the OCM_CLK may be reduced (by a factor of up to 510) so that the OCM itself consumes less power.

### 4.13.10 Pulse Width Modulation (PWM)

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering (due to the interference between panel timing and inverter's AC timing), and adjust brightness.

There are four pins available for PWM outputs: PWM0 (GPIO11), PWM1 (GPIO12), PWM2 (GPIO13) and PWM3 (GPIO14). The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter. Panel HSYNC is used as the clock for a counter generating this output signal.

PWM0 has an additional option for 10-bit duty cycle control.

## 4.14 Bootstrap Configuration Pins

During hardware reset, the external ROM address pins ROM_ADDR[17:0] are configured as inputs. On the negating edge of RESETn, the value on these pins is latched and stored. This value is readable by the on-chip microcontroller (or an external microcontroller via the host interface). Install a 10K pull-up resistor to indicate a '1', otherwise a '0' is indicated because ROM_ADDR[17:0] have a 50KΩ internal pull-down resistor.

**Table 16. Bootstrap Signals**

| Bootstrap | Pin Name | Description |
|---|---|---|
| DEV_ADDR(6:0} | ROM_ADDR6:0 | These pins specify the device address for serial host interface. |
| FORCEIROM<br>FORCEXROM | ROM_ADDR8<br>ROM_ADDR7 | Forces execution from external or internal ROM (see section 4.13.2):<br>00 = Check for signature in external ROM and if present jump to external ROM.<br>01 = Jump to external ROM regardless of whether signature or CRC are present.<br>10 = Jump to internal ROM regardless of whether signature or CRC are present.<br>11 = Check for signature and CRC and if present jump to external ROM (recommended). |
| OCM_USES_TCLK | ROM_ADDR9 | Forces OCM (when executing from embedded boot firmware) to operate using TCLK (see Figure 8):<br>0 = OCM_CLK = FCLK (see Figure 7). UART baud rate is 115200 baud.<br>1 = OCM_CLK = TCLK. UART baud rate is 19200 baud. |
| TCLKSEL1<br>TCLKSEL0 | ROM_ADDR11<br>ROM_ADDR10 | Used by the embedded boot firmware to specify the TCLK frequency:<br>00 = for TCLK = 14.3 MHz<br>01 = for TCLK = 20 MHz<br>10 = for TCLK = 24 MHz<br>11 = for TCLK = 14.3 MHz<br>Note: The embedded firmware uses these bootstraps to program RCLK to 200MHz (or as close as possible in multiples of TCLK) and FCLK to 100MHz. |
| DDCHANSEL | ROM_ADDR12 | Specifies the default DDC2Bi channel when executing from embedded boot firmware:<br>0 = Use DDC_SCL_DVI/DDC_SDA_DVI pin pair.<br>1 = Use DDC_SCL_VGA/DDC_SDA_VGA pin pair. |
| OP_MODE1<br>OP_MODE0 | ROM_ADDR14<br>ROM_ADDR13 | Operating Mode: Selects external register access method.<br>00 = UART (normal operation)<br>01 = 2-wire to JTAG Bridge<br>10 = 5-wire JTAG port<br>11 = Reserved |
| SPI_EN | ROM_ADDR15 | SPI serial ROM interface enable<br>0 = Parallel ROM Interface<br>1 = SPI serial ROM and cache controller |
| OCM_ROM | ROM_ADDR16 | Selects the initial state of internal OCM ROM<br>0 = Internal ROM on at top of 1M in X86 address space (normal operation)<br>1 = Internal ROM off (debug mode – illegal when SPI_EN bootstrap value on ROM_ADDR15 = 1) |
| OSC_SEL | ROM_ADDR17 | Selection of TCLK source. Program to 0 when using external crystal connected to TCLK and XTAL. |

**Note:** There is an internal pull-down resistor of 50KΩ to ground for each signal.

## 4.15 Electrostatic Discharge (ESD)

The gm5221 integrates ESD diodes to protect the device during handling. However, external on-board ESD diodes are required on the analog RGB inputs, DVI inputs, and DDC inputs for protection against electrical overstress (EOS).

# 5 Electrical Specifications

The following targeted specifications have been derived by simulation.

## 5.1 Preliminary DC Characteristics

**Table 17. Absolute Maximum Ratings**

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| 3.3V Supply Voltages (1,2) | $V_{VDD\_3.3}$ | -0.3 | | 3.6 | V |
| 1.8V Supply Voltages (1.2) | $V_{VDD\_1.8}$ | -0.3 | | 1.98 | V |
| Input Voltage (5V tolerant inputs) (1,2) | $V_{IN5Vtol}$ | -0.3 | | 5.5 | V |
| Input Voltage (non 5V tolerant inputs) (1,2) | $V_{IN}$ | -0.3 | | 3.6 | V |
| Electrostatic Discharge | $V_{ESD}$ | | | ±2.0 | kV |
| Latch-up | $I_{LA}$ | | | ±100 | mA |
| Ambient Operating Temperature | $T_A$ | 0 | | 70 | °C |
| Storage Temperature | $T_{STG}$ | -40 | | 150 | °C |
| Operating Junction Temp. | $T_J$ | 0 | | 125 | °C |
| Thermal Resistance (Junction to Air) Natural Convection gm5221 on 4-layer PCB | $\theta_{JA\_4L}$ | | | 34.6 | °C/W |
| Thermal Resistance (Junction to Case) Convection (3) gm5221 | $\theta_{JC}$ | | | 17.0 | °C/W |
| Soldering Temperature (30 sec.) | $T_{SOL}$ | | | TBD | °C |
| Vapor Phase Soldering (30 sec.) | $T_{VAP}$ | | | TBD | °C |

**NOTE (1):** All voltages are measured with respect to GND.

**NOTE (2):** Absolute maximum voltage ranges are for transient voltage excursions.

**NOTE (3):** Based on the figures for the Operating Junction Temperature, $\theta_{JC}$ and Power Consumption in Table 18, the maximum allowed case temperature is calculated as $T_{C(MAX)} = T_{J(MAX)} - P_{(MAX)} \times \theta_{JC}$. For SXGA operation this is 125-1.1x17=106°C.

## Table 18. DC Characteristics

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POWER** | | | | | |
| Power Consumption @ 135 MHz | $P_{SXGA}$ | | 1.1 | | W |
| Power Consumption @ Low Power Mode (1) | $P_{LP}$ | | 50 | | mW |
| 3.3V Supply Voltages (AVDD and RVDD) | $V_{VDD\_3.3}$ | 3.15 | 3.3 | 3.45 | V |
| 1.8V Supply Voltages (VDD and CVDD) | $V_{VDD\_1.8}$ | | 1.8 | | V |
| Supply Current @ CLK =135MHz (gm5221) | I | | 600 | | mA |
| • 1.8V digital supply (2) | $I_{VDD\_1.8}$ | | | 300 | |
| • 1.8V analog supply (3) | $I_{AVDD\_1.8}$ | | | 60 | |
| • 3.3V digital supply (4) | $I_{VDD\_3.3}$ | | | 40 | |
| • 3.3V analog supply (5) | $I_{AVDD\_3.3}$ | | | 200 | |
| Supply Current @ Low Power Mode* | $I_{LP}$ | | 50 | | mA |
| **INPUTS** | | | | | |
| High Voltage | $V_{IH}$ | 2.0 | | $V_{DD}$ | V |
| Low Voltage | $V_{IL}$ | GND | | 0.8 | V |
| Clock High Voltage | $V_{IHC}$ | 2.4 | | $V_{DD}$ | V |
| Clock Low Voltage | $V_{ILC}$ | GND | | 0.4 | V |
| High Current ($V_{IN}$ = 5.0 V) | $I_{IH}$ | -25 | | 25 | µA |
| Low Current ($V_{IN}$ = 0.8 V) | $I_{IL}$ | -25 | | 25 | µA |
| Capacitance ($V_{IN}$ = 2.4 V) | $C_{IN}$ | | | 8 | pF |
| **OUTPUTS** | | | | | |
| High Voltage ($I_{OH}$ = 7 mA) | $V_{OH}$ | 2.4 | | $V_{DD}$ | V |
| Low Voltage ($I_{OL}$ = -7 mA) | $V_{OL}$ | GND | | 0.4 | V |
| Tri-State Leakage Current | $I_{OZ}$ | -25 | | 25 | µA |

**NOTE (1):** Low power figures result from setting the ADC, DVI, and clock power down bits so that only the micro-controller is running.
**NOTE (2):** Includes all CVDD_1.8 pins.
**NOTE (3):** Includes VDD_RX0_1.8, VDD_RX1_1.8, VDD_RX2_1.8, VDD_RXPLL_1.8, VDD_RPLL_1.8 and VDD1_ADC_1.8 pins.
**NOTE (4):** Includes all RVDD_3.3, AVDD _LV_E_3.3 and AVDD _LV_O_3.3 pins.
**NOTE (5):** Includes pins AVDD_RED_3.3, AVDD_GREEN_3.3, AVDD_BLUE_3.3, AVDD_IMB_3.3, AVDD_RX0_3.3, AVDD_RX1_3.3, AVDD_RX2_3.3, AVDD_RXC_3.3, AVDD_RPLL_3.3, AVDD_ADC_3.3, AVDD_LV_3.3 and LBADC_VDD_3.3.
**NOTE (6):** Maximum current figures are provided for the purposes of selecting a power supply circuit.

## 5.2 Preliminary AC Characteristics

All timing is measured to a 1.5V logic-switching threshold. The minimum and maximum operating conditions used were: $T_{DIE}$ = 0 to 125 °C, Vdd = 2.35 to 2.65V, Process = best to worst, $C_L$ = 16pF for all outputs.

**Table 19. Maximum Speed of Operation**

| Clock Domain | Max Speed of Operation |
|---|---|
| Main Input Clock (T_CLK) | 25 MHz (14.3MHz recommended) |
| DVI Differential Input Clock (DVI_CLK) | 165 MHz |
| ADC Clock (S_CLK) | 165 MHz |
| Input Clock (IP_CLK) | 165 MHz |
| Reference Clock (R_CLK) | 220MHz (200MHz recommended) |
| On-Chip Microcontroller Clock (OCM_CLK) | 100 MHz |
| Display Clock (D_CLK) | 165 MHz |

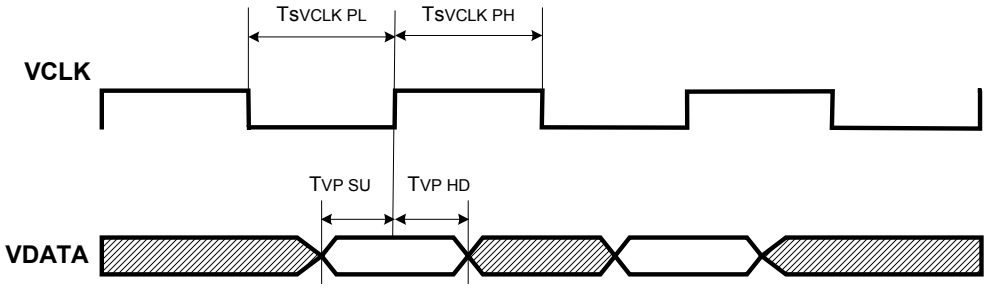


**Figure 26. Timing Diagram for ITU656 Video Port**

**Table 20. Input Timing for ITU656 Video Port**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{VP\_SU}$ | Setup time for data signals valid before VCLK edge. VCLK edge is programmable to be either rising or falling. | 2 | | nsec. |
| $T_{VP\_HD}$ | Hold time for data/control signals to remain valid after VCLK edge. | 1 | | nsec |
| $T_{VCLK\_PH}$ | VCLK high pulse width period | 3 | | nsec |
| $T_{VCLK\_PL}$ | VCLK low pulse width period | 3 | | nsec |
| $F_{VCLK}$ | VCLK maximum operating frequency. | | 28 | Mhz |

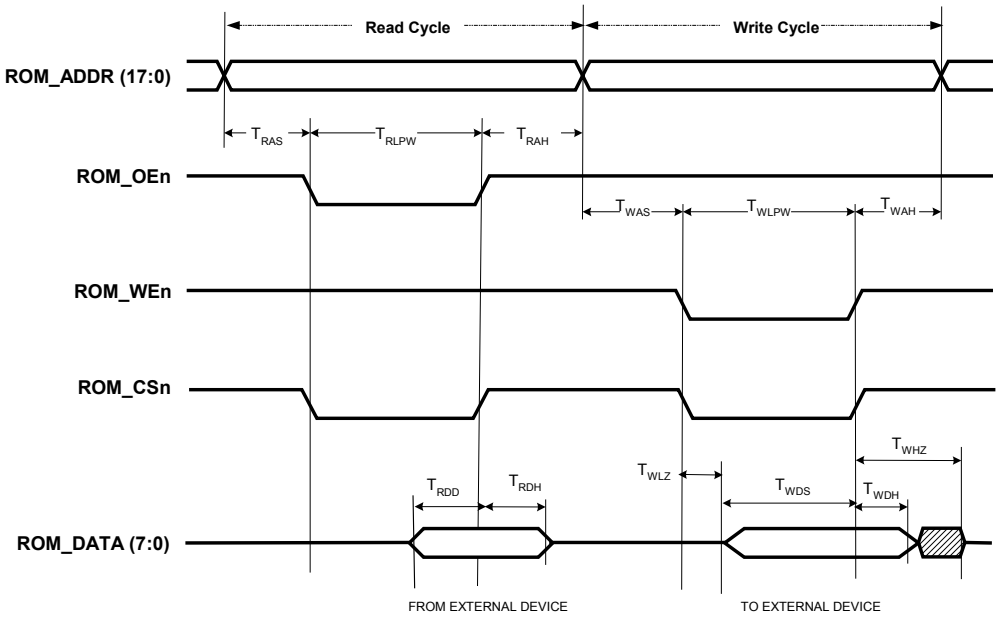


**Figure 27. OCM ROM Interface Timing Diagram**

**Table 21. OCM ROM Interface Timing**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{OCMCLK}$ | On chip OCM clock period. | 10 | | ns |
| $T_{OCM\_WAS}$ | Address setup time provided to falling edge of OCM_WR. | $K1(T_{OCMCLK}) - 3$ | | ns |
| $T_{OCM\_WAH}$ | Address hold time provided from rising edge of OCM_WR. | $T_{OCMCLK} - 3$ | | ns |
| $T_{OCM\_WLPW}$ | OCM_WR active low pulse width | $K2\ (T_{OCMCLK})$ | | ns |
| $T_{OCM\_WDS}$ | OCM_DATA valid time to OCM_WR rising edge (data set-up time provided) | $K2(T_{OCMCLK}) - 3$ | | ns |
| $T_{OCM\_WDH}$ | OCM_DATA held valid from OCM_WR rising edge. (data hold time provided) | $T_{OCMCLK} - 3$ | | ns |
| $T_{OCM\_WLZ}$ | OCM_DATA Low-Z after OCM_WEn falling edge. | -2 | 3 | ns |
| $T_{OCM\_WHZ}$ | OCM_DATA Hi-Z after OCM_WEn rising edge. | $T_{OCMCLK} - 3$ | $T_{OCMCLK} + 3$ | ns |
| $T_{OCM\_RAS}$ | Address setup time provided to falling edge of OCM_RD. | 0 | | ns |
| $T_{OCM\_RAH}$ | Address hold time provided from rising edge of OCM_RD. | $T_{OCMCLK} - 3$ | | ns |
| $T_{OCM\_RLPW}$ | OCM_RD low pulse width | $K3\ (T_{OCMCLK})$ | | ns |
| $T_{OCM\_RDD}$ | Read data valid before OCM_RD rising edge. | 10 | | ns |
| $T_{OCM\_RDH}$ | Read data hold after OCM_RD rising edge. | 0 | | ns |

**NOTE:** Conditions: For ROMC the $C_{LOAD}$ = 16 pF. For ROM_ADDR[17:0] and ROM_DATA[7:0] the $C_{LOAD}$ = 32 pF.

**NOTE:** K1, K2 and K3 are programmable in units of OCM_CLK.

# 6 Ordering Information

| Order Code | Application | High Quality ADC | Ultra-Reliable DVI™ | HDCP Content Protection | ITU656 Video Input | ACC/ACM-II Color Controls and Video Windowing | LVDS Tx | Package | Temperature Range |
|---|---|---|---|---|---|---|---|---|---|
| gm5221-LF-BC | SXGA | √ | √ | | √ | √ | 2 | 208-pin PQFP | 0-70°C |
| gm5221H-LF-BC (1) | SXGA | √ | √ | √ | √ | √ | 2 | | |

**Note (1):** gm5221H is sold to HDCP licensed customers only.

# 7 Mechanical Specifications

COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 4.10 | — | — | 0.161 |
| A1 | 0.25 | — | — | 0.010 | — | — |
| A2 | 3.20 | 3.32 | 3.60 | 0.126 | 0.131 | 0.142 |
| D | 30.60 BSC. | | | 1.205 BSC. | | |
| D1 | 28.00 BSC. | | | 1.102 BSC. | | |
| E | 30.60 BSC. | | | 1.205 BSC. | | |
| E1 | 28.00 BSC. | | | 1.102 BSC. | | |
| R2 | 0.08 | — | 0.25 | 0.003 | — | 0.010 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 8° REF | | | 8° REF | | |
| θ3 | 8° REF | | | 8° REF | | |
| c | 0.09 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.30 REF | | | 0.051 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC | | | 0.020 BSC | | |
| D2 | 25.50 | | | 1.004 | | |
| E2 | 25.50 | | | 1.004 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | — | 0.08 | — | — | 0.003 | — |
| ddd | — | 0.08 | — | — | 0.003 | — |

NOTES :
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. THE MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.
3. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.

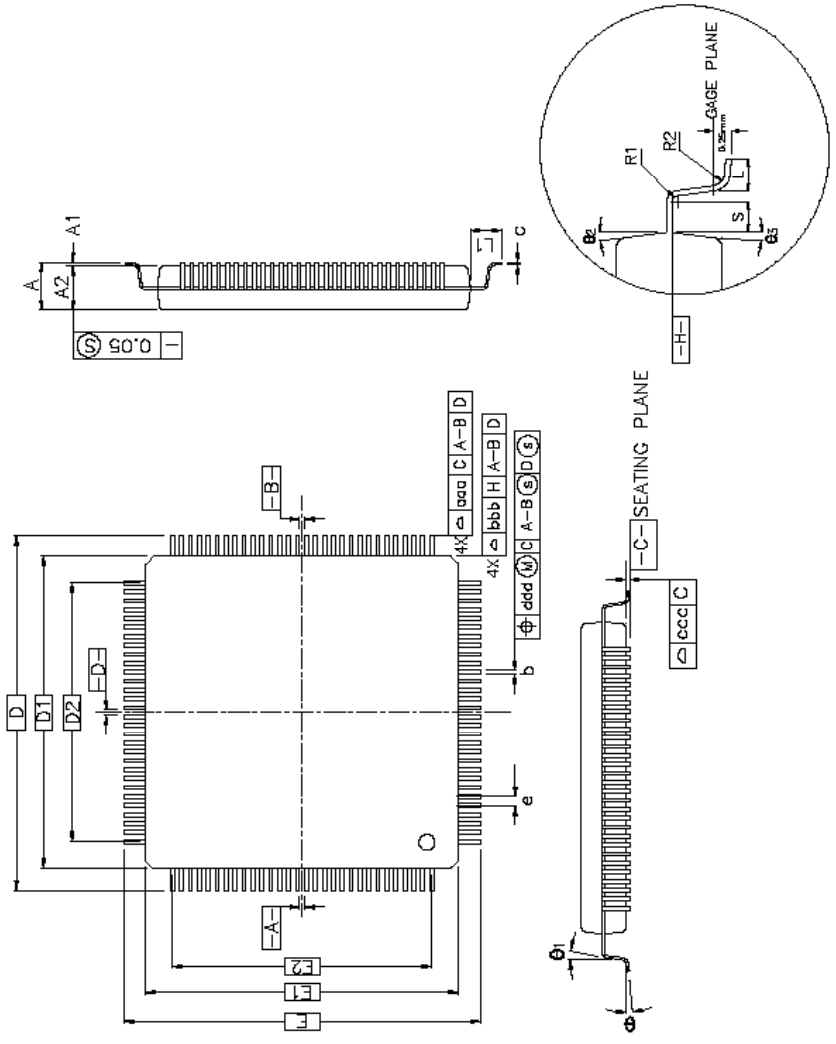


**Figure 28. gm5221 208-pin PQFP Mechanical Drawing**