4+1 Channel Voltage Buffers for TFT LCD

Introduction (General Description)

The EC5565 is a 4+1 channel voltage buffers that buffers reference voltage for gamma correction in a thin film transistor liquid crystal display (TFT LCD). This device incorporates a Vcom amplifier circuits, four rail to rail buffer amplifier circuits.

The EC5565 is available in a space saving 14-pin TSSOP package and, QFN 16L package. and the operating temperature is from –20°C to +85°C.

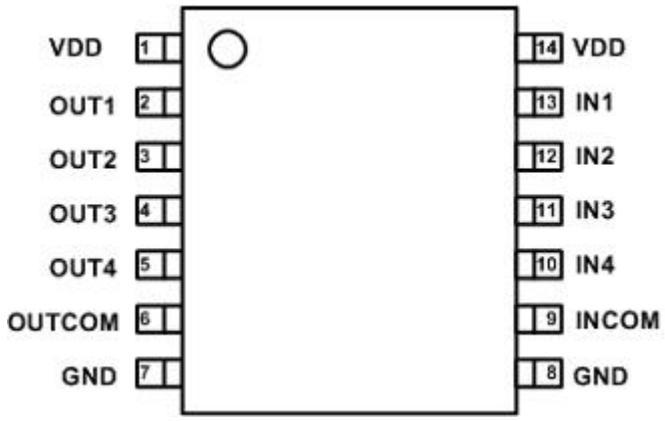
Features

- Wide supply voltage range 6.5V ~ 18V
- Rail-to-Rail output swing (The highest two stage & lowest two stage)
- High slew rate 1V/μs
- GBWP 1 MHz
- 2 MHz -3dB Bandwidth
- Large Vcom Drive Current: ±100mA(Max.)
- Ultra-small Package TSSOP-14 and QFN 16L.

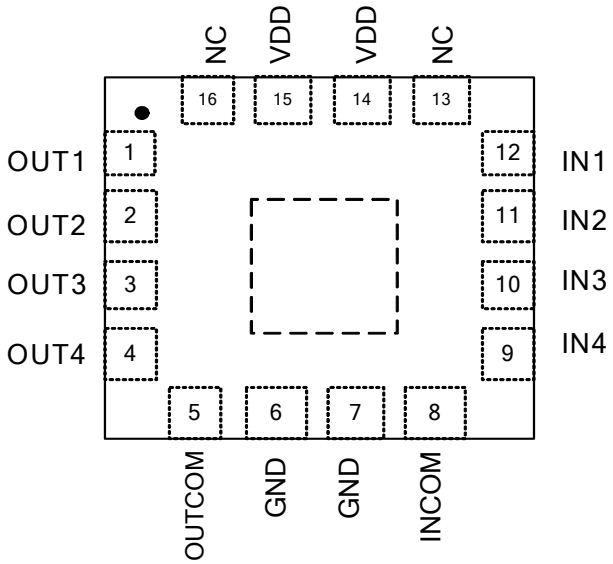
Applications

- TFT-LCD Reference Driver

Pin Assignment For TSSOP-14



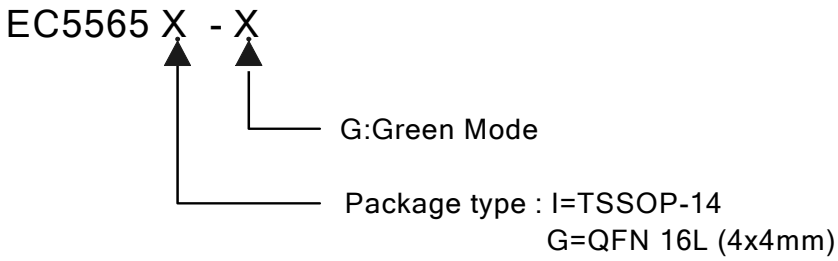
Pin Assignment For QFN 16L (Top View)



Ordering Information

PART NUMBER	MAKING	PACKAGE
EC5565I	AS05	TSSOP-14
EC5565I-G	AS05-G	GREEN Mode, TSSOP-14
EC5565G-G	AS05-G	GREEN Mode, QFN 16L (4x4 mm)

Ordering Information



Absolute maximum ratings (TA = 25 °C)

Values beyond absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional device operation is not implied. Exposure to AMR conditions for extended periods may affect device reliability. .

Parameter	Symbol	Value	Unit
Supply Voltage between V_{S+} and V_{S-}	Vs	+18	V
Input Voltage (For rail to rail)	Vin	V_{S-} -0.5	V
		V_{S+} +0.5	V
Maximum Output Current (1 ~ 4 Buffers)	Iout	±30	mA
Maximum Output Current (Com Buffer)	Iout(com)	±100	mA
Maximum Junction Temperature	TJ	+125	°C
Storage Temperature Range	TSTG	-65 to +150	°C
Operating Temperature Range	TOP	-20 to +85	°C
Lead temperature	Tlead	260	°C
ESD Voltage	VESD	2	KV

Important Note:

All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Characteristics

(Typical Performance Characteristics)

V_{S+}= +5V, V_{S-} = -5V, R_L = 10kΩ and C_L = 10pF to 0V, T_A = 25°C unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Units
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM}= 0V		2	12	mV
TCV_{OS}	Average Offset Voltage Drift	[1]		5		µV/°C
I_B	Input Bias Current	V_{CM}= 0V		2	50	nA
R_{IN}	Input Impedance			1		G
C_{IN}	Input Capacitance			1.35		pF
Output Characteristics						
V_{OL}	Output Swing Low	I_L= -5mA (O1, O2, O3, O4 rail-to-rail Buffers)		-4.92	-4.85	V
V_{OH}	Output Swing High	I_L= 5mA (O1, O2, O3, O4 rail-to-rail Buffers)	4.85	4.92		V
I_{SC}	Short Circuit Current	(Out1 ~ Out4 Buffers)		±120		mA
I_{OUT}	Output Current	(Out1 ~ Out4 Buffers)		±30		mA
$I_{SC(Com)}$	Short Circuit Current	(Com Buffer)		±300		mA
$I_{OUT(Com)}$	Output Current	(Com Buffer)		±100		mA
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±3.25V to ±7.75V	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load (Out1 ~ Out4 Buffers)		500	750	µA
$I_{S(Com)}$	Supply Current	(Com Buffer)		2.5		mA
Dynamic Performance						
SR	Slew Rate [2]	-4.0V≦V_{OUT}≦4.0V, 20% to 80%		1		V/µs
t_S	Settling to +0.1% (AV = +1)	(AV = +1), V_O=2V Step		5		µs
BW	-3dB Bandwidth	RL = 10KΩ, CL = 10PF		2		MHz
PM	Phase Margin	RL = 10KΩ, CL = 10PF		60		Degrees
CS	Channel Separation	f = 1 MHz		75		dB

1. Measured over operating temperature range

2. Slew rate is measured on rising and falling edges

Typical Performance Characteristics

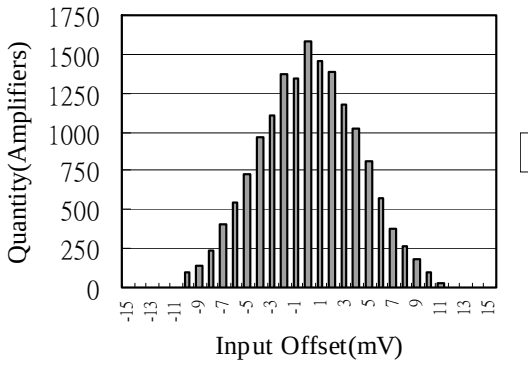


Figure (a) Input Offset Voltage Distribution

VCC = 10V , F :10K

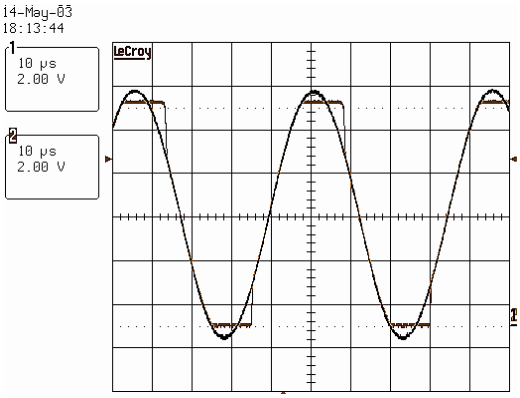


Figure (b) Input beyond the rails

VCC = 10V , F :10K

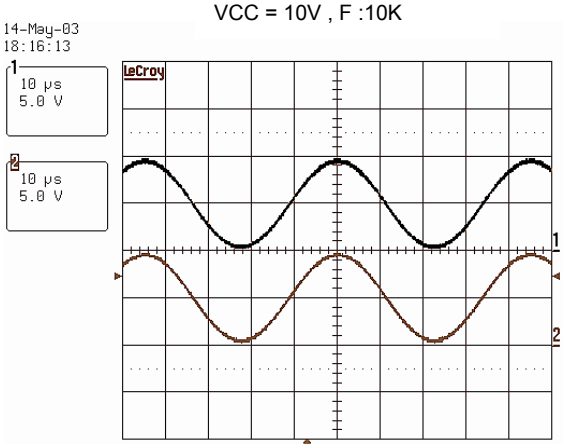


Figure (c) Rail to Rail Capability

VCC = 10V , F :1K

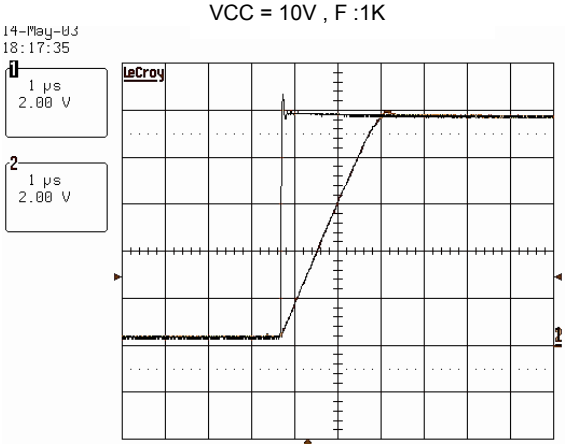


Figure (d) Large Signal Transient Response

VCC = 10V , F :1K

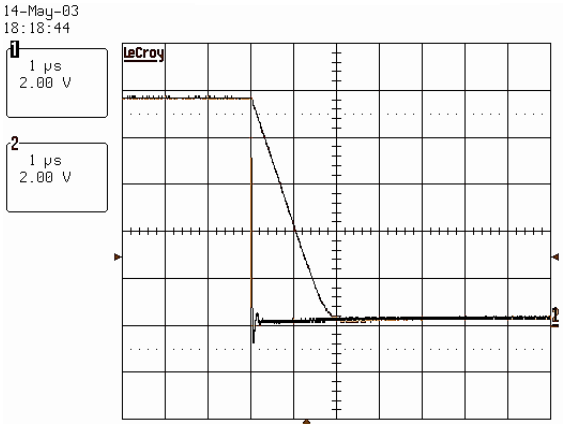


Figure (e) Large Signal Transient Response

VCC = 10V , F :1K

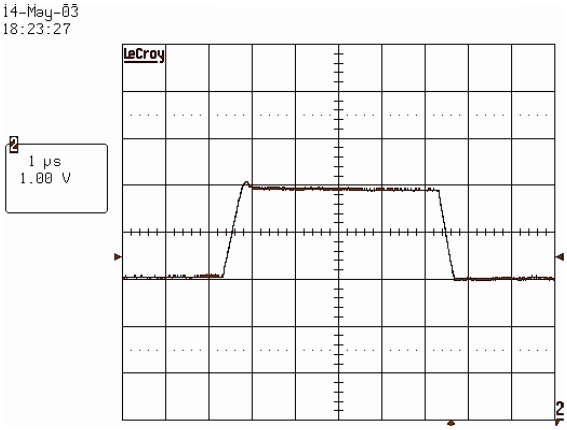


Figure (f) Small Signal Transient Response

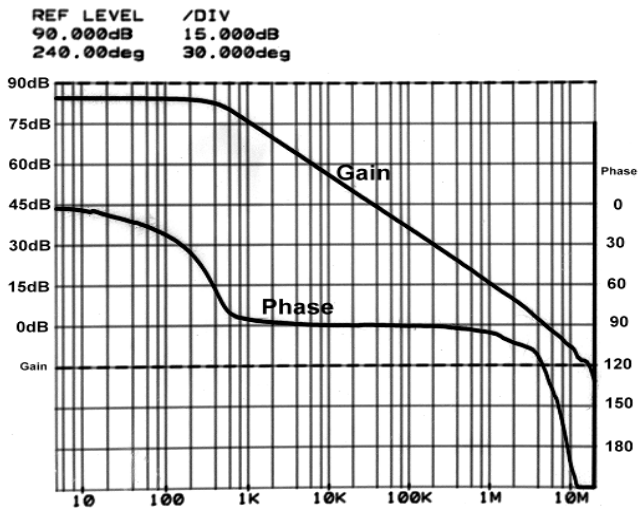


Figure (g) Open Loop Gain & Phase vs. Frequency

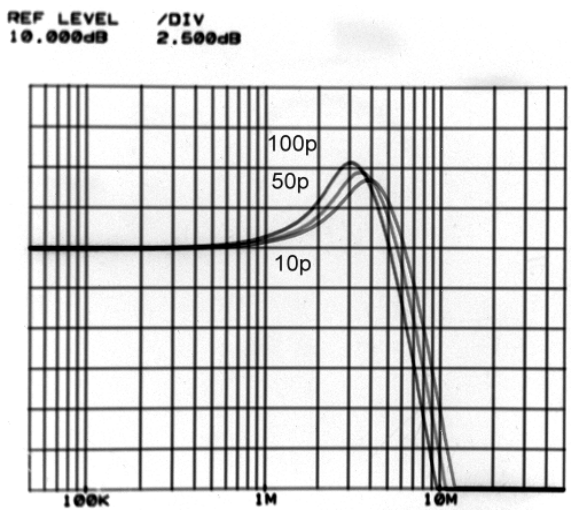


Figure (h) Frequency Response for Various C_L

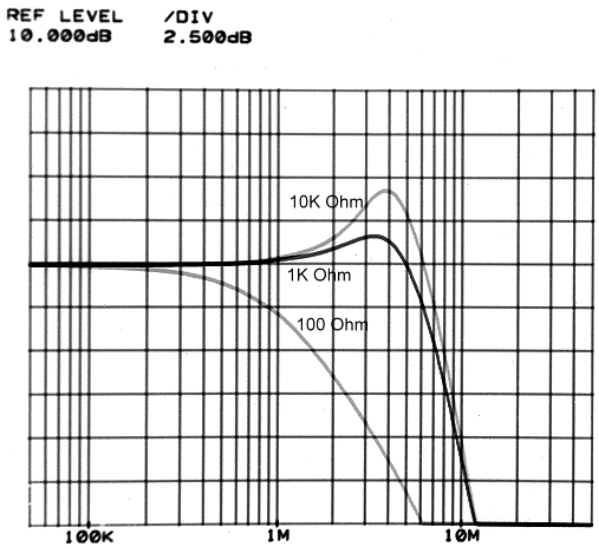


Figure (i) Frequency Response for Various R_L

Applications Information

Product Description

The EC5565 rail-to-rail 5 channels amplifier is built on an advanced high voltage CMOS process. It's beyond rails input capability and full swing of output range made itself an ideal amplifier for use in a wide range of general-purpose applications. The features of 1μS high slew rate, fast settling time, 2MHz of GBWP as well as high output driving capability have proven the EC5565 a good voltage reference buffer in TFT-LCD for grayscale reference applications. High phase margin and extremely low power consumption (500μA per amplifier) make the EC5565 ideal for Connected in voltage follower mode for low power high drive applications

Supply Voltage, Input Range and Output Swing

The EC5565 can be operated with a single nominal wide supply voltage ranging from 6.5V to 18V with stable performance over operating temperatures of -20 °C to +85 °C.

With 500mV greater than rail-to-rail input common mode voltage range and 75dB of Common Mode Rejection Ratio, the EC5565 allows a wide range sensing among many applications without having any concerns over exceeding the range and no compromise in accuracy. The output swings of the EC5565 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. The output voltage swing can be even closer to the supply rails by merely decreasing the load current. Figure 1 shows the input and output waveforms for the device in the unity-gain configuration. The amplifier is operated under ±5V supply with a 10k. load connected to GND. The input is a 10Vp-p sinusoid. An approximately 9.985 Vp-p of output voltage swing can be easily achieved.

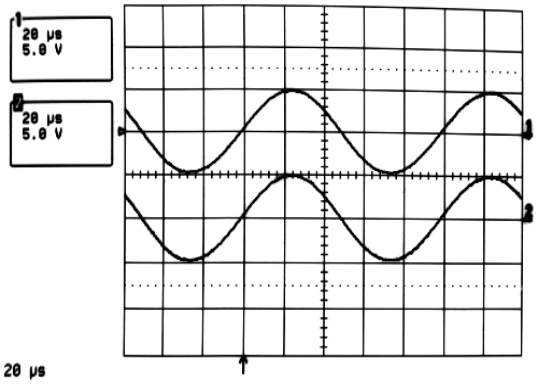


Figure 1. Operation with Rail-to-Rail Input and Output

Output Short Circuit Current Limit

A +/-120mA short circuit current will be limited by the EC5565 if the output is directly shorted to the positive or the negative supply. For an indefinitely output short circuit, the power dissipation could easily increase such that the device may be damaged. The internal metal interconnections are well designed to prevent the output continuous current from exceeding +/-30 mA such that the maximum reliability can be well maintained.

Output Phase Reversal

The EC5565 is designed to prevent its output from being phase reversal as long as the input voltage is limited from V_{S-} −0.5V to V_{S+} +0.5V. Figure 2 shows a photo of the device output with its input voltage driven beyond the supply rails. Although the phase of the device's output will not be reversed, the input's over-voltage should be avoided. An improper input voltage exceeds supply range by more than 0.6V may result in an over stress damage.

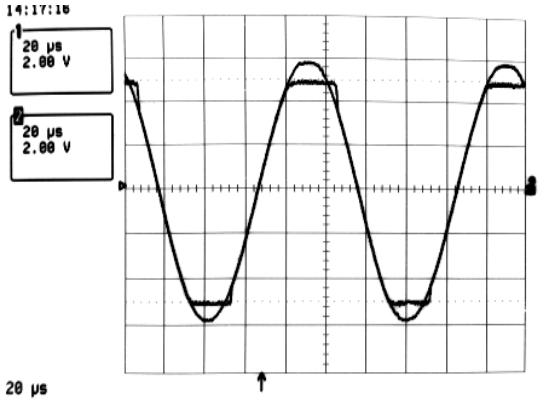


Figure 2. Operation with Beyond-the Rails Input

Power Dissipation

The EC5565 is designed for maximum output current capability. Even though momentary output shorted to ground causes little damage to the device.

For the high drive amplifier EC5565, it is possible to exceed the 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area. The maximum power dissipation allowed in a package is determined according to:

$$P_{Dmax} = \frac{T_{Jmax} - T_{Amax}}{\Theta_{JA}}$$

Where:

$\mathbf{T_{Jmax}}$ = Maximum Junction Temperature

$\mathbf{T_{Amax}}$= Maximum Ambient Temperature

$\mathbf{\Theta_{JA}}$ = Thermal Resistance of the Package

$\mathbf{P_{Dmax}}$ = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$\mathbf{P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_{S+} - V_O) * I_L]}$

When sourcing, and

$\mathbf{P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_O - V_{S-}) * I_L]}$

When sinking.

Where:
i = 1 to 4
$\mathbf{V_S}$ = Total Supply Voltage
$\mathbf{I_{Smax}}$ = Maximum Supply Current Per Amplifier
$\mathbf{V_O}$ = Maximum Output Voltage of the Application
$\mathbf{I_L}$ = Load current
$\mathbf{R_L}$ = Load Resistance = $(\mathbf{V_{S+} - V_O})/\mathbf{I_L} = (\mathbf{V_O - V_{S-}})/\mathbf{I_L}$
A calculation for R_L to prevent device from overheat can be easily solved by setting the two P_{Dmax} equations equal to each other.

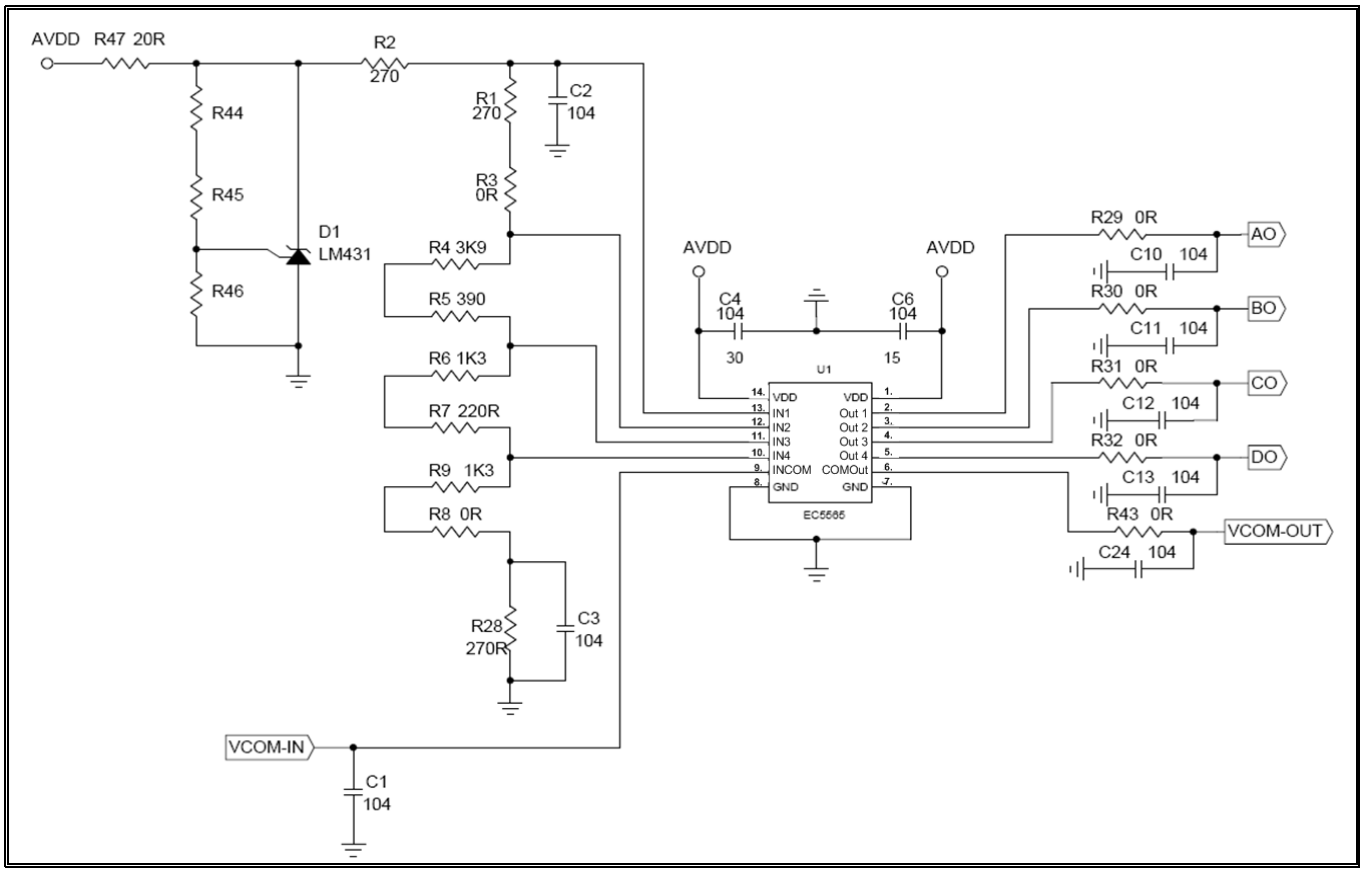
Pin Count	Θja (℃/W)	Θjc (℃/W)
TSSOP-14	100	17
QFN 16L	43	8

Driving Capacitive Loads
The EC5565 is designed to drive a wide range of capacitive loads. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features make the EC5565 ideally for applications such as TFT LCD panel grayscale reference voltage buffers, ADC input amplifiers, etc.

As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The amplifiers drive 10pF loads in parallel with10KΩ. with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ωand 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it improves the settling and overshooting performance while does not draw any DC load current or reduce the gain.

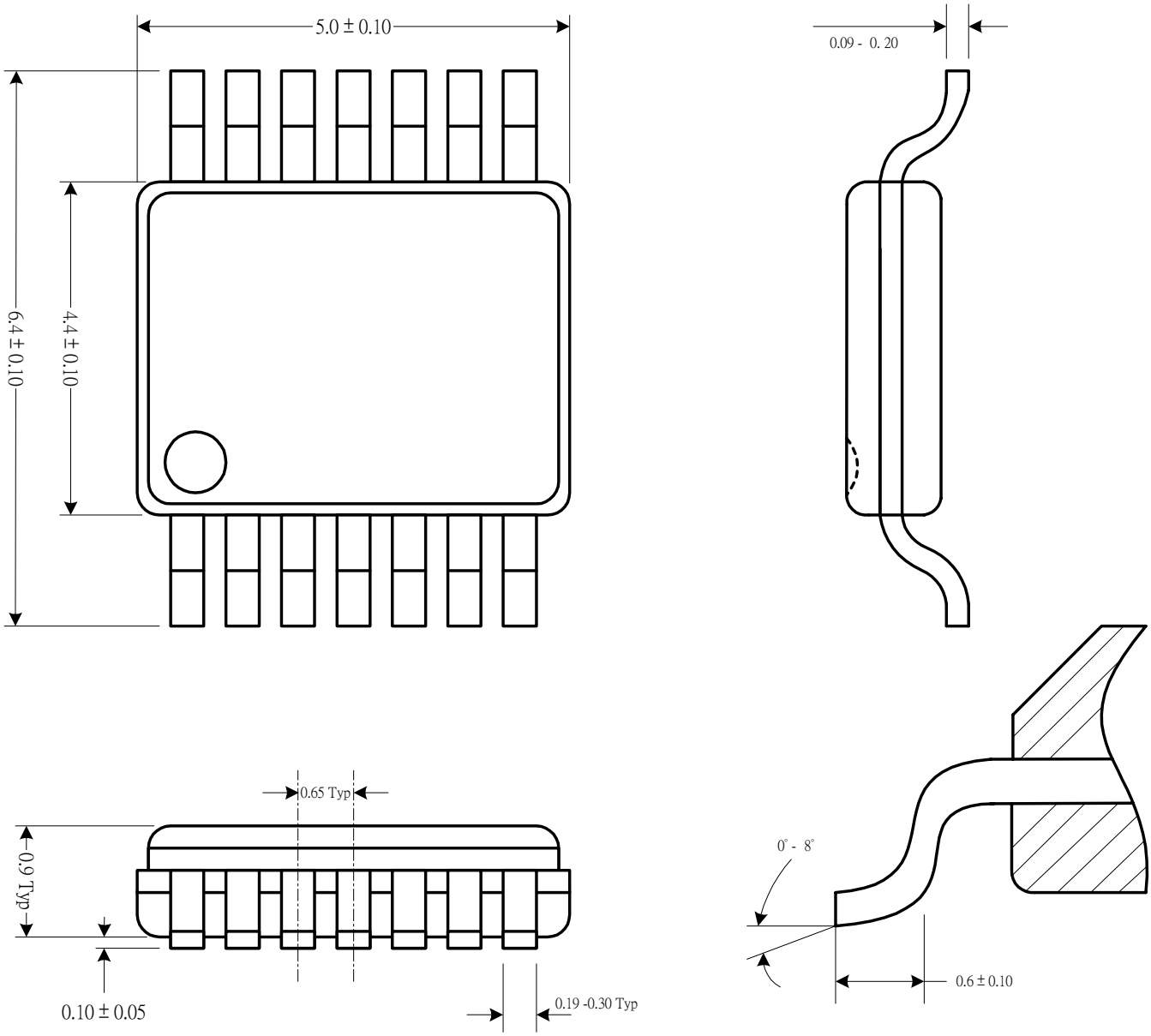
Power Supply Bypassing and Printed Circuit Board Layout
With high phase margin, the EC5565 performs stable gain at high frequency. Like any high-frequency device, good layout of the printed circuit board usually comes with optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1 μF ceramic capacitor should be placed from V_{S+} pin to V_{S-} pin as a bypassing capacitor. A 4.7μF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7μF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Applications Circuits



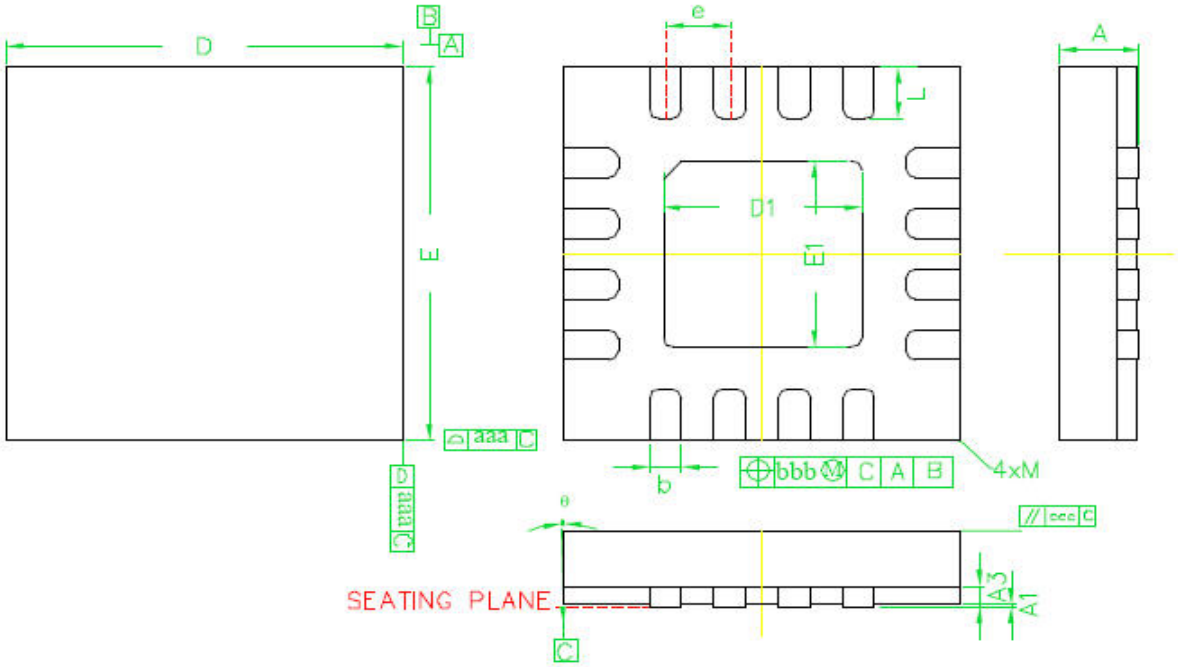
Outline Dimensions (Dimensions shown in millimeters)

TSSOP-14



Outline Dimensions

QFN 16L (4x4 mm)



DIMN	Millimeters		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.015	0.030
A3	—	0.20REF.	—
b	0.15	0.20	0.25
D	3.90	4.00BSC	4.10
D1	2.50	2.60	2.70
E	3.90	4.00BSC	4.10
E1	2.50	2.60	2.70
e	—	0.65BSC	—
L	0.32	0.40	0.48
Q	-12	—	0
aaa	—	0.25	—
bbb	—	0.10	—
ccc	—	0.10	—
M	—	—	0.05
Burr	0	0.030	0.060

NOTE

1. ALL DIMENSIONS ARE IN MILLMETER, Q IS IN DEGREES.
2. M: THE MAXIMUM ALLOW ABLE CORNER ON THE MOLDED PLASTIC BODY CORNERS.
3. DIMENSION D DOES NOT INCLUDES MOLD PROTRUSIONS OR GATE BURRS.MOLD PROTRUSIONDS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
4. DIMENSION E DOES NOT INCLUDES INTERTERMINAL MOLD PROTRUSIONS OR TERMINAL PROTRUSIONS.INTERMINAL MOLD PROTRUSIONS AND/OR TERMINAL PROTRUSIONS SHALL NOT EXCEED 0.20 mm PER SIDE.
5. DIMENSION b APPLIES TO PLATED TERMINALS.DIMENSION A1 IS PRIMARILY Y TERMINAL PLATING, BUT MAY OR MAY NOT INCLUDE A SMALL PROTRUSION OF TERMINAL BELOW THE BOTTOM SURFACE OF THE PACKAGE.
6. JEDEC STANDARD MO-220.