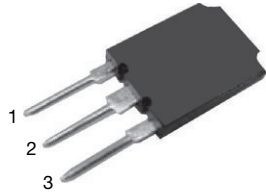
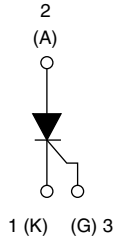




## Thyristor High Voltage, Phase Control SCR, 70 A



Super TO-247



### FEATURES

- High surge capability
- High voltage input rectification
- Designed and qualified according to JEDEC®-JESD47
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS COMPLIANT

### APPLICATIONS

- AC switches
- High voltage input rectification (soft start)
- High current crow-bar
- Other phase-control circuits
- Designed to be used with Vishay input diodes, switches, and output rectifiers which are available in identical package outlines

### DESCRIPTION

The VS-70TPS..PbF high voltage series of silicon controlled rectifiers are specifically designed for high and medium power switching, and phase control applications.

PRODUCT SUMMARY	
Package	Super TO-247
Diode variation	Single SCR
$I_{T(AV)}$	70 A
$V_{DRM}/V_{RRM}$	1200 V, 1600 V
$V_{TM}$	1.25 V
$I_{GT}$	100 mA
$T_J$	-40 °C to 125 °C

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$	Sinusoidal waveform	70	A
$I_{RMS}$	Lead current limitation	75	
$V_{RRM}/V_{DRM}$	Range	1200/1600	V
$I_{TSM}$		1100	A
$V_T$	100 A, $T_J = 25\text{ °C}$	1.4	V
dV/dt		500	V/μs
dI/dt		150	A/μs
$T_J$		-40 to 125	°C

VOLTAGE RATINGS			
PART NUMBER	$V_{RRM}/V_{DRM}$ , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}/I_{DRM}$ AT 125 °C mA
VS-70TPS12PbF	1200	1300	15
VS-70TPS16PbF	1600	1700	



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current	$I_{T(AV)}$	$T_C = 82\text{ }^\circ\text{C}$ , 180° conduction half sine wave		70	A
Maximum continuous RMS on-state current as AC switch	$I_{T(RMS)}$	Lead current limitation		75	
Maximum peak, one-cycle non-repetitive surge current	$I_{TSM}$	10 ms sine pulse, rated $V_{RRM}$ applied		930	A <sup>2</sup> s
		10 ms sine pulse, no voltage reapplied		1100	
Maximum $I^2t$ for fusing	$I^2t$	10 ms sine pulse, rated $V_{RRM}$ applied		4325	
		10 ms sine pulse, no voltage reapplied		6115	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms to }10\text{ ms}$ , no voltage reapplied		61 150	A <sup>2</sup> √s
Low level value of threshold voltage	$V_{T(TO)1}$	$T_J = 125\text{ }^\circ\text{C}$		0.916	V
High level value of threshold voltage	$V_{T(TO)2}$			1.21	
Low level value of on-state slope resistance	$r_{t1}$			4.138	mΩ
High level value of on-state slope resistance	$r_{t2}$			3.43	
Maximum peak on-state voltage	$V_{TM}$	100 A, $T_J = 25\text{ }^\circ\text{C}$		1.4	V
Maximum rate of rise of turned-on current	$di/dt$	$T_J = 25\text{ }^\circ\text{C}$		150	A/μs
Maximum holding current	$I_H$	Anode supply = 6 V, resistive load, initial $I_T = 1\text{ A}$ , $T_J = 25\text{ }^\circ\text{C}$		200	mA
Maximum latching current	$I_L$	Anode supply = 6 V, resistive load, $T_J = 25\text{ }^\circ\text{C}$		400	
Maximum reverse and direct leakage current	$I_{RRM}/I_{DRM}$	$T_J = 25\text{ }^\circ\text{C}$		1.0	
		$T_J = 125\text{ }^\circ\text{C}$		15	
Maximum rate of rise of off-state voltage	$dV/dt$	$T_J = 125\text{ }^\circ\text{C}$		500	V/μs

TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	$P_{GM}$	$T = 30\text{ }^\mu\text{s}$		10	W
Maximum average gate power	$P_{G(AV)}$			2.5	
Maximum peak gate current	$I_{GM}$			2.5	A
Maximum peak negative gate voltage	$-V_{GM}$			10	V
Maximum required DC gate voltage to trigger	$V_{GT}$	$T_J = -40\text{ }^\circ\text{C}$		1.8	
		$T_J = 25\text{ }^\circ\text{C}$		1.5	
		$T_J = 125\text{ }^\circ\text{C}$		1.1	
Maximum required DC gate current to trigger	$I_{GT}$	$T_J = -40\text{ }^\circ\text{C}$		150	mA
		$T_J = 25\text{ }^\circ\text{C}$		100	
		$T_J = 125\text{ }^\circ\text{C}$		80	
Maximum DC gate voltage not to trigger	$V_{GD}$	$T_J = 125\text{ }^\circ\text{C}$ , $V_{DRM} = \text{Rated value}$		0.25	V
Maximum DC gate current not to trigger	$I_{GD}$			6	mA



THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction temperature range	$T_J$		-40 to 125	°C
Maximum storage temperature range	$T_{Stg}$		-40 to 150	
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation	0.27	°C/W
Maximum thermal resistance, junction to ambient	$R_{thJA}$		40	
Typical thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth and greased	0.2	
Approximate weight			6	g
			0.21	oz.
Mounting torque	minimum		6 (5)	kgf · cm (lbf · in)
	maximum		12 (10)	
Marking device		Case style Super TO-247	70TPS12	
			70TPS16	

$\Delta R_{thJ-hs}$ CONDUCTION PER JUNCTION											
DEVICE	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VS-70TPS..PbF	0.078	0.092	0.117	0.172	0.302	0.053	0.092	0.125	0.180	0.306	°C/W

**Note**

- The table above shows the increment of thermal resistance  $R_{thJ-hs}$  when devices operate at different conduction angles than DC

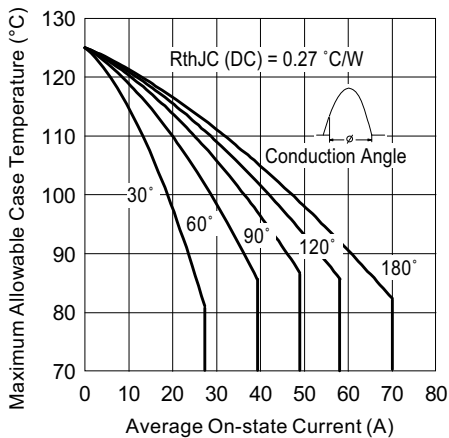


Fig. 1 - Current Rating Characteristics

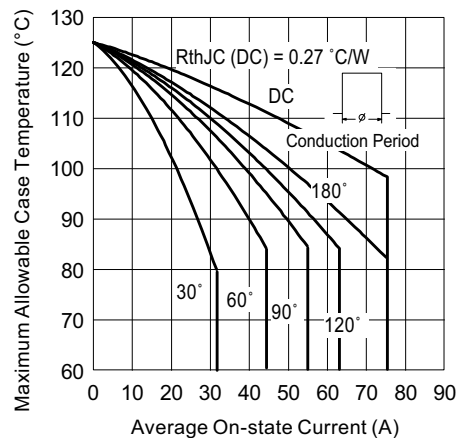


Fig. 2 - Current Rating Characteristics

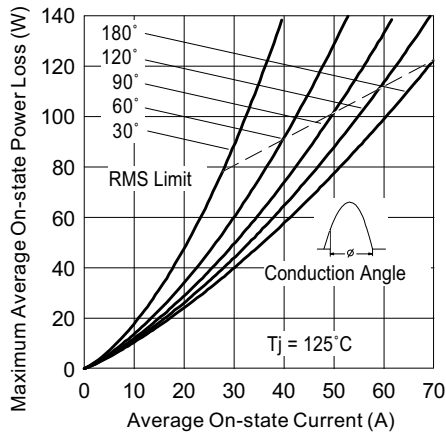


Fig. 3 - On-State Power Loss Characteristics

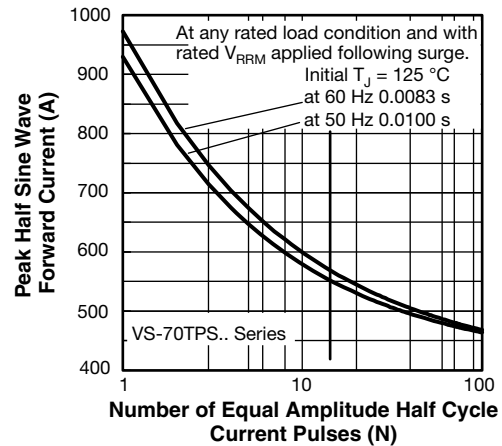


Fig. 5 - Maximum Non-Repetitive Surge Current

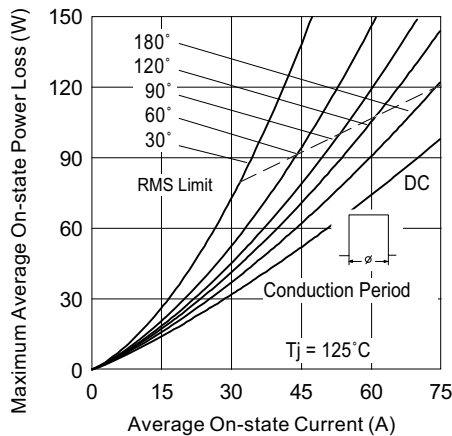


Fig. 4 - On-State Power Loss Characteristics

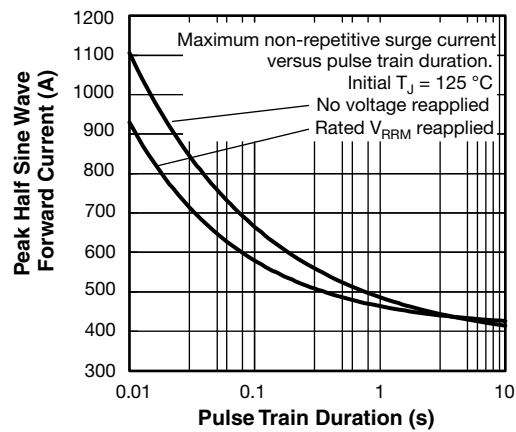


Fig. 6 - Maximum Non-Repetitive Surge Current

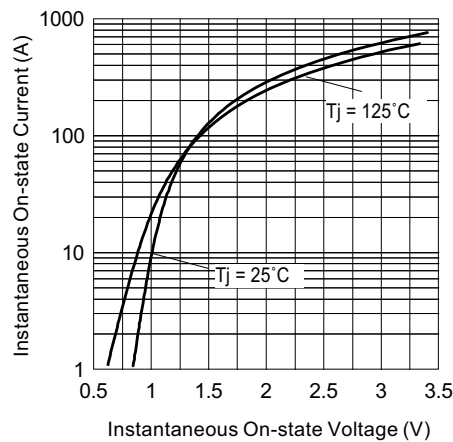


Fig. 7 - On-State Voltage Drop Characteristics

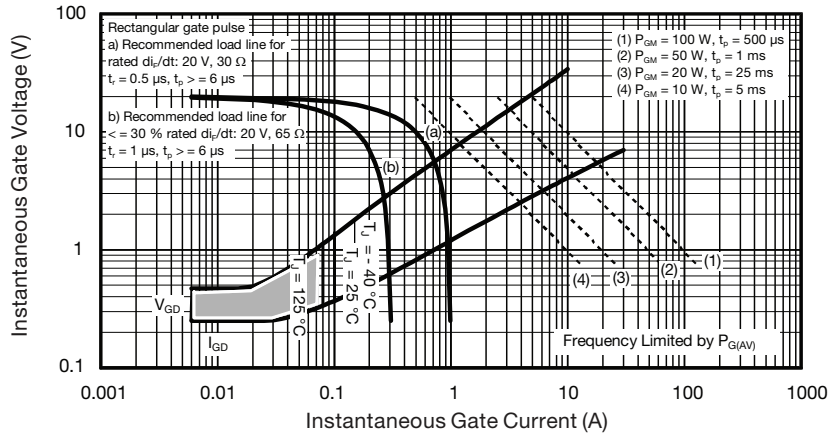


Fig. 8 - Gate Characteristics

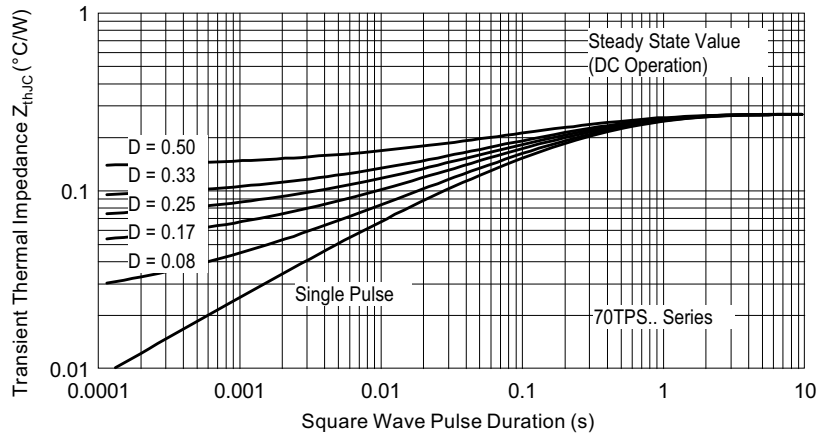
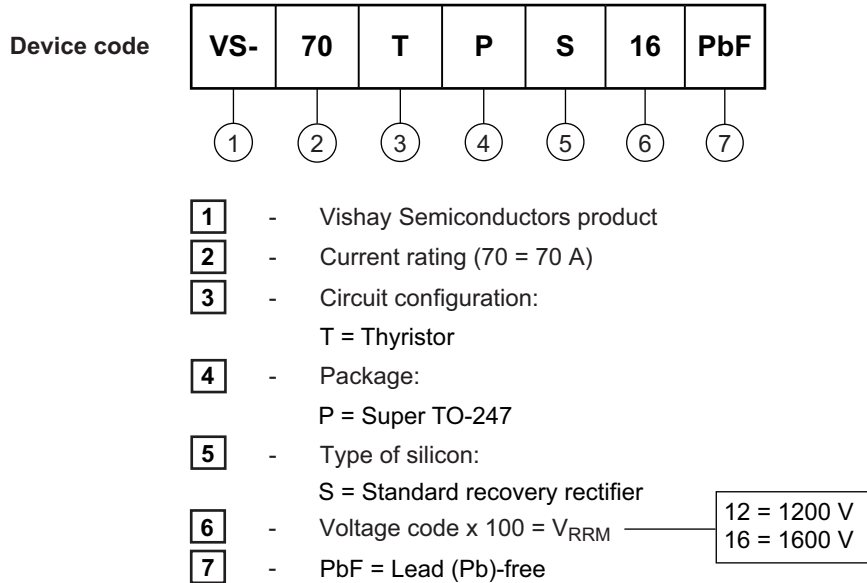


Fig. 9 - Thermal Impedance  $Z_{thJC}$  Characteristics



## ORDERING INFORMATION TABLE



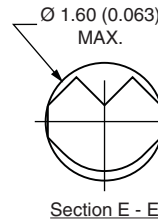
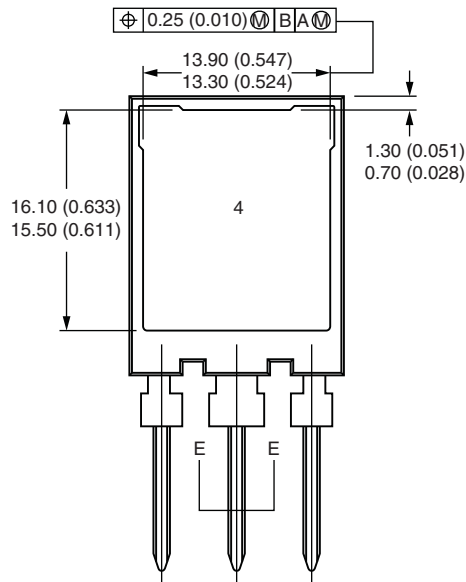
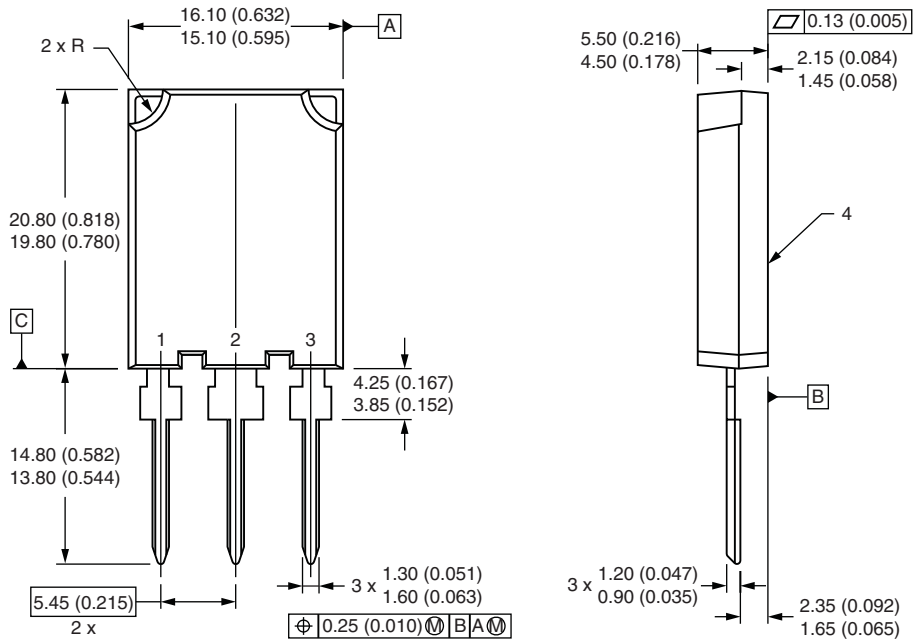
ORDERING INFORMATION (example)			
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-70TPS12PbF	25	500	Antistatic plastic tube
VS-70TPS16PbF	25	500	Antistatic plastic tube

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95073">www.vishay.com/doc?95073</a>
Part marking information	<a href="http://www.vishay.com/doc?95070">www.vishay.com/doc?95070</a>



### Super TO-247

**DIMENSIONS** in millimeters (inches)



#### Lead assignments

MOSFET	IGBT
1 - Gate	1 - Gate
2 - Drain	2 - Collector
3 - Source	3 - Emitter
4 - Drain	4 - Collector

#### Notes

- (1) Dimension and tolerancing per ASME Y14.5M-1994
- (2) Controlling dimension: millimeter
- (3) Outline conforms to JEDEC® outline TO-274AA



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