2SK3069

Silicon N Channel MOS FET
High Speed Power Switching

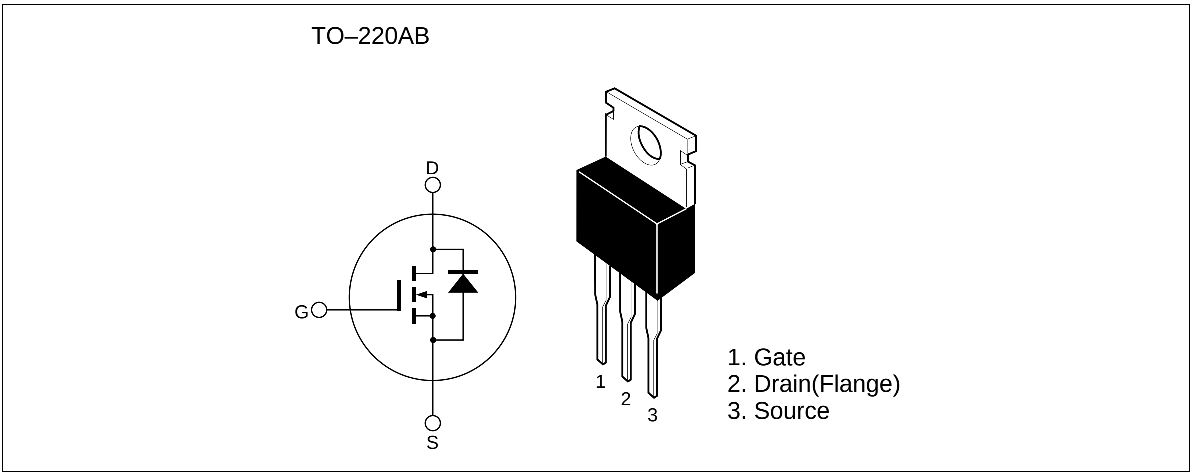
HITACHI

ADE-208-694I (Z)
10th. Edition
February 1999

Features

- Low on-resistance
  $R_{DS(on)}$ = 6 mΩ typ.
- Low drive current
- 4 V gate drive device can be driven from 5 V source

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}$ Note 1	300	A
Body-drain diode reverse drain current	I_{DR}	75	A
Avalanche current	I_{AP} Note 3	50	A
Avalanche energy	E_{AR} Note 3	214	mJ
Channel dissipation	Pch Note 2	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

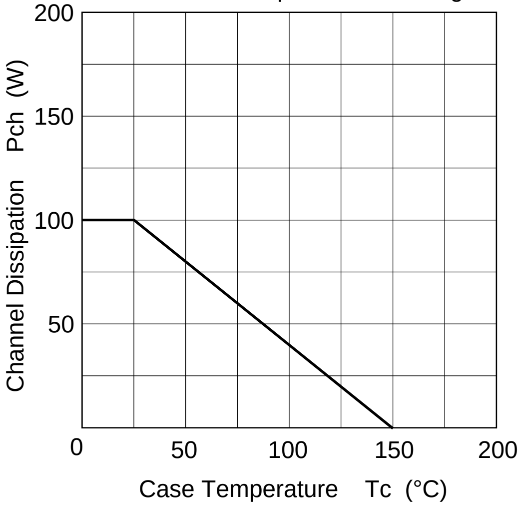
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V Note 1
Static drain to source on state resistance	$R_{DS(on)}$	—	6.0	7.5	mΩ	I_D = 40 A, V_{GS} = 10 V Note 1
		—	8.0	12	mΩ	I_D = 40 A, V_{GS} = 4 V Note 1
Forward transfer admittance	$\|y_{fs}\|$	50	80	—	S	I_D = 40 A, V_{DS} = 10 V Note 1
Input capacitance	Ciss	—	7100	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1000	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	280	—	pF	f = 1 MHz
Total gate charge	Qg	—	125	—	nc	V_{DD} = 25 V
Gate to source charge	Qgs	—	25	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	25	—	nc	I_D = 75 A
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	V_{GS} = 10 V, I_D = 40 A
Rise time	t_r	—	300	—	ns	R_L = 0.75 Ω
Turn-off delay time	$t_{d(off)}$	—	520	—	ns	
Fall time	t_f	—	330	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.05	—	V	I_F = 75 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	90	—	ns	I_F = 75 A, V_{GS} = 0 diF/ dt = 50 A/ µs

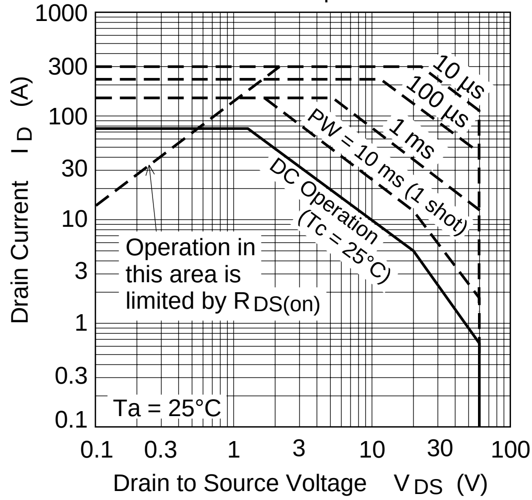
Note: 1. Pulse test

Main Characteristics

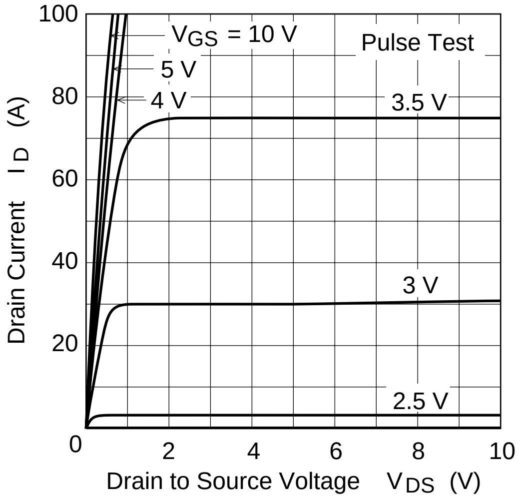
Power vs. Temperature Derating



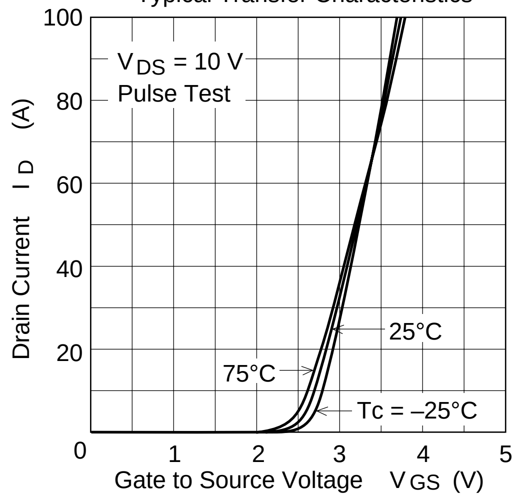
Maximum Safe Operation Area



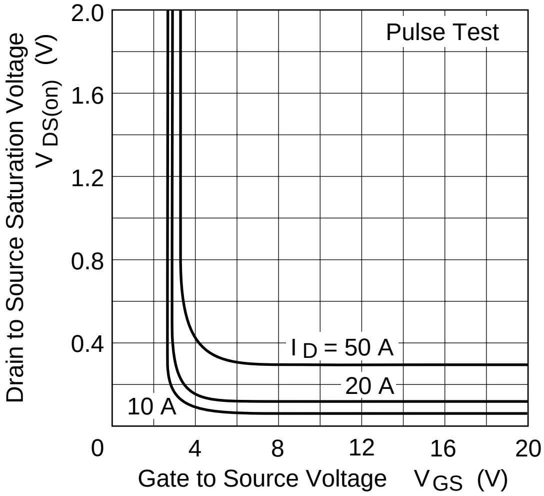
Typical Output Characteristics



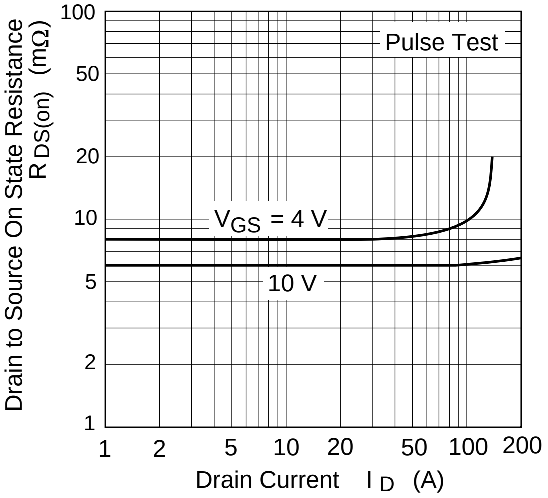
Typical Transfer Characteristics



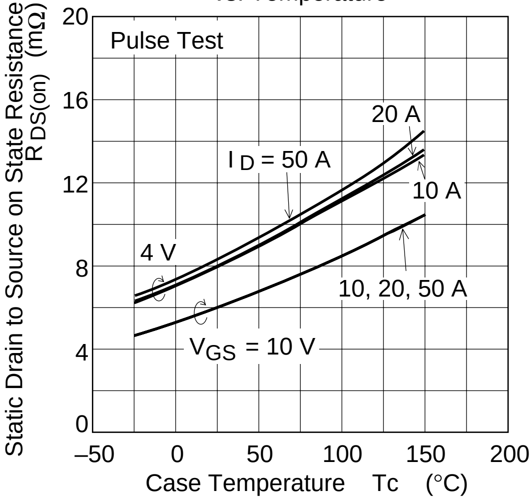
Drain to Source Saturation Voltage vs. Gate to Source Voltage



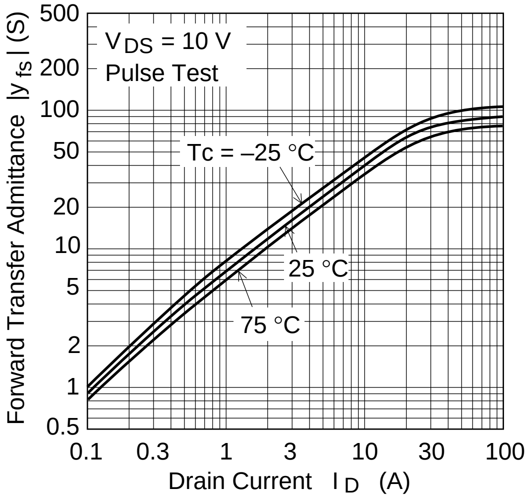
Static Drain to Source on State Resistance vs. Drain Current



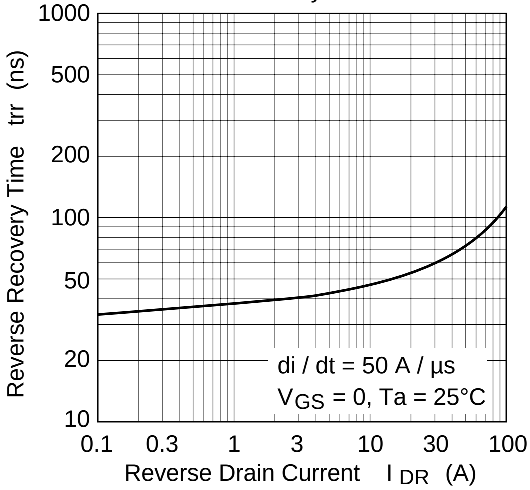
Static Drain to Source on State Resistance vs. Temperature



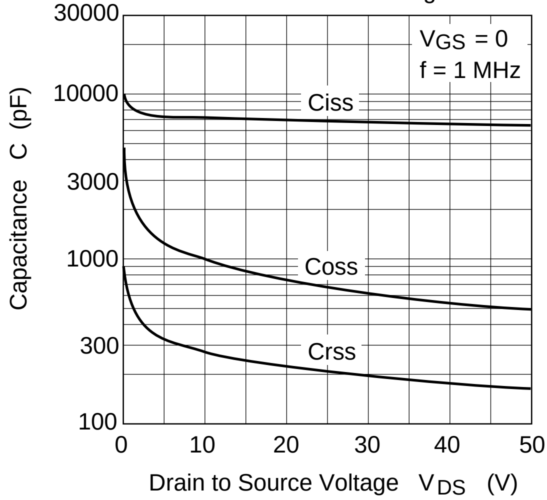
Forward Transfer Admittance vs. Drain Current



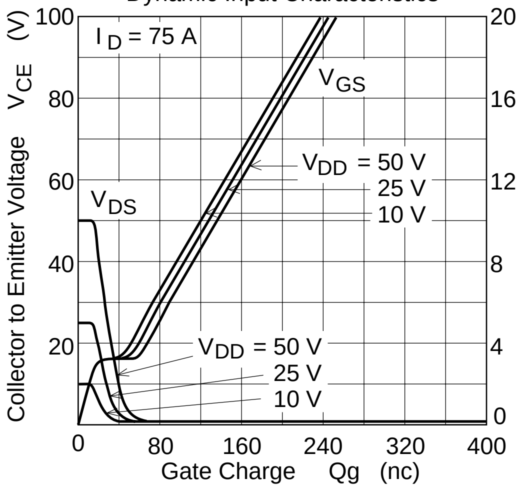
Body–Drain Diode Reverse Recovery Time



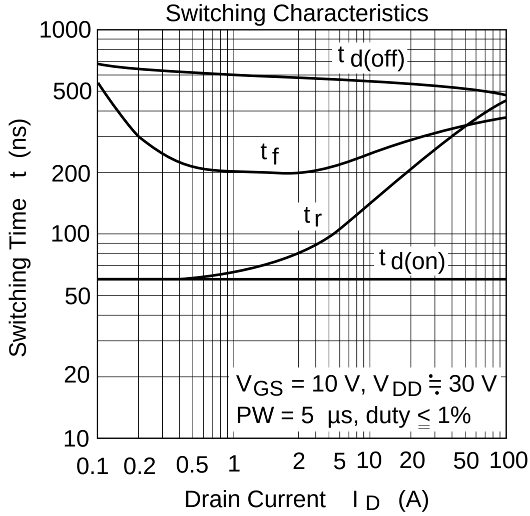
Typical Capacitance vs. Drain to Source Voltage

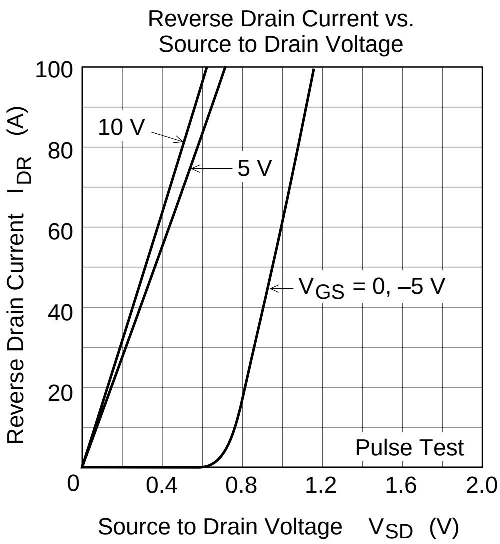


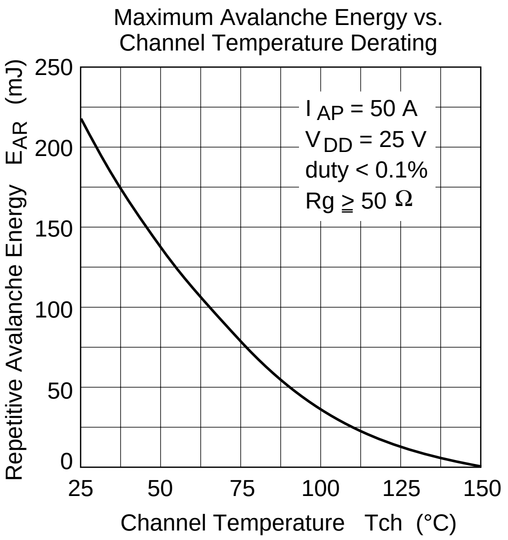
Dynamic Input Characteristics



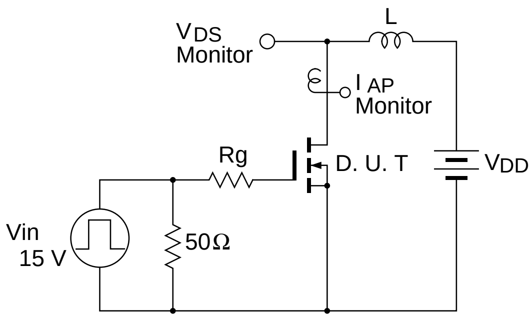
Switching Characteristics





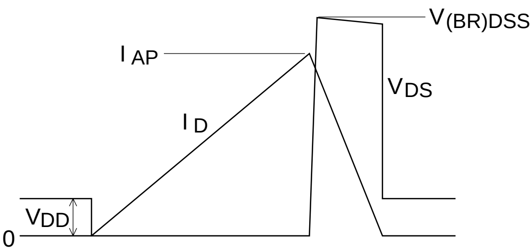


Avalanche Test Circuit

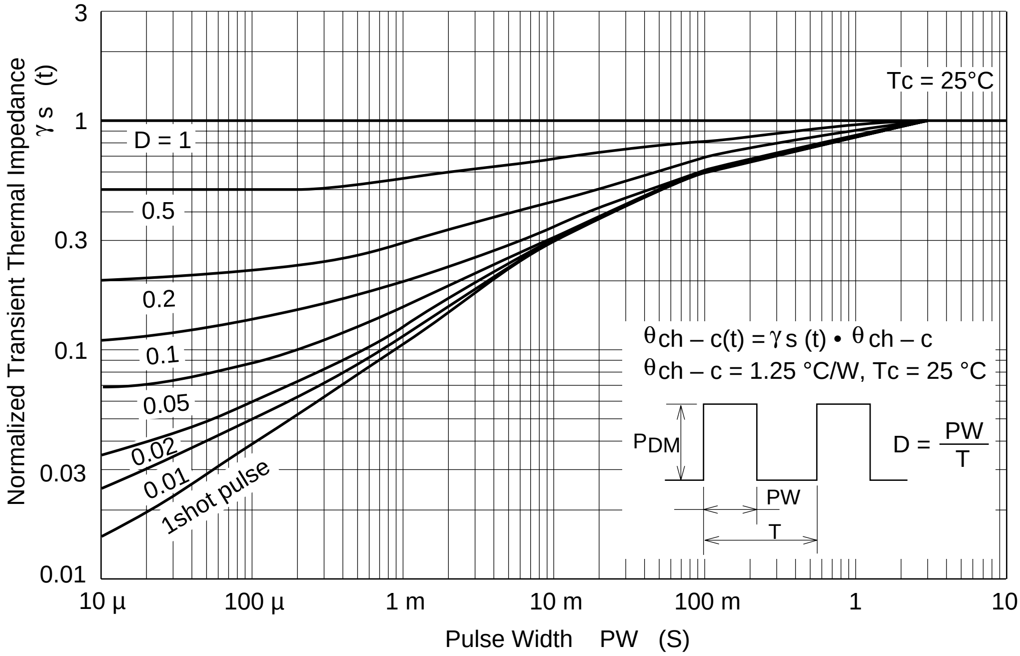


Avalanche Waveform

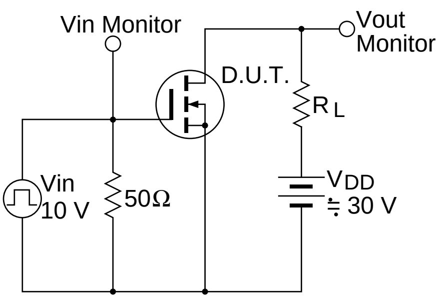
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



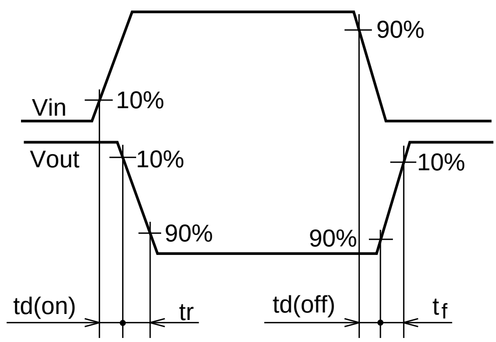
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

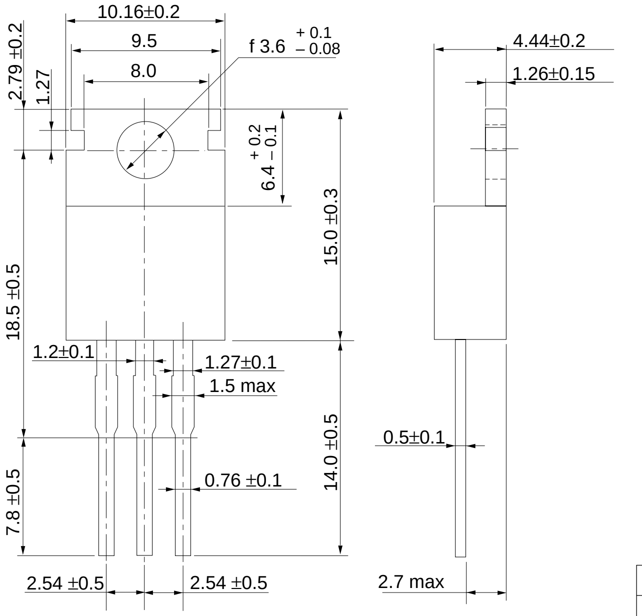


Waveform



Package Dimensions

Unit: mm



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EIAJ	SC–46
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