CMOS 4-BIT MICROCONTROLLER

TMP47C233AN, TMP47C433AN

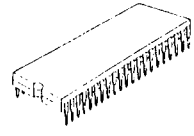
The 47C233A / 433A are the high speed and high performance 4-bit single chip microcomputers based on the TLCS-47 CMOS series with D / A converter (pulse width modulation) outputs and A/D converter input, and are suitable application in digital tuning systems for TV sets.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C233AN	2048 x 8-bit	128 x 4-bit	SDIP42	TMP47C933AE
TMP47C433AN	4096 x 8-bit	256 x 4-bit		

FEATURES

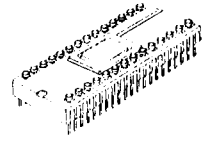
- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.9 us(at 4.2 MHz)
- ◆90 basic instructions
- ◆Table look - up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting: 15 levels max.
- ◆5 interrupt sources (External: 2, Internal: 3)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I / O port (36 pins)
  - Input 2 ports 5 pins
  - Output 2 ports 8 pins
  - I / O 6 ports 23 pins
- ◆Interval Timer
- ◆Two 12-bit Timer / Counters
  Timer, event counter, and pulse width measurement mode
- ◆D / A converter (Pulse width modulation) outputs
  - 14-bit resolution 1 channel
  - 6-bit resolution 3 channels
- ◆3-bit A / D converter input 1 channel
  Auto frequency control signal (S-shaped curve) detection
- ◆High current outputs
  LED direct drive capability (typ. 20 mA x 8 bits)
- ◆Hold function
  Battery / Capacitor back - up
- ◆Real Time Emulator: BM47217A

SDIP42



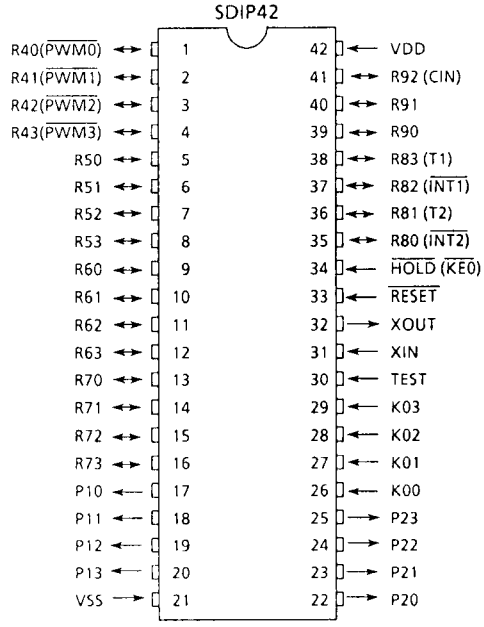
TMP47C233AN
TMP47C433AN

SDIC42

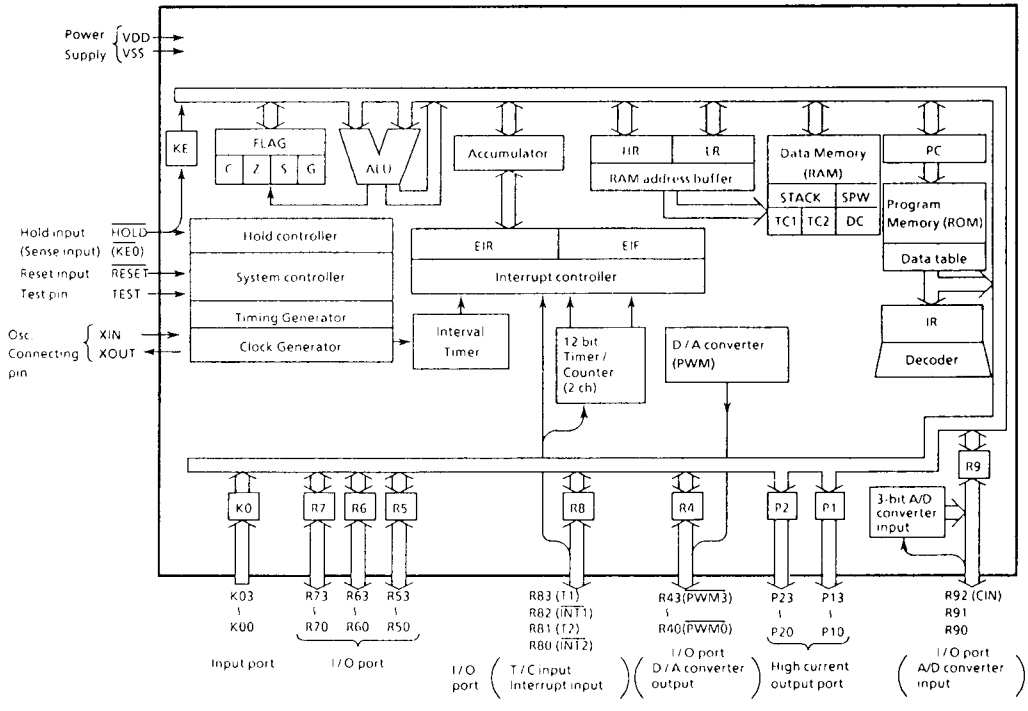


TMP47C933AE

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input / Output	FUNCTIONS	
K03 - K00	Input	4 - bit input port	
P13 - P10	Output	4 - bit output port with latch. 8 - bit data are output by the 5 - bit to 8 - bit data conversion instruction [OUTB @HL].	
P23 - P20			
R43 ($\overline{PWM3}$) -R41 ($\overline{PWM1}$)	I / O (Output)	4 - bit I / O port with latch. When used as input port or D/A converter outputs pins, the latch must be set to "1"	6 - bit D / A converter output
R40 ($\overline{PWM0}$)			14 - bit D / A converter output
R53 - R50	I / O	4 - bit I / O port with latch. When used as input port, the latch must be set to "1" Every bit data is possible to be set, clear and tested by the manipulation of the L - register indirect addressing.	
R63 - R60			
R73 - R70			
R83 (T1)	I / O (Input)	4 - bit I / O port with latch. When used as input port, external interrupt input pin, or Timer / Counter external input pin, the latch must be set to "1".	Timer / Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 (CIN)	I / O(Input)	3 - bit I / O port with latch. When used as input port or serial port, the latch must be set to "1".	3-bit A/D converter input
R91 - R90	I / O		
XIN	Input	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request / release signal input	Sense input
TEST	Input	Test pin for out - going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C233A / 433A, the configuration and functions of hardwares are described.
As the description is porvided with priority on those parts differing from the 47C200A/400A, the technical data sheets for the 47C200A / 400A shall also be referred to.
The 47C233A / 433A have no serial interface, differing from the 47C200A / 400A.

1 SYSTEM CONFIGURATION

(1) I / O Ports
(2) A / D Converter (Comparator) input
(3) D / A Converter (Pulse Width Modulation) output

2 PERIPHERAL HARDWARE FUNCTION

2.1 I / O Ports

The 47C233A / 433A have 10 I/O ports (36 pins) each as follows:

①	K0	; 4 - bit input
②	P1, P2	; 4 - bit output
③	R4	; 4 - bit input / output (shared by pulse with modulation output)
④	R6	; 4 - bit input / output *(Note)*
⑤	R5, R7	; 4 - bit input / output
⑥	R8	; 4 - bit input / output (shared by external interrupt input and timer / counter input)
⑦	R9	; 3 - bit input / output (shared by A / D converter input: R92 pin)
⑧	KE	; 1 - bit sense input (shared by hold request / release signal input)

Note . Port R6 becomes a tri-state output buffer when the I/O circuit code : PF is selected.

(1) Port R4 (R43-R40)
This is a 4-bit I/O port with latch. The latch should be set to "1" when the port is used as an input port. The latch is initial to "1" during reset.
It is R4 port common to $\overline{PWM}$ output. The latch should be set to "1" when $\overline{PWM}$ is used as an output port.

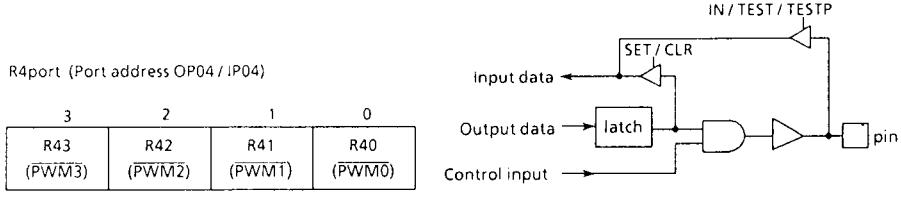


Figure 2-1. Port R4

(2) Port R6 (R63-R60)

The 4-bit I/O port with latch. The output buffers become a tri-state output buffer when the I/O circuit code: PF is selected, and the state of them is simultaneously controlled by the port. Controlling the Tri-state is performed by MSB of the port address OP09. When the data of the MSB of the OP09 are "0", the output buffers are high-impedance state. The MSB of the OP09 is initialized to "0" during reset, the output latch should be set to "1" when the port is used as output port. The output buffers should be set to high-impedance when the port is used as input port.

```
Example :   Outputs the immediate data "5" to the R6 port.
        SET       %OP09,  3          ; OP09₃←1 (Output buffer is on)
        OUT       #5,  %OP06         ; Port R6←5
```

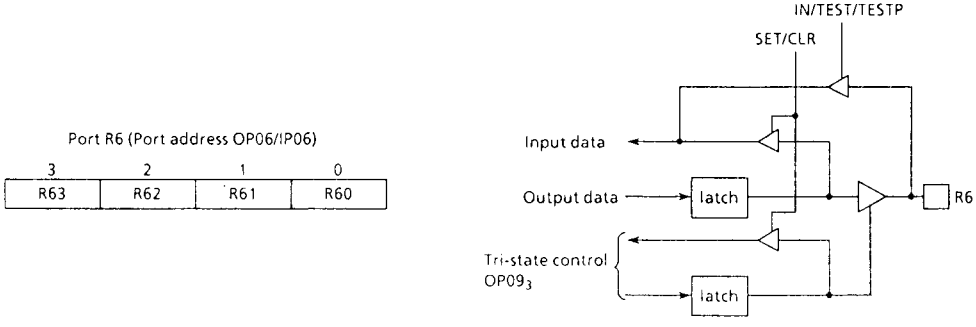


Figure 2-2. Port R6

(3) Port R9 (R92-R90)

This is a 3-bit I/O port with latch. The latch should be set to "1" when the port is used as an input port. The latch is initial to "1" during reset.

R92 (CIN) pin can also be used for A/D convertor (comparator) input for AFC (Auto Frequency Control) signal detection. R92 input is ordinary digital input which is read from bit 2 of IP09. CIN input is comparator input read from bit 3 of IP09 and uses the programmable 3-bit D/A convertor output as the reference voltage.

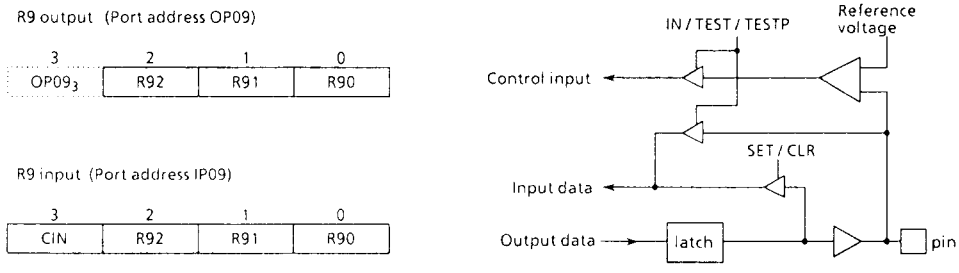


Figure 2-3. Port R9

Note. About OP09₃

When I/O circuit code : PF is selected, this bit functions for R6 port tri-state control. The output buffer is set to high impedance when the data is "0". When code : PC is selected, the R6 port is set for open drain output and the OUT/SET/CLR instruction for OP09₃ becomes ineffective.

Port address (**)	Port		Input / Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	○	○	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 2)	○	○	–
02	P2 output latch	P2 output port	○	○	○		○	○	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port (Note 3)	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	——	——	–	–	–	–	–	–	–
0E	Hold status	——	○	–	–	–	–	○	–
0F	——	——	–	–	–	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	A/D converter input control	–	○	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	PWM buffer selector	–	○	–	–	–	–	–
18	Undefined	PWM data transfer buffer	–	○	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer / Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer / Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	——	–	–	–	–	–	–	–

Notes. 1. *"——" means the reserved state. Unavailable for the user programs.*

2. *The 5 - bit to 8 - bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.*

3. *I/O circuit code : Controlling the tri-state (R6 port) is performed by MSB of the port address OP09, when I/O circuit code select PF.*

Table 2-1. Port Address Assignments and Available I / O Instructions

2.2 3-bit A/D Converter (Comparator) Input

Comparator input consists of a comparator and a 3-bit D/A converter. AFC input voltage can be detected in 8 steps by sensing bit 3 of IP09 while changing the reference voltage (D/A converter output voltage) with the command register (OP12).

R92 pin is also used for comparator input. Bit 2 is used to set R92 pin for ordinary digital input.

The comparator is disabled and bit 3 is set to "0" during reset. The latch should be set to "1" when R92 pin is used for comparator input and digital input.

2.2.1 Circuit Configuration

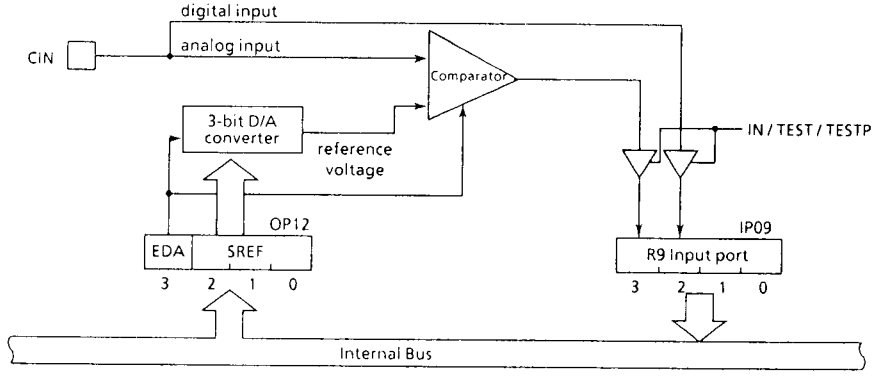


Figure 2-4. Comparator input Circuit

2.2.2 Control of Comparator Input

The reference voltage of the comparator is set using the lower 3 bits of the command register.

Table 2-2 shows the reference voltage at V_{DD} = 5V.

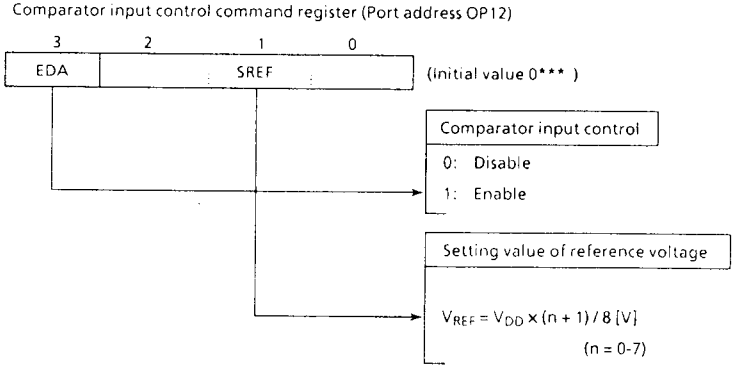


Figure 2-5. Control Command Register

OP12			reference voltage [V]
2	1	0	
0	0	0	0.62
0	0	1	1.25
0	1	0	1.87
0	1	1	2.50
1	0	0	3.12
1	0	1	3.75
1	1	0	4.37
1	1	1	5.00

Table 2-2. Reference Voltage

2.3 D / A converter (PWM) output

The 47C233A/433A have four channels built-in D/A converter ($\overline{PWM}$) outputs. $\overline{PWM}$ output can easily be obtained by connecting an external low pass filter.

$\overline{PWM}$ outputs data are multiplex to the R4 port. When the R4 ($\overline{PWM}$) port is used for $\overline{PWM}$ output, the corresponding bits of R4 output latch should be set to "1". The output buffer is set to high impedance during reset and so must be set to ON status by instruction (refer to section 2-1 I/O ports).

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). PWM data written to the data transfer buffer can be sent to the PWM data latch by writing "C_H" to the buffer selector, and $\overline{PWM}$ output switches switch to $\overline{PWM}$ output. PWM data transferred to the PWM data latch remain intact until overwritten. Resetting and holding clear the buffer selector, data transfer buffer and PWM data latch to "0" ($\overline{PWM}$ output is "high" level).

2.3.1 Configuration of PWM circuit

Configuration of PWM circuit shown in Figure 2-7.

2.3.2 Output waveform of PWM circuit

(1) $\overline{PWM0}$ output

$\overline{PWM0}$ is a PWM output controlled by 14 bits data. The basic period of the $\overline{PWM0}$ is $T_M = 2^{15} / fc$.

The higher 8 bits of 14 bits data are used to control the pulse width of the pulse output with the period of $T_S = T_M / 64$, which is the sub - period of the $\overline{PWM0}$. When the 8 bits data are decimal n ($0 \leq n \leq 255$), this pulse width becomes $n \times t_0$, where $t_0 = 2 / fc$.

The lower 6 bits of 14 bits data are used to control the generation of an additional t_0 wide pulse in each T_S period. When the 6 bits data are decimal m ($0 \leq m \leq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a T_M period. The relationship between the 6 bits data and the position of T_S period where the additional pulse is generated is shown in Table 2-3.

(2) $\overline{PWM1}$-$\overline{PWM3}$ output

Each of $\overline{PWM1}$ to $\overline{PWM3}$ is a PWM output controlled by 6 bits data. The period of them is $T_N = 2^7 / fc$. When the 6 bits data are decimal k ($0 < k < 63$), the pulse width becomes $k \times t_0$. The waveform is also illustrated in Figure 2-6.

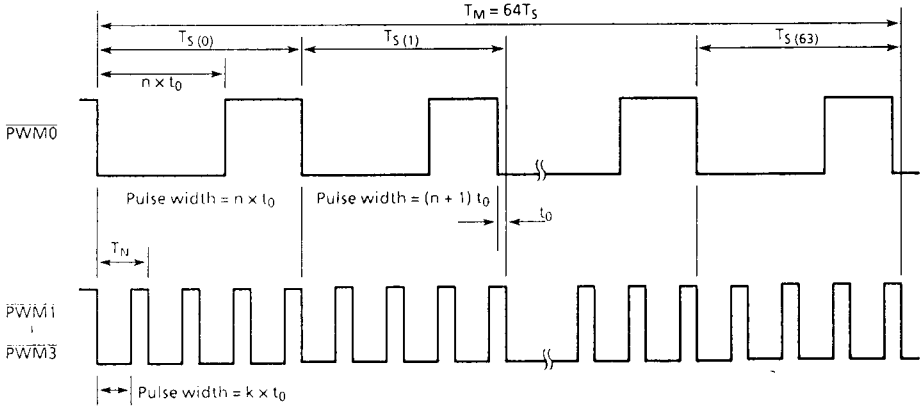


Figure2-6. $\overline{PWM}$ Output Waveform (It is shown to the additional pulse $T_{S(1)}$ and $T_{S(63)}$ of the $\overline{PWM0}$)

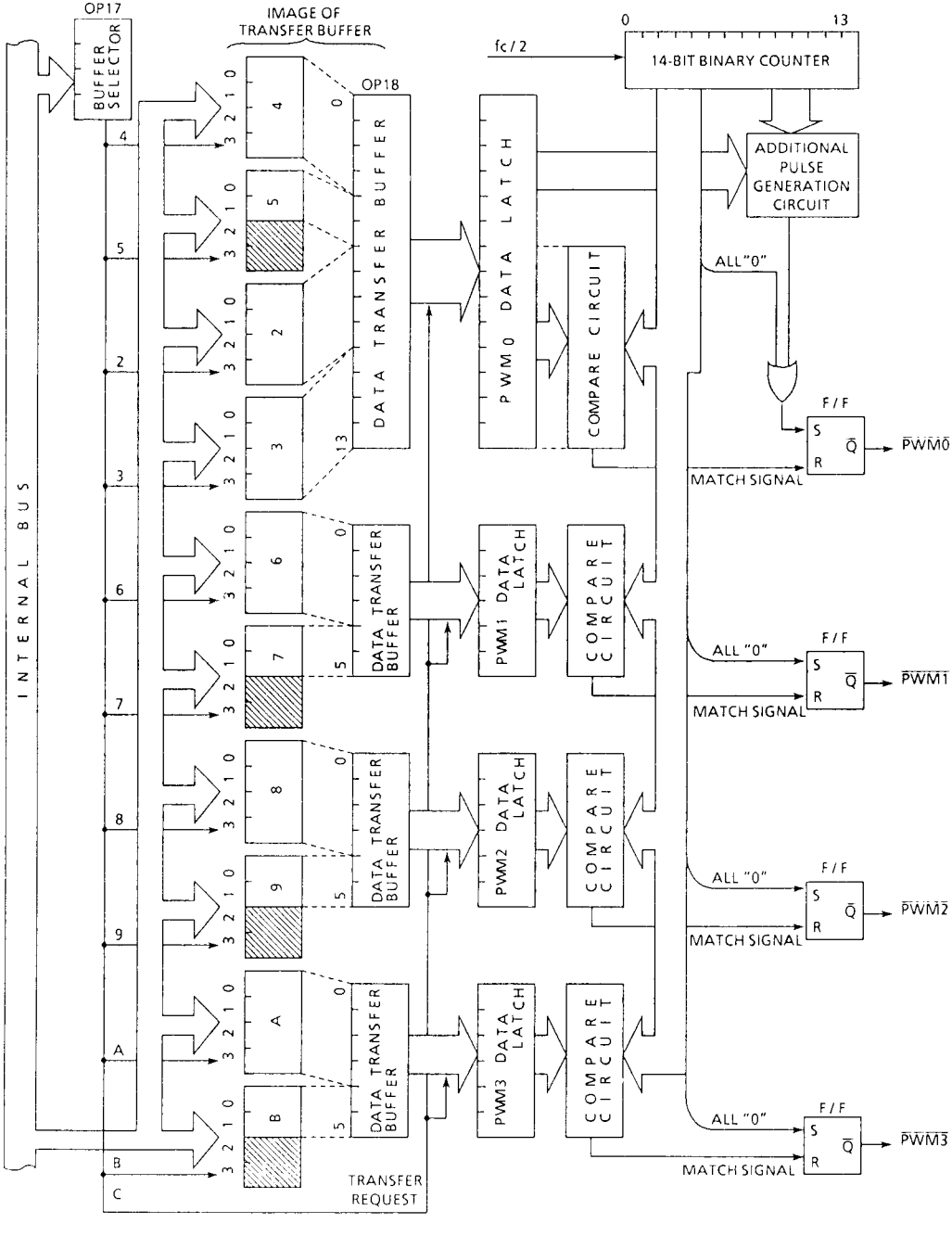


Figure 2-7. Pulse Width Modulation Circuit

Bit position of 6 bits data	Relative position of Ts where the output pulse is generated (No. i of $T_{S(i)}$ is listed)
Bit 0	32
Bit 1	16, 48
Bit 2	8, 24, 40, 56
Bit 3	4, 12, 20, 28, 36, 44, 52, 60
Bit 4	2, 6, 10, 14, 18, 22, 26, 30, ·····, 58, 62
Bit 5	1, 3, 5, 7, 9, 11, 13, 15, 17, ·····, 59, 61, 63

Note. When the corresponding bit is "1", it is output.

Table 2-3. Correspondence between 6 bits data and the additional pulse generated Ts periods

2.3.3 Control of PWM circuit (Data transfer)

$\overline{PWM}$ output is controlled by writting output data to a data transfer buffer (OP18). For writing, the output data are divided using the buffer selector (OP17). Buffer numbers are assigned to the data transfer buffers for these divided data, after which the data are written as shown in Table 2-4.

① The number of the transfer buffer to which the data are to be written is written to the buffer selector (OP17).

② The corresponding PWM data are written to the transfer buffer (OP18).

③ Operations ① and ② are repeated, continuously writing data to the transfer buffer.

④ When all of the output data have been written, "C_H" is written to the buffer selector.

While the output data are being written to the transfer buffer, the previously written data are being output. For $\overline{PWM0}$ output, switching to $\overline{PWM}$ output occurs at a maximum of 2^{15} / fc [sec] (at 4MHz, 8192μs) after "C_H" is written to the buffer selector. For $\overline{PWM1}$ through $\overline{PWM3}$ output data switching, this requires 2^9 / fc [sec] (at 4MHz, 128μs).

Buffer Number (OP17)	Correspondence to bit (OP18)		Mode	PWM Output
2	Bit of PWM0 transfer buffer	9 - 6	Write	Preceding data
3	Bit of PWM0 transfer buffer	13 - 10	Write	Preceding data
4	Bit of PWM0 transfer buffer	3 - 0	Write	Preceding data
5	Bit of PWM0 transfer buffer	5 - 4	Write	Preceding data
6	Bit of PWM1 transfer buffer	3 - 0	Write	Preceding data
7	Bit of PWM1 transfer buffer	5 - 4	Write	Preceding data
8	Bit of PWM2 transfer buffer	3 - 0	Write	Preceding data
9	Bit of PWM2 transfer buffer	5 - 4	Write	Preceding data
A	Bit of PWM3 transfer buffer	3 - 0	Write	Preceding data
B	Bit of PWM3 transfer buffer	5 - 4	Write	Preceding data
C	None		Transfer	Present data

Table 2-4. The bit and buffer number of data transfer buffer

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include R92 pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin except R92 pin	− 0.5 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Ports R5, R7, R8, R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (Time)	T_{sld}		260 (10 sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the HOLD mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST RESET, HOLD	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	−	−	− 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up / pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Tri-state port Port R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output High Voltage	V_{OH1}	Ports P, R (push-pull)	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	−	−	V
	V_{OH2}	Port R (Tri-state)	V_{DD} = 4.5V, I_{OH} = − 0.7mA	4.1	−	−	
Output Low Voltage	V_{OL1}	Ports R5, R7 to R9	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
	V_{OL2}	Ports R4, R6	V_{DD} = 4.5V, I_{OL} = 0.7mA				
Output Low Current	I_{OL}	Port P	V_{DD} = 4.5V, V_{OL} = 1.0V	−	20	−	mA
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up / pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3V / 0.2V
The K0 port is open when the pull-up / pull-down resistor is contained. The Voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A / D CONVERTER CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V_{AIN}	CIN		V_{SS}	−	V_{DD}	V
A / D Conversion Error	−			−	−	± 1/4	LSB

A.C. CHARACTERISTICS

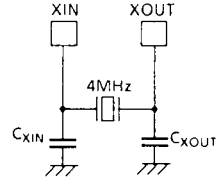
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	–	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					

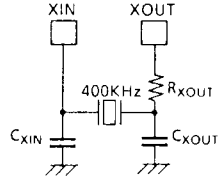
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

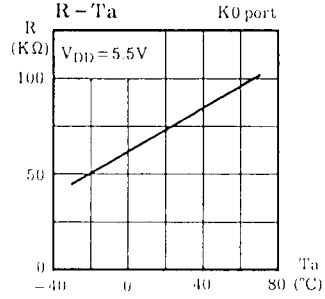
(1) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

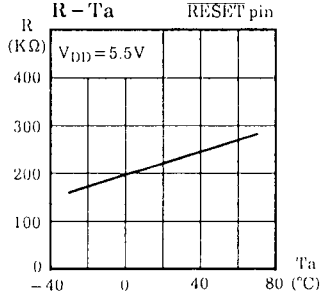


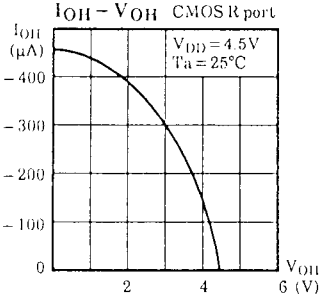
(2) 400KHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

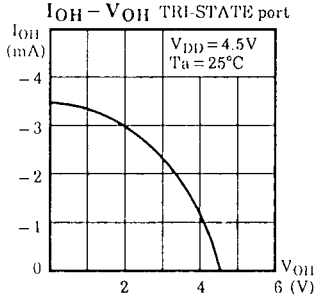


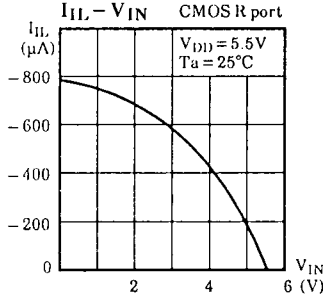
TYPICAL CHARACTERISTICS

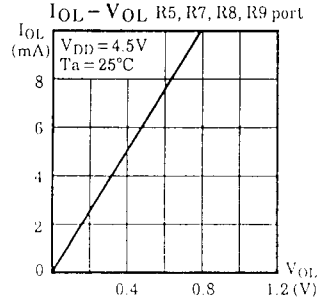


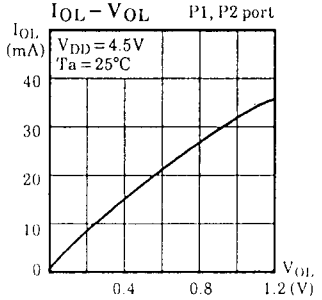


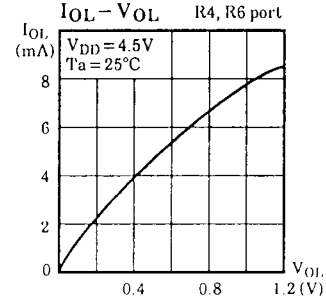


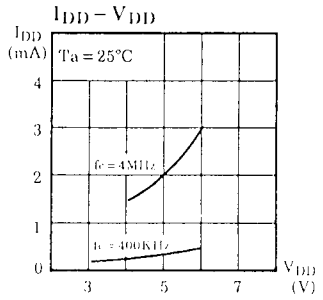


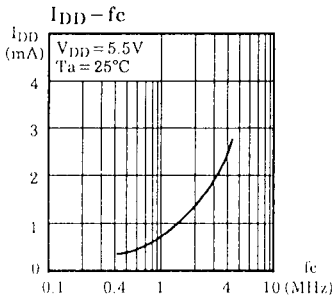












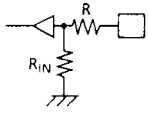
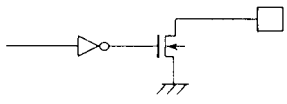
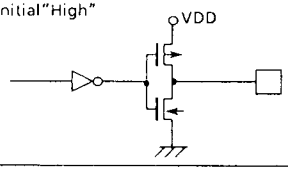
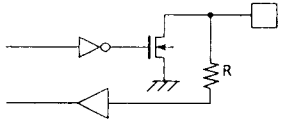
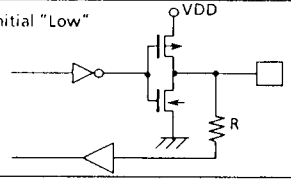
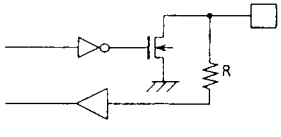
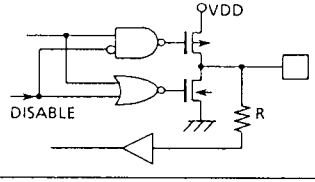
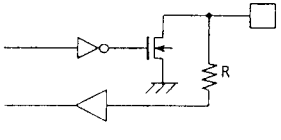
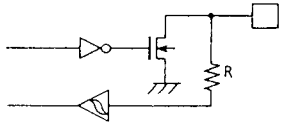
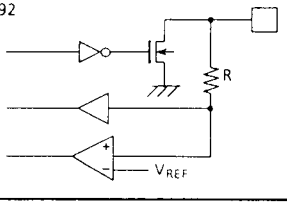
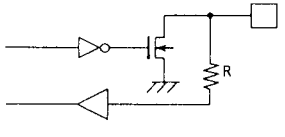
Input / Output Circuitry

(1) Control pins

I / O circuitries of the 47C233A / 433A control pins are similar to that of the 47C200A / 400A.

(2) I / O ports

The I / O circuitries of the 47C233A / 433A I/O ports are shown below, any one of the circuitries can be chosen by a code (PC, PF) as a mask option.

PORT	I / O	Input/Output CIRCUITRY and CODE	REMARKS
K0	Input		pull - down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P1 P2	Output	PC: Initial "Hi-Z"  PF: Initial "High" 	Sink open drain or Push-pull output High current I_{OL} = 20mA (typ.)
R5	I/O	PC: Initial "Hi-Z"  PF: Initial "Low" 	Sink open drain or Push-pull output R = 1KΩ (typ.)
R6	I/O	PC  PF 	Sink open drain or Tri-state Initial "Hi-Z" R = 1KΩ (typ.)
R4 R7 R8	I/O	R4, R7  R8 	Sink open drain Initial "Hi-Z" Hysteresis input (Port R8) R = 1KΩ (typ.)
R9	I/O	R92  R91, R90 	Sink open drain Initial "Hi-Z" Comparator input (R92 pin) R = 1KΩ (typ.)

This Page Intentionally Left Blank

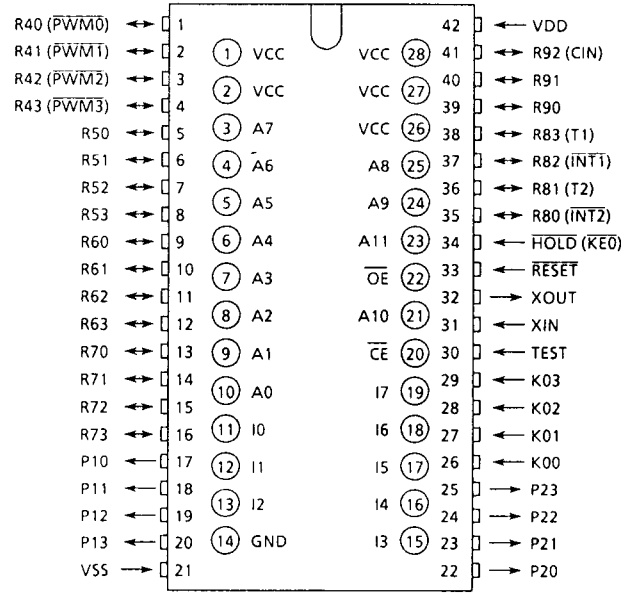
CMOS 4-BIT MICROCONTROLLER

TMP47C933AE

The 47C933A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C233A/433A application systems (programs).
The 47C933A is pin compatible with the 47C233A/433A which are mask-programed ROM devices.

PIN ASSIGNMENT (TOP VIEW)

SDIC42



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5 to 6.0V C_L = 100pF Topr = – 30 to 70°C	–	–	150	ns
Data Setup Time	t_{IS}		150	–	–	ns
Data Hold Time	t_{IH}		50	–	–	ns

NOTES FOR USE

(1) Program memory

The program area are as shown in Figure 1. When this chip is used as evaluator of the 47C233A, data conversion table for [OUTB @HL] instruction must be allocated at two areas and they must be the same contents as shown in Figure 1.

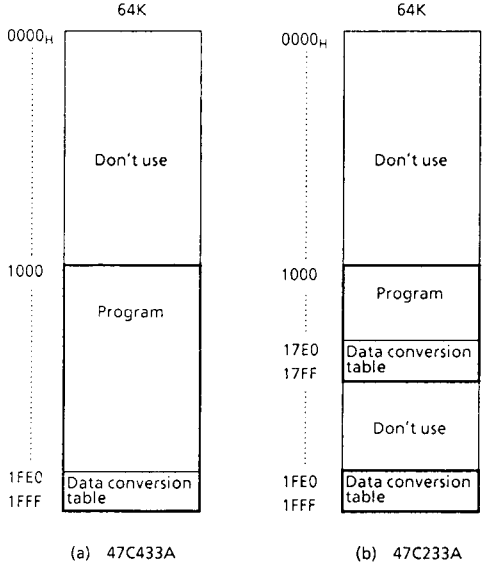


Figure 1. Program area

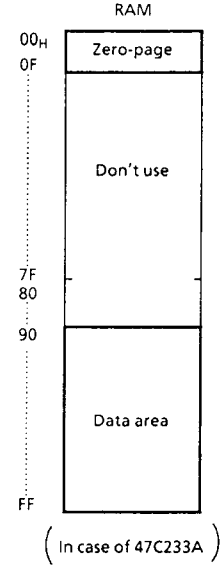


Figure 2. RAM addressing

(2) Data memory

The 47C933A contains 256 x 4-bit (equivalent to 47C433A) data memory. When the 47C933A is used as evaluator of the 47C233A, programming should be performed assuming that the RAM is assigned to addresses $00\sim0F_H$ and $90\sim FF_H$ as show in Figure 2 by considering the application software evaluation.

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C933A are similar to the code PC of the 47C233A/433A. When this chip is used as evaluator with other I/O code, it is nacessary to provide the external resistors.

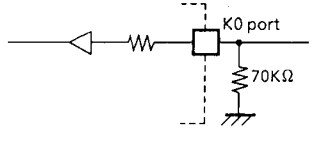


Figure 3. External circuitry

Note. Caution is required when using the 47C933A as a code PF evaluator. The follwing ports of the 47C933A differ from those of the 47C233A/433A (code PF).

① *Ports P1 and P2 are not push-pull output (initial "High").*

② *Port R5 is not push-pull output (initial "Low").*

③ *Port R6 is not tristate output (initial "Hi-Z").*