

AN8091, AN8091S

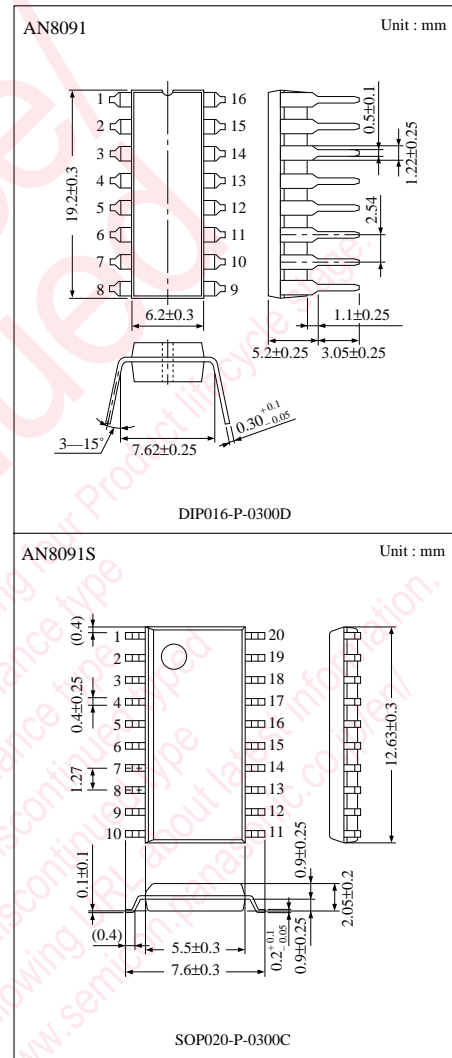
Overvoltage Protective Circuit Incorporated Switching Power Supply

■ Overview

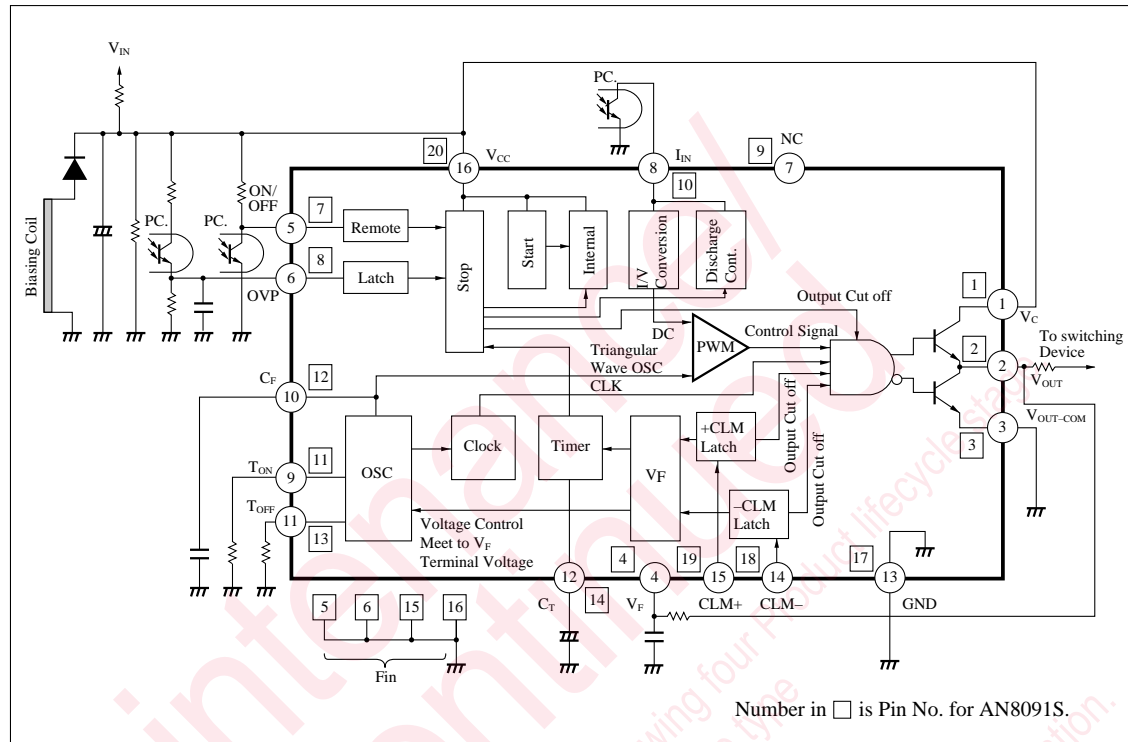
The AN8091 and AN8091S are equipped with various protection functions such as from overcurrent and overvoltage, which can raise the reliability of the power supply, realizing the high-speed control up to 500kHz.

■ Features

- The PWM control frequency of up to 500kHz and miniaturization realized.
- The power MOS FET of large capacitance directly controllable
- Built-in overcurrent protective function for two systems of positive side detection and negative one, and intermittent operation function for protection when overcurrent condition proceeds further
- ON/OFF function allowing the power supply to be started or stopped by the external signal, and current control function required for the secondary side control incorporated
- Package : 16-lead DIP for the AN8091, 20-lead SOP for the AN8091S
- Overvoltage protection circuit built-in



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	
Supply voltage	V_{CC}	31	V	
Collector terminal allowable applied voltage	V_C	31	V	
Maximum continuous output current	I_{Omax}	±150	mA	
T_{ON} terminal allowable applied voltage	I_{TON}	-1	mA	
T_{OFF} terminal allowable applied voltage	I_{TOFF}	-1	mA	
Power dissipation $T_a \leq 25^\circ\text{C}$	P_D	AN8091	1736	mW
		AN8091S	1500	
Allowable joint temperature	T_j	150	°C	
Operating ambient temperature	T_{opr}	-30 to +85	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

Note) For surface mounting on the glass epoxy board (50 × 50 × 0.45mm)

■ Recommended Operating Range (Ta=25°C)

Parameter	Symbol	Range
Operating supply voltage	V_{CC}	Stop voltage to 30V

■ Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Operation start voltage	$V_{CC (start)}$		15.2	16	17.2	V
Operation stop voltage	$V_{CC (stop)}$		9	10	10.9	V
Voltage difference between operation start and stop	DV_{CC}	$DV_{CC}=V_{CC (start)}-V_{CC (stop)}$	5	6	7	V
Pre-start circuit current (1)	I_{CCL1}	$V_{CC}=14.5V$	50	100	120	μA
Circuit current (1)	I_{CC01}	$V_{CC}=11V$ (Start Condition)	10	15	21	mA
Circuit current (2)	I_{CC02}	$V_{CC}=30V$	10	15	21	mA
OFF-time circuit current (1)	$I_{CC1 OFF}$	$V_{CC}=14V$	50	100	120	μA
OFF-time circuit current (2)	$I_{CC2 OFF}$	$V_{CC}=25V$	0.95	1.5	1.9	mA
Timer off operation circuit current (1)	$I_{CC1 CT}$	$V_{CC}=14V$	—	190	270	μA
Timer off operation circuit current (2)	$I_{CC2 CT}$	$V_{CC}=25V$	0.95	1.55	2	mA
OVP operation circuit current (1)	$I_{CC1 OVP}$	$V_{CC}=9.5V$	215	280	380	μA
OVP operation circuit current (2)	$I_{CC2 OVP}$	$V_{CC}=25V$	1.3	2	3	mA
ON/OFF terminal H threshold voltage	$V_{THH ON/OFF}$		2.1	2.6	3.1	V
ON/OFF terminal L threshold voltage	$V_{THL ON/OFF}$		1.9	2.4	2.9	V
ON/OFF terminal hysteresis voltage	$DV_{TH ON/OFF}$		0.1	0.2	0.3	V
Output 0% duty FB current	$I_{FB MIND}$	$V_{CC}=18V$	-2	-1.5	-1.1	mA
Output maximum duty FB current	$I_{FB MAXD}$	$V_{CC}=18V$	-0.9	-0.55	-0.4	mA
FB current difference between output 0% and maximum duty	DI_{FB}	$DI_{FB}=I_{FB MIND}-I_{FB MAXD}$	-1.35	-0.95	-0.7	V
FB terminal voltage	V_{FB}	$I_{FB}=-0.95mA$	4.6	5.6	6.8	V
FB terminal discharging current	$I_{FB Res}$		1	3	—	mA
OVP terminal threshold voltage	$V_{TH OVP}$		1.2	1.4	1.6	V
OVP terminal input current	$I_{IN OVP}$	$V_{OVP}=5V$	-0.5	0	0.5	μA
OVP release supply voltage	$V_{CC OVP}$		6	7	8	V
Power supply stop voltage OVP release supply voltage	$DV_{CC OVP}$	$DV_{CC OVP}=V_{CC STOP}-V_{CC OVP}$	0.65	1.3	—	V
Timer frequency	f_{TIM}		0.27	0.44	0.6	Hz
Timer charging current (1)	$I_{CH1 TM}$		-180	-125	-80	μA
Timer OFF/ON time ratio	G_{TIM}		7	8.3	11	—
CLM ⁻ terminal threshold voltage (1)	$V_{TH1 CLM-}$		-215	-200	-185	mV
CLM ⁻ terminal out-current	$I_{OUT CLM-}$		-170	-125	-90	μA
CLM ⁺ terminal threshold voltage (1)	$V_{TH1 CLM+}$		185	200	215	mV
CLM ⁺ terminal out-current	$I_{OUT CLM+}$		-270	-200	-140	μA
Oscillation frequency (1)	f_{OSC1}	$R_1=17k\Omega, R_2=20k\Omega, C_F=220pF$	185	200	215	kHz
Duty ratio (1)	G_{DUTY1}	$R_1=17k\Omega, R_2=20k\Omega, C_F=220pF$	47	49	51	%
Oscillation waveform upper limit voltage	V_{OSCH}		4	4.4	4.8	V
Oscillation waveform lower limit voltage	V_{OSCL}		1.8	2	2.2	V
Oscillation waveform voltage difference between upper and lower limit	DV_{OSC}		2.2	2.4	2.6	V
CLM operation oscillation frequency (1)	$f_{OSC1 VF}$	$R_1=17k\Omega, R_2=20k\Omega, C_F=220pF, V_F=5V$	185	200	215	kHz
CLM operation oscillation frequency (2)	$f_{OSC2 VF}$	$R_1=17k\Omega, R_2=20k\Omega, C_F=220pF, V_F=2V$	110	124	141	kHz
CLM operation oscillation frequency (3)	$f_{OSC3 VF}$	$R_1=17k\Omega, R_2=20k\Omega, C_F=220pF, V_F=0.2V$	20	25	32	kHz
Timer operation start V_F voltage	$V_{TH TIM}$		2.7	3	3.3	V

■ Electrical Characteristics (cont.) (Ta=25°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Pre-circuit current (2) ^{Note 1)}	I _{CCL2}	V _{CC} =14.5V, -30°C ≤ Ta ≤ 85°C	40	100	160	μA
Timer charging current (2) ^{Note 1)}	I _{CH2 TIM}	V _{CT} =3.3V, Ta= -5°C	95	130	185	μA
Timer charging current (3) ^{Note 1)}	I _{CH3 TIM}	V _{CT} =3.3V, Ta=85°C	75	100	145	μA
CLM ⁻ terminal threshold voltage (2) ^{Note 1)}	V _{TH2 CLM-}	-30°C ≤ Ta ≤ 85°C	-215	-200	-185	mV
CLM ⁻ terminal delay time ^{Note 1)}	T _{PD CLM-}		—	190	—	ns
CLM ⁺ terminal threshold voltage (2) ^{Note 1)}	V _{TH2 CLM+}	-30°C ≤ Ta ≤ 85°C	185	200	215	mV
CLM ⁺ terminal delay time ^{Note 1)}	T _{PD CLM+}		—	190	—	ns
Oscillation frequency (2) ^{Note 1)}	f _{OSC2}	R ₁ =17kΩ, R ₂ =20kΩ, C _F =220pF, -30°C ≤ Ta ≤ 85°C	185	200	215	kHz
Oscillation frequency (3) ^{Note 1)}	f _{OSC3}	R ₁ =17kΩ, R ₂ =20kΩ, C _F =68pF, -30°C ≤ Ta ≤ 85°C	462	500	538	kHz
Duty ratio (2) ^{Note 1)}	G _{DUTY2}	R ₁ =17kΩ, R ₂ =20kΩ, C _F =220pF, -30°C ≤ Ta ≤ 85°C	46	49	52	%
Duty ratio (3) ^{Note 1)}	G _{DUTY3}	R ₁ =17kΩ, R ₂ =20kΩ, C _F =68pF, -30°C ≤ Ta ≤ 85°C	44	49	54	%
FB terminal voltage ^{Note 1)}	R _{FB}		—	500	—	Ω
T _{ON} terminal voltage ^{Note 1)}	V _{TON}	R ₁ =17kΩ	—	4.4	—	V
T _{OFF} terminal voltage ^{Note 1)}	V _{TOFF}	R ₂ =20kΩ	—	3.6	—	V
Output voltage rise time ^{Note 1)}	G _{rise}	Under no load	—	50	—	ns
Output voltage fall time ^{Note 1)}	G _{fall}	Under no load	—	40	—	ns

Note 1) These are design reference values, not guaranteed values.

■ Precautions on Use (Ta=25°C)

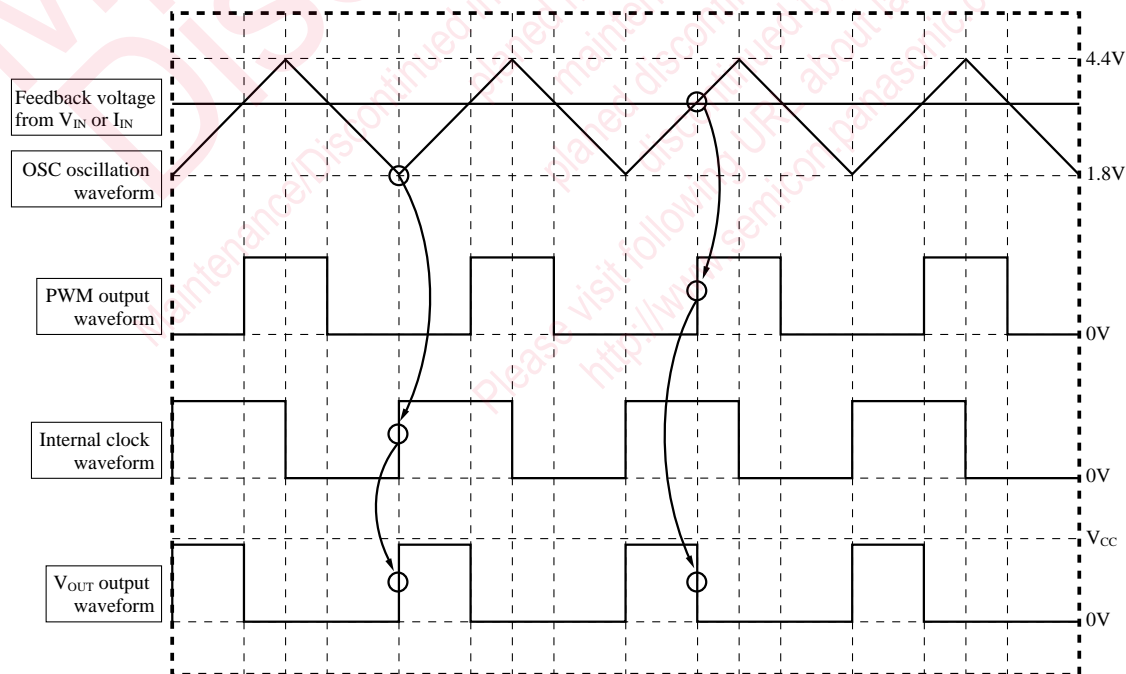
Parameter	Symbol	Rating	Unit
Peak output current	I _{Opeak}	±2	A
V _F terminal allowable applied voltage	V _F	V _{CC}	V
ON/OFF terminal allowable applied voltage	V _{ON/OFF}	V _{CC}	V
CLM ⁻ terminal allowable applied voltage	V _{CLM-}	±4	V
CLM ⁺ terminal allowable applied voltage	V _{CLM+}	-0.3, 4	V
OVP terminal allowable applied voltage	V _{OVP}	V _{CC}	V
FB terminal allowable applied voltage	V _{FB}	0, 10	V

■ Pin Descriptions

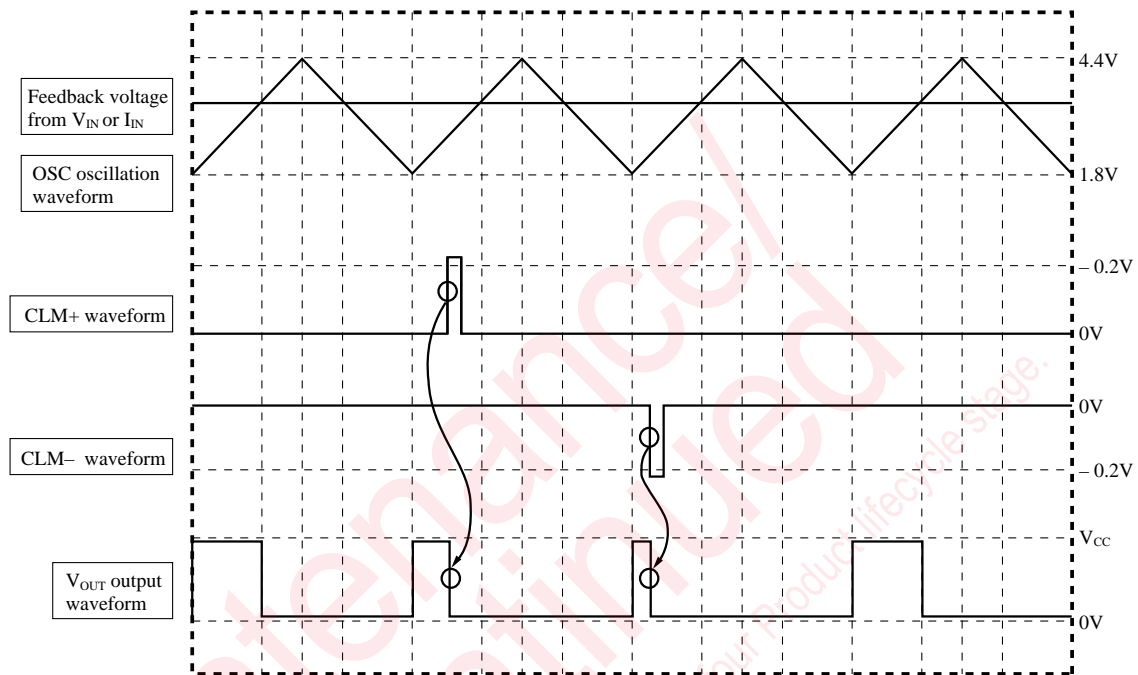
Pin No.		Symbol	Terminal description
DIL	SO		
1	1	V_C	Terminal applying the supply voltage to the output transistor.
2	2	V_{OUT}	Output terminal for IC. It drives the bipolar transistor.
3	3	$V_{OUT.COM}$	Ground terminal for the output transistor.
4	4	V_F	It detects the average level of output pulse and performs the timer control and duty control for the output.
5	7	ON/OFF	IC turning ON/OFF terminal. "H" to stop the IC (output "L"), "L" to operate the IC.
6	8	OVP	It detects the overvoltage to stop the IC. The stop condition is kept.
7	9	NC	
8	10	F/B	Terminal for current-feedback of power supply output.
9	11	T_{ON}	Terminal for connecting the resistor which determines the inclination of internally oscillated triangular wave during the charging period.
10	12	C_F	Terminal for connecting the capacitor which determines the frequency of internally oscillated triangular wave.
11	13	T_{OFF}	Terminal for connecting the resistor which determines the inclination of internally oscillated triangular wave during the discharging period.
12	14	C_T	Terminal for connecting the capacitor which determines the frequency of timer control.
13	17	GND	Ground terminal for the signal system.
14	18	CLM ⁻	Overcurrent detection terminal for the negative potential side.
15	19	CLM ⁺	Overcurrent detection terminal for the positive potential side.
16	20	V_{CC}	Terminal applying the supply voltage. It detects the start voltage and stop one.
—	5	FIN (GND)	Terminal which is directly connected with the IC chip. It has double function as radiator and ground terminal.
—	6	FIN (GND)	Terminal which is directly connected with the IC chip. It has double function as radiator and ground terminal.
—	15	FIN (GND)	Terminal which is directly connected with the IC chip. It has double function as radiator and ground terminal.
—	16	FIN (GND)	Terminal which is directly connected with the IC chip. It has double function as radiator and ground terminal.

■ Timing Chart

Under normal operation

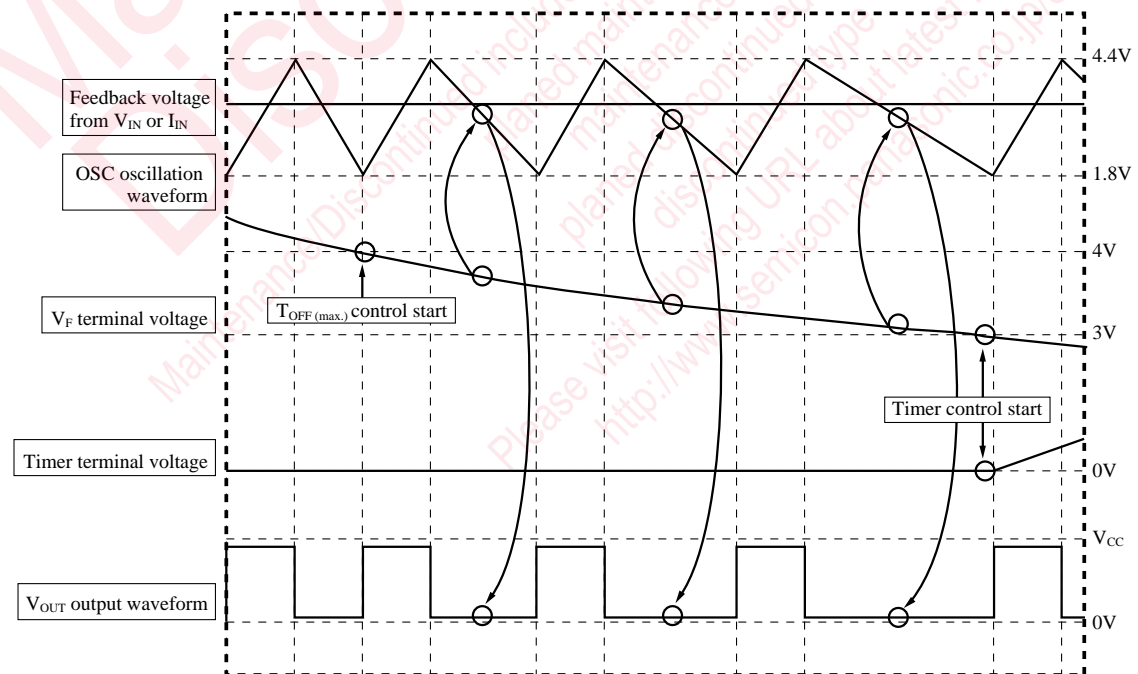


Under current-limited operation Note 1)



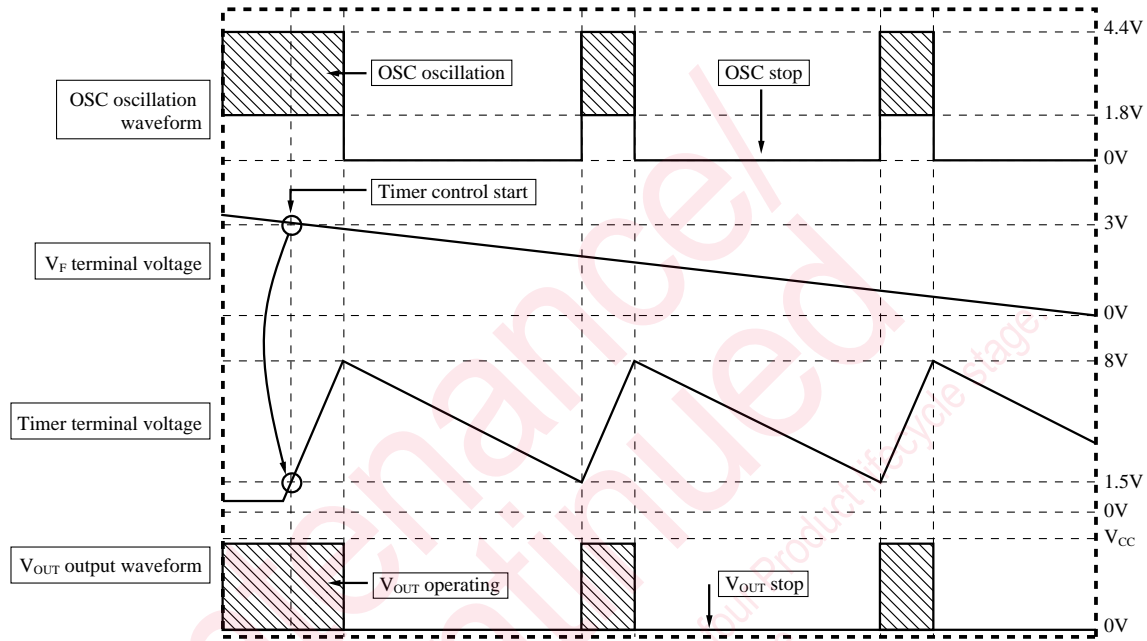
Note 1) V_F terminal voltage $\geq T_{OFF(max)}$ control voltage ($\leq 4V$)

Under $T_{OFF(max)}$ control operation Note 2)



Note 2) The $T_{OFF(max)}$ control and timer control work under current-limited operation ($CLM+ \geq 0.2V$, $CLM- \leq -0.2V$)

Under timer-controlled operation Note 3)



Note 3) Even under the timer-controlled operation, the OFF time of OSC (V_{OUT}) is controlled by the $T_{OFF(max)}$ control.

■ Technical Description on PWM Control IC for Switching Power Supply Using the Primary Side Control Method

1. Overview

The AN8091/S is a control IC suitable for the switching power supply using the primary side control method.

The control frequency can be set up to 500kHz, and the power supply can be miniaturized. Since the output current drive capability is large (its absolute maximum rating is ± 2 A peak), even the power MOS FET with large capacitance can be directly driven. Moreover, the pre-operation current is very small, 100 μ A. For the overcurrent protection function which limits the pulse current at overcurrent, two circuits are built in : One of them is dedicated to the positive voltage detection and the other is dedicated to the negative one. Thus, the AN8091/S is provided with various functions which are not built in the conventional ICs. In addition, the above built-in functions are mainly for the protection.

2. Features

- 1) The totem pole method is used in the output block. The output current drive capability is large : Its absolute maximum rating is ± 2 A (peak).
- 2) It can operate at the frequency of up to 500kHz. The output rise time is 50ns and the output fall time is 40ns : The high-speed operation is ensured.
- 3) The pre-operation current is small (100 μ A).
- 4) For the overcurrent protection function which limits the pulse current, two circuits are incorporated : One of them is dedicated to the positive voltage detection and the other is dedicated to the negative one. Detection voltage is ± 0.2 V.
- 5) It has the frequency variable function, which ensures the overcurrent protection.
- 6) It has the function which suppresses the secondary side output short-circuit current, allowing it to be decreased 1/8 time the overcurrent set value.
- 7) It has the output ON/OFF function and the overvoltage protection function.

3. Specifications

- 1) Supply voltage : 31V (max.)
- 2) Operation start voltage : 16V (typ.)
Operation stop voltage : 10V (typ.)
- 3) Pre-start operation current : 100 μ A (typ.)
Operation start circuit current : 15mA (typ.)
- 4) Oscillation frequency : 500kHz (max.)
- 5) Absolute maximum rated output current : ± 2 A (Peak)
 ± 150 mA (continuous)
- 6) Overcurrent protection detection voltage : ± 0.2 V (typ.)
(Two circuits respectively for positive voltage detection and negative one)
- 7) Output ON/OFF control voltage
 ≥ 2.6 V (output off)
 ≥ 2.4 V (output on) 1.4V (typ.)
- 8) Overvoltage protection detection voltage :

4. Application Equipment

Switching power supply of feed forward type

Switching power supply of flyback type

5. Overview of Each Block and Its Operation Description

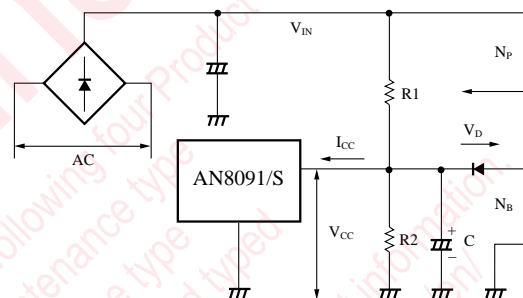
5.1. Operation Start/Stop Circuit Block

The AN8091/S starts operation with the current from the capacitor and bias which are resistance-divided from the power supply line. After operation start, it receives the bias supply from the auxiliary winding.

The pre-start current is used to determine the condition before operation start. Since the output terminal is kept to "L" level, malfunction due to leak current from the power MOS FET is prevented. Since its value is decreased to 100 μ A, loss of start resistance can be suppressed. The range of dispersion is narrow, thus the accuracy of operation start input voltage can be raised.

The hysteresis width of the operation start voltage and stop voltage is set wide (6V). The input capacitance can be downsized and the malfunction due to ripple can be prevented.

(Setting the constant)



Required parameters

- IC operation start voltage : $V_{CC(\text{start})}$
- IC stop voltage : $V_{CC(\text{stop})}$
- IC pre-start voltage : I_{CCL}

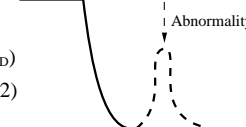
[Fig.1-1]

Operation start voltage $V_{IN(\text{start})}$:

$$V_{IN(\text{start})} \cong V_{CC(\text{start})} \left(1 + \frac{R1}{R2} \right) + R1 I_{CCL} \quad (1-1)$$

Operation stop voltage $V_{IN(\text{stop})}$:

$$V_{IN(\text{stop})} \cong \frac{N_p}{N_B} (V_{CC(\text{stop})} - V_D) \quad (1-2)$$



[Fig.1-2] Output Voltage (Operation Stop)

However, unless $V_{IN(\text{start})} > V_{IN(\text{stop})}$, the abnormality of the output voltage as shown in Fig.1-2 can occur at operation start/stop.

[Operation start/stop voltage]

When the operation start voltage ($16 \pm 1.5V$) and stop voltage ($10 \pm 1V$) of the AN8091/S are set, the following should be considered :

When the primary side input voltage V_{IN} is set to the range from 85 to 135V, the IC stop voltage $V_{IN(stop)}$ is set 75V, taking the margin into consideration. Therefore, the (1-3) is obtained from (1-2) :

$$\frac{N_P}{N_B} \cong \frac{V_{IN(stop)}}{V_{CC(stop)} - V_D} = 6.8V \quad (1-3)$$

If the above setting is made and $V_{IN}^{MAX} = 135V$, the voltage applied to the IC V_{CC}^{MAX} and the voltage of "H" level of the output pulse applied to the MOS FET gate are :

$$V_{CC}^{MAX} \cong V_{IN}^{MAX} \cdot \frac{N_S}{N_B} = 19.8V \quad (1-4)$$

$$V_{OUT(H)}^{MAX} \cong V_{CC}^{MAX} - 2V_{BE} - V_{CE(sat)} = 18.2V \quad (1-5)$$

If the above setting is made and the withstand voltage between the MOS FET gate and source is $\pm 20V$, the margin is insufficient.

The above consideration uses the premise that the stop voltage is set to 10V. If this stop voltage can be decreased, the problem on insufficient withstand voltage of the MOS FET V_{GSS} will be removed. However, "H" level voltage of the output pulse $V_{OUT(H)}^{MIN}$ when $V_{CC} = V_{CC(stop)}$ is :

$$V_{OUT(H)}^{MIN} \cong V_{CC(stop)} - 2V_{BE} - V_{CE(sat)} = 8.4V$$

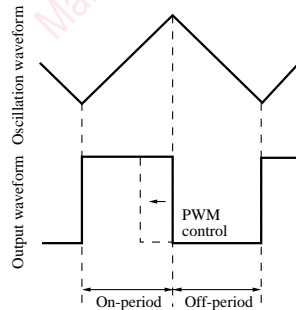
Therefore, when the margin is allowed for, the above stop voltage can not be decreased under the present situation.

Form the above review, we should conclude that the withstand voltage between the MOS FET gate and source of $\pm 20V$ is insufficient. We recommend that the product with withstand voltage of $\pm 25V$ be used.

5.2 Oscillation Circuit Block

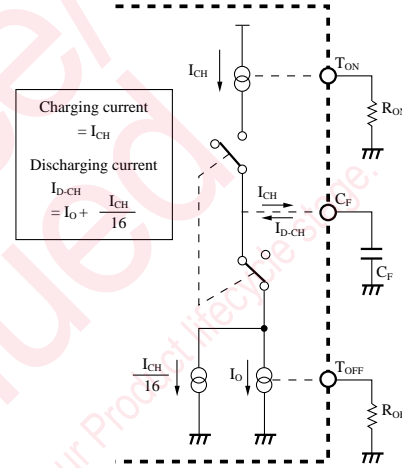
The oscillation waveform of the AN8091/S is triangular, and the value of charging/discharging constant current depends on the external resistance.

Fig.2-1 shows the oscillation waveform and output oscillation. For the oscillation waveform, the constant current charging time is a period when the output can be set "H" and the constant current discharging time is a period when it can be set "L."



[Fig.2-1]

Fig.2-2 shows the schematic diagram of the oscillation circuit. The charging current depends on the external resistance R_{ON} . On the other hand, the discharging current consists of the current of constant current source which depends on the external resistance R_{OFF} and the current 1/6 time the charging current. It is provided so that the maximum value of OFF period could be set to the value 1/8 time the ON period when the OFF period of the oscillation waveform is continuously extended under the cycle control described in the below.



[Fig.2-2]

5-2-1. Under Constant Operation

The ON-period and OFF-period of the oscillation waveform during the constant operation are given :

$$T_{ON} = \frac{R_{ON} \cdot C_F \cdot \Delta V_{OSC}}{V_{TON}} \quad (2-1)$$

$$T_{OFF} = \frac{C_F \cdot \Delta V_{OSC}}{\frac{V_{TOFF}}{R_{OFF}} + \frac{V_{TON}}{16R_{ON}}} \quad (2-2)$$

Therefore,

$$T = \left\{ \left(\frac{V_{TOFF}}{R_{OFF}} + \frac{V_{TON}}{16R_{ON}} \right) + \frac{R_{ON}}{V_{TON}} \right\} C_F \cdot \Delta V_{OSC} \quad (2-3)$$

$$\delta^{MAX} = 1 - \frac{16}{17 + 16\alpha} \left(\alpha = \frac{V_{TOFF} \cdot R_{ON}}{V_{TON} \cdot R_{OFF}} \right) \quad (2-4)$$

Where,

T_{ON} : Charging period of oscillation waveform

T_{OFF} : Discharging period of oscillation waveform

ΔV_{OSC} : Voltage difference between upper and lower limit of oscillation waveform

$$\Delta V_{OSC} = V_{OSCH} - V_{OSCL}$$

V_{TON} : Terminal voltage of T_{ON}

$$V_{TON} \approx 4.4V$$

V_{TOFF} : Terminal voltage of T_{OFF}

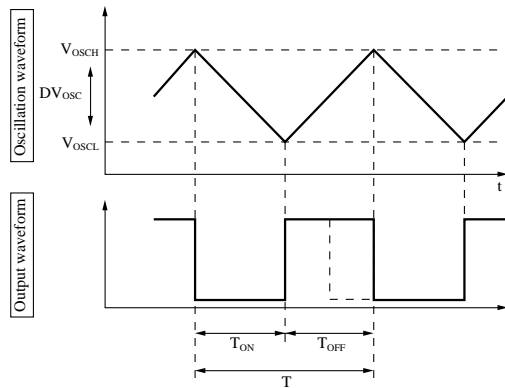
$$V_{TOFF} \approx 3.6V \text{ (Under constant condition)}$$

T : Oscillation frequency

$$f_{OSC} = 1/T$$

δ^{MAX} : Maximum time ratio determined by oscillation waveform

$$\delta^{MAX} = T_{ON}/T$$



[Fig.2-3] Oscillation Waveform and Output Waveform

5-2-2. Under Overcurrent Cycle Control and Intermittent Operation

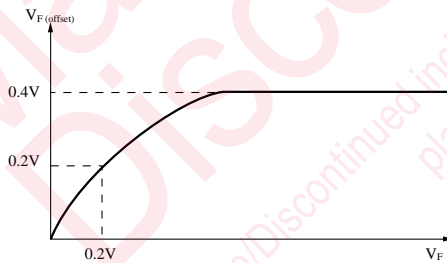
For the overcurrent cycle control function and the intermittent operation functions, refer to the description provided in another section below.

This section describes the oscillation waveform when these functions are activated.

When they are activated, the OFF period of oscillation waveform is extended in inverse-proportion to the terminal voltage of V_F . At this time, the V_F terminal voltage (V_F) and the T_{OFF} terminal voltage have the following relationship :

$$V_F = V_{TOFF} + V_{F(\text{offset})} \quad (2-5)$$

Moreover, the relationship shown in Fig.2-4 is kept between V_F and $V_{F(\text{offset})}$:



[Fig.2-4]

The above means that 0.4V of offset is provided between the V_F terminal voltage and the T_{OFF} terminal voltage. There is an area where the offset amount is decreased, corresponding to decrease of V_F terminal voltage, and $V_{TOFF} = 0$ when V_F terminal voltage is 0.2V. Therefore, in the same way as (2-1), T_{ON} and T_{OFF} are given as follows :

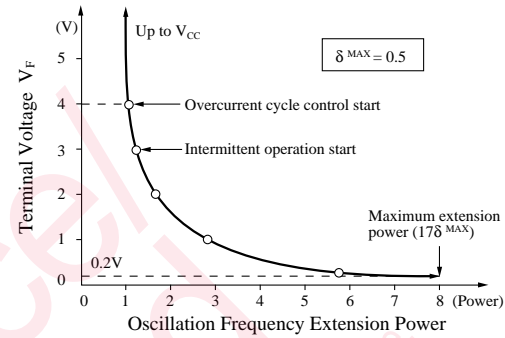
$$T_{ON} = \frac{R_{ON} \cdot C_F \cdot \Delta V_{OSC}}{V_{TON}} \quad (2-6)$$

$$T_{OFF} = \frac{C_F \cdot \Delta V_{OSC}}{\frac{V_F - V_{F(\text{offset})}}{R_{OFF}} + \frac{V_{TON}}{16R_{OFF}}} \quad (2-7)$$

☆) When $V_F = 0.2V$

$$T_{OFF} = \frac{1}{16} T_{ON}$$

Fig.2-5 shows the relationship between the V_F terminal voltage when $\delta^{MAX} = 0.5$ and the oscillation frequency extension power :

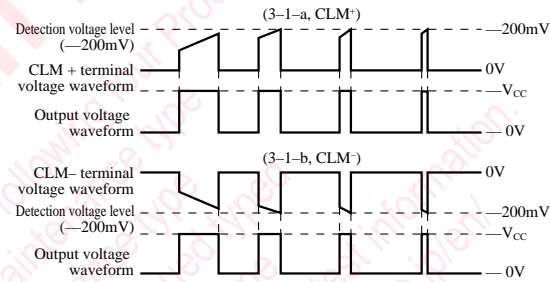


[Fig.2-5]

5.3. Overcurrent Protection Circuit Block

The overcurrent protection circuit of the AN8091/S is intended to control the peak value of the primary side switching current for each cycle. (Refer to Fig.3-1.)

By ensuring the overcurrent upper limit, the output overcurrent limitation and the control such as for the switching device current transient condition can be both achieved.



[Fig.3-1]

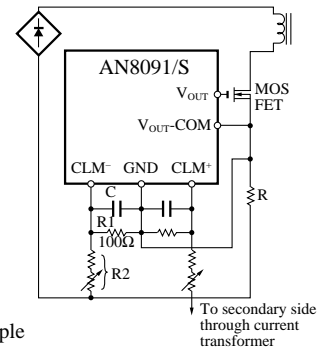
Moreover, the detection voltage is set low ($\pm 200mV$, typ.) to decrease the loss of detection resistance and realize the detection by the sense MOS FET.

If the negative potential side is detected, the detection accuracy will be further improved and influence by noise will be able to be minimized.

(Setting the constant)

The switching current waveform has irregular elements. In order to prevent wrong detection due to these irregular elements, filter is required. The application example is shown in Fig.3-2. The time constant of this filter is :

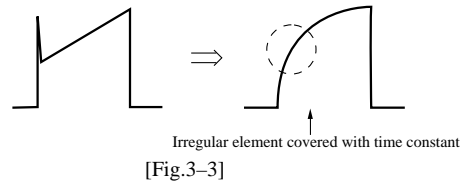
$$T = \frac{C \cdot R1 \cdot R2}{R1 + R2}$$



[Fig.3-2] CLM Application Example

Either of the CLM⁺ terminal and the CLM⁻ terminal has flowing-out current of about 100 to 200μA. Fix the R1 to 100Ω. Compensation is required to cover the height of irregular element of C and R2.

Non-transparent conductive resistor should be used for R1, R2 and detection resistance R.

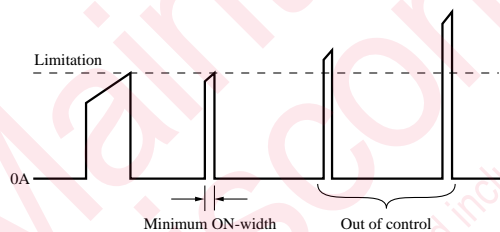


5.4 Overcurrent Cycle Control Function Block (V_F Control Function)

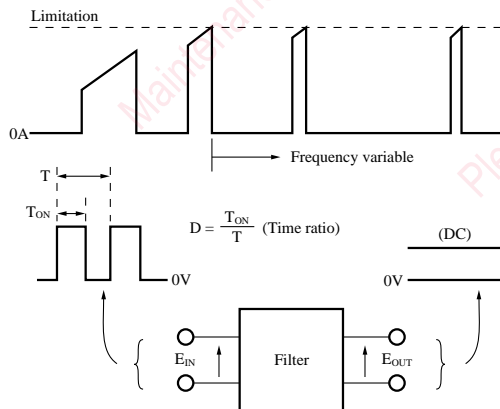
As described in 5.3, the higher the frequency becomes, the more the overcurrent protection suffers from decrease of control range due to response delay. It means :

1. Delay produced by the time constant of filter for preventing the noise malfunction of the overcurrent detection block.
2. Delay of control IC itself
3. Turning off time of the switching device

By the above factors, the ON-period which is minimum-controllable is limited to approx. 0.2 to 0.15μs, producing the areas where control can not be achieved (Refer to Fig.4-1).



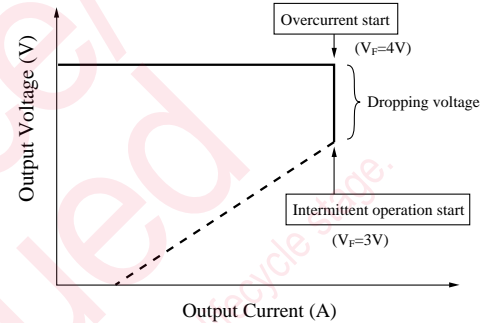
In order to remove the above problem, the AN8091/S incorporates the function which makes the oscillation frequency variable for extension, corresponding the overcurrent condition. The following shows why the above function can realize the extension of control range :



$$\left. \begin{array}{l} \text{[Feed Forward]} \quad E_O = DE_{IN} \\ \text{[Flyback]} \quad E_O = \frac{D}{1-D} E_{IN} \end{array} \right\}$$

$$(D = T_{ON}/T ; \text{Time ratio}) \quad (4-1)$$

The above represents the input and output generally (Refer to Fig.4-3). The above relationship can be kept even under the overcurrent dropping condition.



Therefore, when the output voltage reaches 0V under overcurrent condition, time ratio D should be decreased toward 0. However, since ON period T_{ON} has minimum limitation as described in the above, time ratio D is decreased toward 0 by extending the oscillation frequency T, attempting to satisfy (4-1).

This overcurrent cycle control function works by the output voltage level which is monitored by the V_F terminal. The V_F terminal detects the dropping voltage under the overcurrent condition of power supply output and performs the following function switching according to its level :

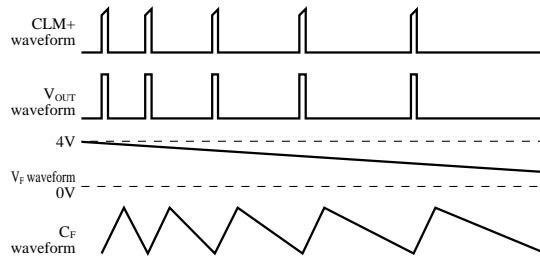
- 1). 4V (typ.) < V_F terminal voltage
○ Overcurrent protection function
- 2). 3V (typ.) < V_F terminal voltage < 4V (typ.)
○ Overcurrent cycle control function (V_F control)
- 3). V_F terminal voltage < 3V (typ.)
○ Overcurrent cycle control function (V_F control)
○ Intermittent operation function (timer control)

When the overcurrent is detected (CLM⁺ side or CLM⁻ side), if the V_F terminal voltage decreases under 4V (typ.), as described in Item 2-2 T_{OFF} terminal voltage keeps the following relationship :

$$V_F = V_{TOFF} + V_{F(\text{offset})} \quad (4-2)$$

Therefore, the T_{OFF} period is extended, corresponding to decrease of V_F terminal voltage (Refer to Fig.2-5). This process is shown in Fig.4-4.

Then, the description shifts to V_F terminal setting.



[Fig.4-4] V_F Terminal Voltage, Oscillation Waveform and Output Waveform

[Setting the V_F terminal]

V_F terminal voltage should set to 5 to 4V.

When it is too high ; ○ overshoot could occur in the primary side control current at power-on or short-circuit of output.

○ Or, timer start point is lowered.

When it is too low ; ○ Oscillation is easy to occur at timer start point.

○ Or, timer start point is raised.

These can be utilized positively.

- For AC-DC power supply, it is impossible from the view of insulation requirements to monitor the power supply output directly. It should be produced simulatively by using the following methods.

- Feed forward method

The voltage in proportion to the power supply output voltage can be obtained, if the IC output pulse voltage is averaged by using the following three facts : The IC supply voltage V_{CC} changes in proportion to the input voltage V_{IN} . The IC output pulse voltage determines the time ratio (D). The peak voltage is in proportion to the V_{CC} .

$$\left. \begin{array}{l} V_{CC} \propto V_{IN} \\ E_{IN} \propto V_{IN} \\ E_O = DE_{IN} \end{array} \right\} \begin{array}{l} \text{Assuming } V_F = DV_{CC}, \\ \hat{I}E_O \propto V_{CC} \hat{I} \text{ Then,} \\ \therefore V_F \propto E_O \end{array}$$

The V_F terminal is set as shown in Fig.4-5.

$$\begin{array}{l} R=15k\Omega \\ C=10000pF \end{array}$$

The above condition is optimum. The setting equations are as follows :

$$V_F = V_{OUT} \times \frac{T_{ON}}{T} \quad [V_F \text{ voltage value}]$$

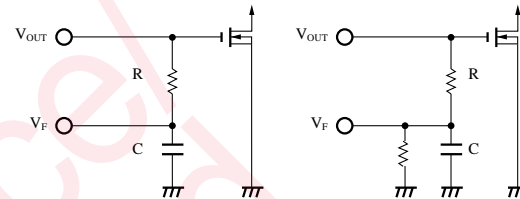
$$DV_F = V_F \left(1 - e^{-\frac{T_{ON}}{RC}} \right) \quad \left[\begin{array}{l} V_F \text{ voltage} \\ \text{ripple value} \end{array} \right]$$

$$\frac{DV_F}{V_F} = 1 - e^{-\frac{T_{ON}}{RC}} \approx 0.1 - 0.05$$

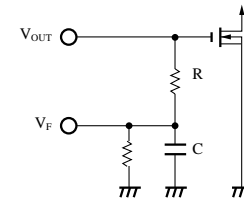
* When the V_F terminal voltage is set lower than the standard value, the circuit as shown in Fig.4-6 should be used.

* Reversely, when it is set higher than the standard value, the circuit as shown in Fig.4-7 should be used.

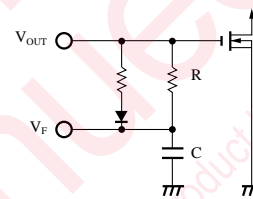
* If the V_{OUT} voltage waveform is distorted due to load connected to the V_{OUT} output, the output circuit should be modified to the circuit shown in Fig.4-8.



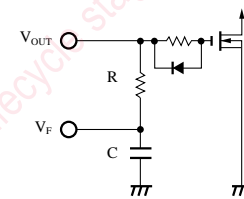
[Fig. 4-5] Standard



[Fig. 4-6] Set Lower



[Fig. 4-7] Set Higher



[Fig. 4-8]

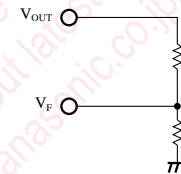
- Flyback method

When the IC supply voltage V_{CC} is supplied from the flyback voltage, the following expression is made :

$$V_{CC} \propto E_O$$

Then, inputting the divided V_{CC} voltage to the V_F terminal, the following relationship can be produced :

$$V_F \propto E_O$$



5.5. Intermittent Operation Function (Timer Control Function)

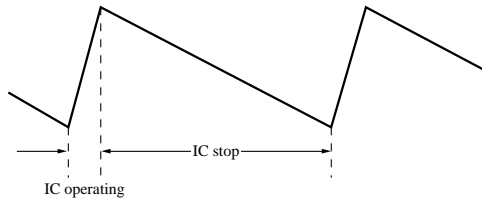
When the overcurrent is detected from the CLM+ or CLM- terminal, and the monitor voltage of output voltage which is inputted to the V_F terminal is decreased under 3V (typ.), the intermittent operation (timer operation) starts. The intermittent operation suppresses the effective current in the secondary side by the following procedures :

The capacitor which is connected to the CT terminal is given the triangular oscillation by :

- (Charging : 125 μ A
- Discharging : 15 μ A
- Hysteresis width : 6 μ A (upper limit 8V (typ.))
- lower limit 2V (typ.))

And the operation cycle, which consists of operation for charging time and stop for discharging time, is repeated (Refer to Fig.5-1).

The above operation decreases the burden on the second rectification diode and the load, and suppresses the loss.



[Fig.5-1] Timer Waveform

This operation can be effective particularly under the overload condition of one output of multi-output power supply.

[Setting the constant]

- (Parameter)
- Timer terminal charging current : $I_{ch}^{timer} = 125\mu A$
 - Timer terminal discharging current : $I_{d-ch}^{timer} = 15\mu A$
 - Timer waveform upper limit voltage : $V_H^{timer} = 8V$
 - Timer waveform lower limit voltage : $V_L^{timer} = 2V$
 - Timer operation : Operating : Stop = 1 : 8

Timer cycle : T_{timer}

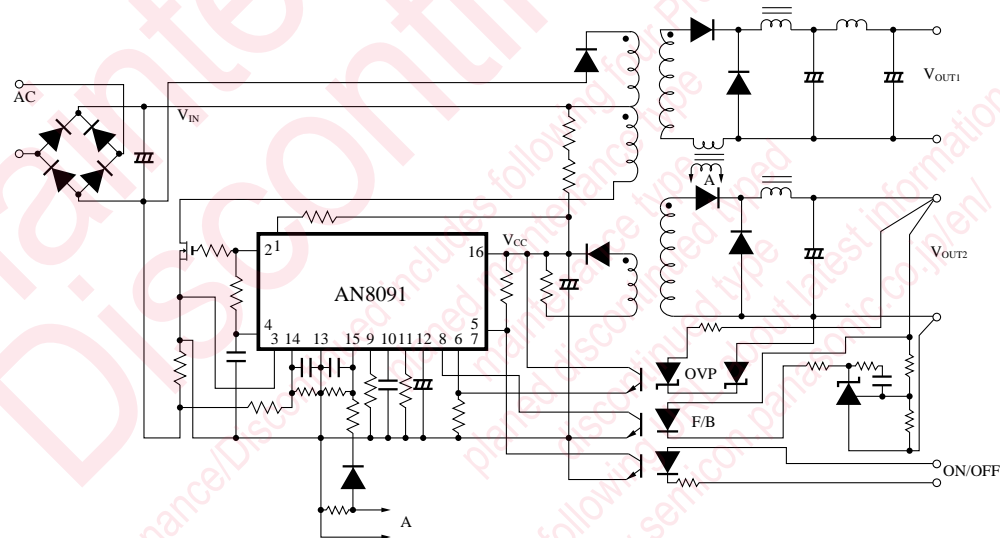
$$T_{timer} = C_T (V_H^{timer} - V_L^{timer}) \left(\frac{1}{I_{ch}^{timer}} + \frac{1}{I_{d-ch}^{timer}} \right)$$

However, the following expression must be satisfied :

$$\text{Power supply rise time} < \frac{C_T (V_H^{timer} - V_L^{timer})}{I_{ch}^{timer}}$$

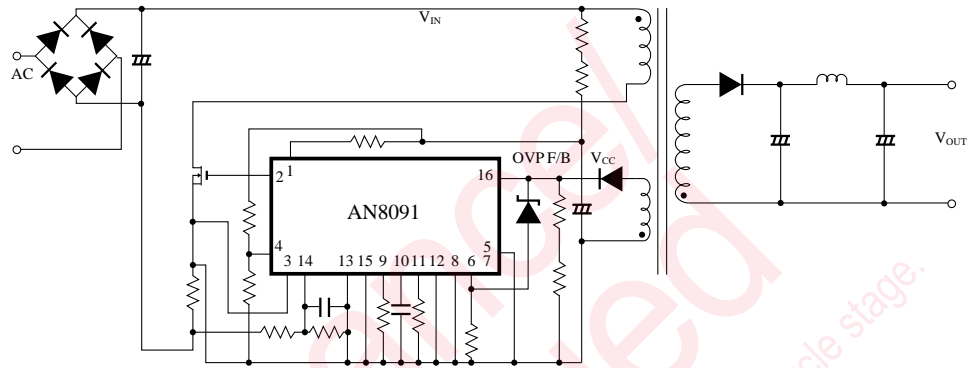
$$\left(\begin{array}{l} 0.12\text{sec when} \\ C_T = 4.7\mu F \end{array} \right)$$

[Feed Forward Application]



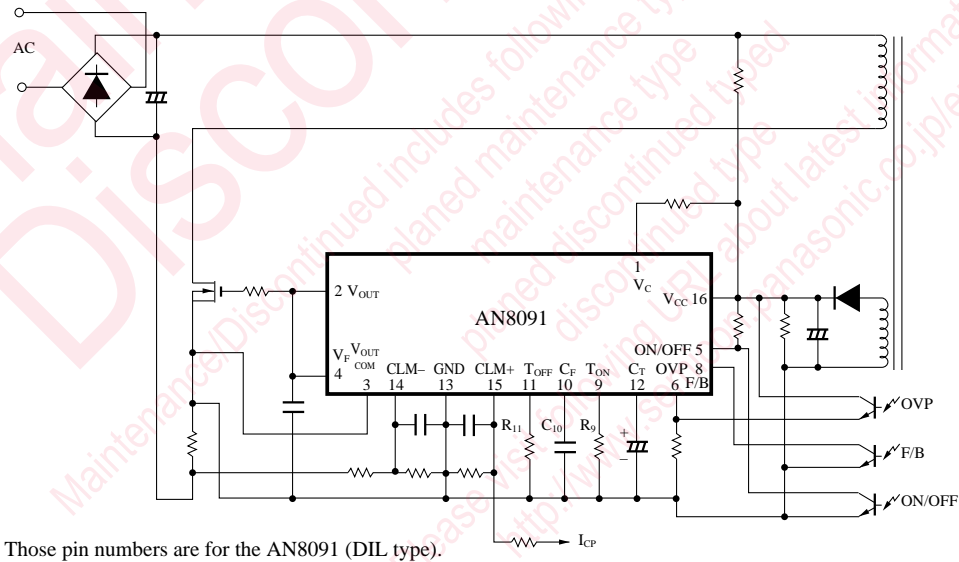
Those pin numbers are for the AN8091 (DIL type).

[Flyback Application]



Those pin numbers are for the AN8091 (DIL type).

[Feed Forward Application]



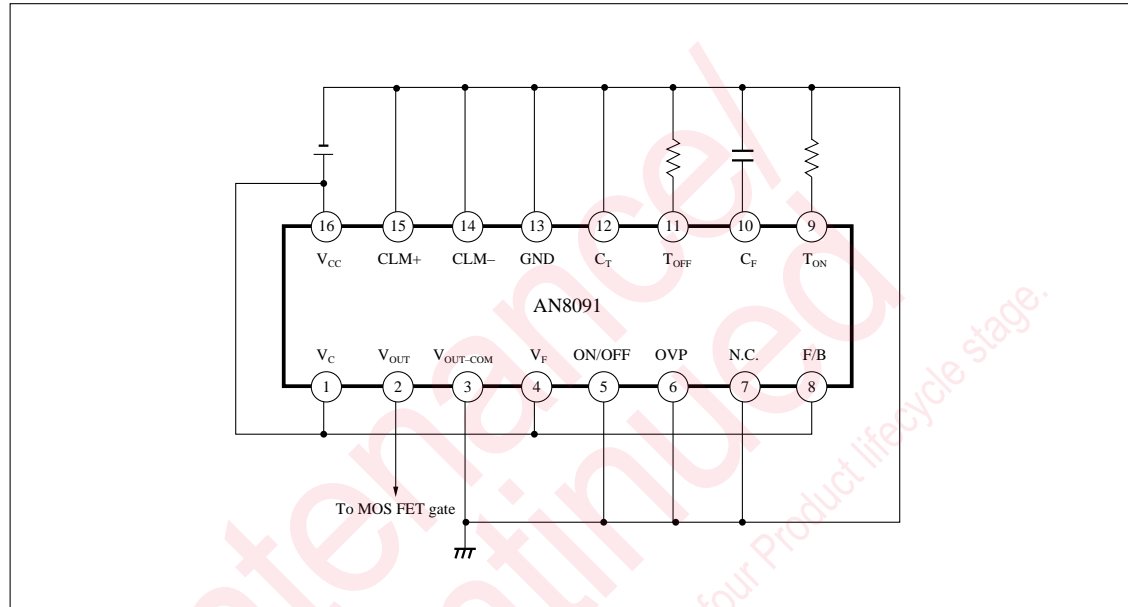
Those pin numbers are for the AN8091 (DIL type).

[Terminal treatment when some functions are not used]

The following shows the terminal treatment when some functions are not used. In order to avoid the influence by noise, the terminal should be out of the open condition.

[Terminal treatment when some functions are not used]

The following shows the terminal treatment when some functions are not used. In order to avoid the influence by noise, the terminal should be out of the open condition.



Pin Function Descriptions

AN8091 Pin No.	Symbol	Treatment
4	V_F	Maintain its voltage in the range from the V_F control start voltage (4V) to the V_{CC} . However, the V_F control and timer control should not be used and only the overcurrent protection function should be used.
5	ON/OFF	Maintain its voltage under the $V_{TH(ON/OFF)}$ (approx. 2.8V). It is the most convenient and easy to drop to the GND.
6	OVP	Maintain its voltage under the $V_{TH(OVP)}$ (approx. 1.4V). It is most convenient and easy to drop to the GND. Particular care should be taken because it is very weak against noise.
8	F/B	Maintain its voltage in the range from 7V to the V_{CC} .
12	C_T	Maintain its voltage in the range from 0 to 7V. Since the current of approx. 125 μ A flows out, set the terminal impedance low. It is most convenient and easy to drop to the GND.
14	CLM ⁻	Maintain its voltage in the range from $V_{TH\ CLM^-}$ (approx. -0.2V) to 0.3V. Since the current of approx. 130 μ A flows out, set the terminal impedance low. It is most convenient and easy to drop to the GND.
15	CLM ⁺	Maintain its voltage in the range from -0.3V to $V_{TH\ CLM^+}$ (approx. -0.2V). Since the current of approx. 200 μ A flows out, set the terminal impedance low. It is most convenient and easy to drop to the GND.

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