

Silicon PNP Power Transistors

2SB966

DESCRIPTION

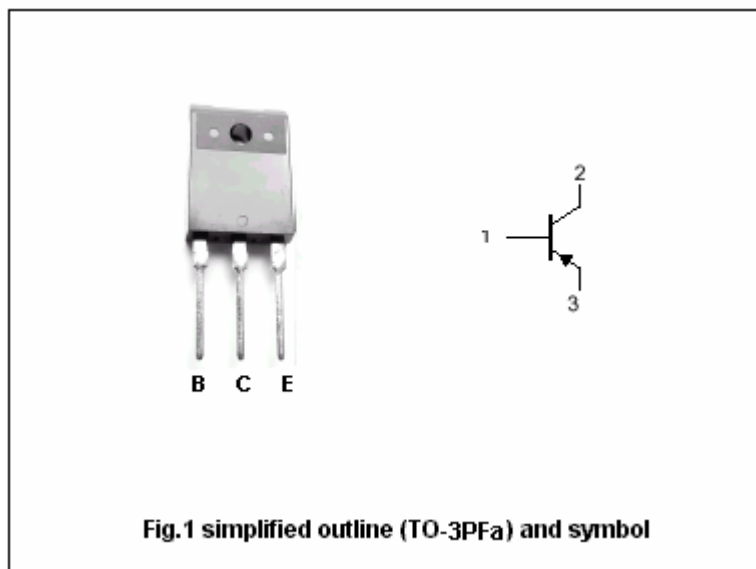
- With TO-3PFa package
- Complement to type 2SD1289

APPLICATIONS

- For use in low frequency and power amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

Absolute maximum ratings($T_a=25$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-120	V
V_{CEO}	Collector-emitter voltage	Open base	-120	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-8	A
I_{CM}	Collector current-peak		-12	A
P_C	Collector power dissipation	$T_C=25$	80	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA ; I _B =0	-120			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-5A ; I _B =-0.5A			-1.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-5A ; I _B =-0.5A			-2.0	V
I _{CBO}	Collector cut-off current	V _{CB} =-120V; I _E =0			-50	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-50	μ A
h _{FE -1}	DC current gain	I _C =-1A ; V _{CE} =-5V	60		320	
h _{FE -2}	DC current gain	I _C =-5A ; V _{CE} =-5V	20			
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =-10V; f=1MHz		200		pF
f _T	Transition frequency	I _C =-1A ; V _{CE} =-5V		65		MHz

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PACKAGE OUTLINE

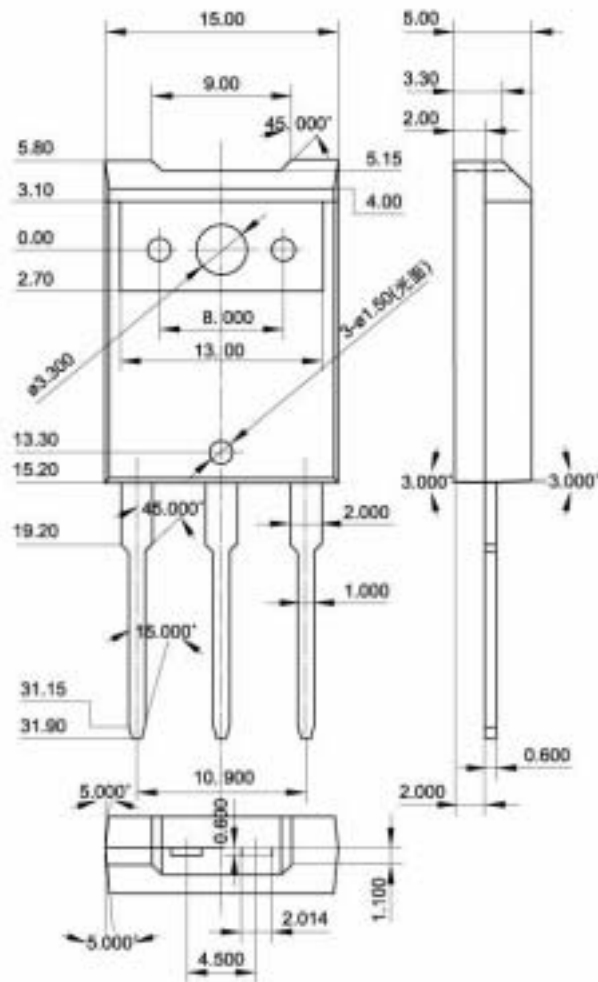


Fig.2 Outline dimensions (unindicated tolerance: ± 0.30 mm)