Ordering number:ENN2019A

PNP/NPN Epitaxial Planar Silicon Transistors

2SB1124/2SD1624

High Current Switching Applications

Applications

Voltage regulators, relay drivers, lamp drivers, electrical equipment.

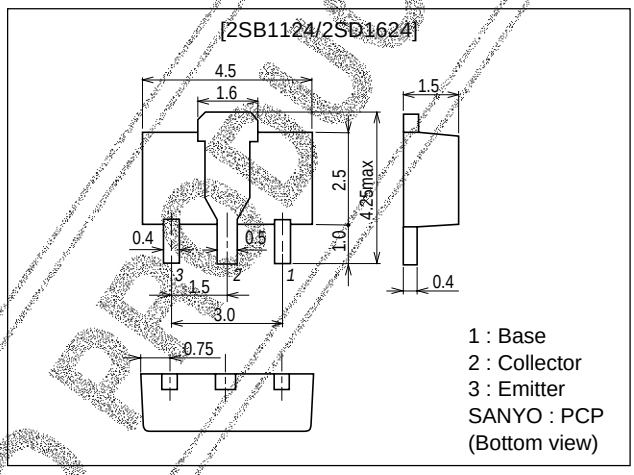
Features

Adoption of FBET, MBIT processes.
Low collector-to-emitter saturation voltage.
Fast switching speed.
Large current capacity and wide ASO.

Package Dimensions

unit:mm

2038A



( ) : 2SB1124

Specifications

Absolute Maximum Ratings at Ta = 25 C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		(–)60	V
Collector-to-Emitter Voltage	V_{CEO}		(–)50	V
Emitter-to-Base Voltage	V_{EBO}		(–)6	V
Collector Current	I_C		(–)3	A
Collector Current (Pulse)	I_{CP}		(–)6	A
Collector Dissipation	P_C		500	mW
		Mounted on ceramic board (250mm²×0.8mm)	1.5	W
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25 C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=(–)40V, I_E=0			(–)1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(–)4V, I_C=0			(–)1	μA
DC Current Gain	$h_{FE}1$	V_{CE}=(–)2V, I_C=(–)100mA	100*		560*	
	$h_{FE}2$	V_{CE}=(–)2V, I_C=(–)3A	35			
Gain-Bandwidth Product	f_T	V_{CE}=(–)10V, I_C=(–)50mA		150		MHz

* ; The 2SB1124/2SD1624 are classified by 100mA h_{FE} as follows :

Rank	R	S	T	U
h_{FE}	100 to 200	140 to 280	200 to 400	280 to 560

Marking 2SB1124 : BG
2SD1624 : DG

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SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

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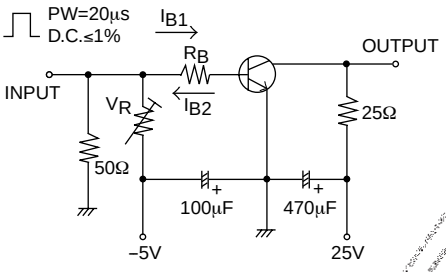
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output Capacitance	C_{ob}	V_{CB}=(–)10V, f=1MHz		(39)		pF
				25		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=(–)2A, I_B=(–)100mA		(–0.35)	(–0.7)	V
				0.19	0.5	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=(–)2A, I_B=(–)100mA		(–0.94)	(–)1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=(–)10μA, I_E=0	(–)60			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=(–)1mA, R_{BE}=∞	(–)50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=(–)10μA, I_C=0	(–)6			V
Turn-ON Time	t_{on}	See specified Test Circuit.		70		ns
				(70)		ns
Storage Time	t_{stg}	See specified Test Circuit.		650		ns
				(450)		ns
Fall Time	t_f	See specified Test Circuit.		35		ns
				(35)		ns

Switching Time Test Circuit



$10I_{B1}$= $-10I_{B2}$=I_C=1A
(For PNP, the polarity is reversed.)