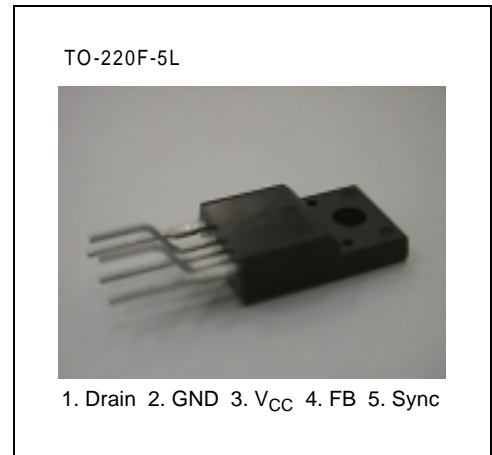


S P S

The SPS product family is specially designed for an off-line SMPS with minimal external components. The SPS consist of high voltage power SenseFET and current mode PWM IC. Included PWM controller features integrated fixed oscillator, under voltage lock out, leading edge blanking, optimized gate turn-on/turn-off driver, thermal shut down protection, over voltage protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or RCC switching converter solution, a SPS can reduce total component count, design size, and weight and at the same time increase efficiency, productivity, and system reliability. It has a basic platform well suited for cost-effective design in Quasi-Resonant Converter as C-TV power supply.



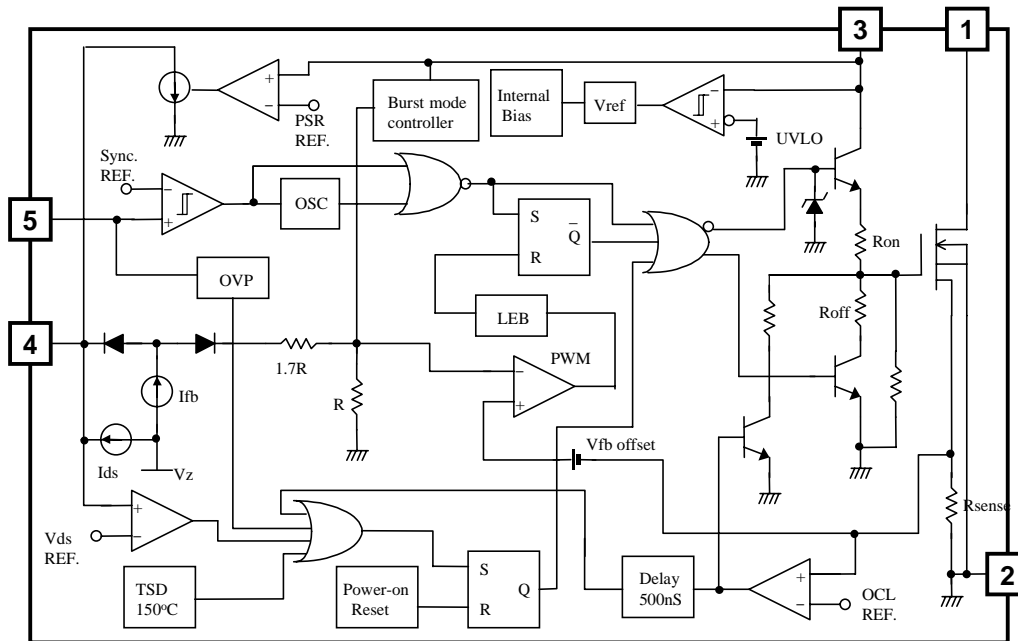
FEATURES

- Quasi Resonant Converter Controller
- Internal Burst mode Controller for Stand-by mode
- Pulse by pulse current limiting
- Over current Latch protection
- Over voltage protection (Vsync: Min. 11V)
- Internal thermal shutdown function
- Under voltage lockout
- Internal high voltage sense FET
- Auto-restart mode

ORDERING INFORMATION

| Device | Package | Topr (°C) |
|------------|------------|----------------|
| KA5Q0765RT | TO-220F-5L | -25°C to +85°C |

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Value | Unit |
|--|-------------------------|-------------------------|-----------------|
| Drain-source (GND) voltage ⁽¹⁾ | V _{DSS} | 650 | V |
| Drain-Gate voltage (R _{GS} =1MΩ) | V _{DGR} | 650 | V |
| Gate-source (GND) voltage | V _{GS} | ±30 | V |
| Drain current pulsed ⁽²⁾ | I _{DM} | 28.0 | A _{DC} |
| Single pulsed avalanche energy ⁽³⁾ | E _{AS} | 570 | mJ |
| Avalanche current ⁽⁴⁾ | I _{AS} | 20 | A |
| Continuous drain current (T _C =25°C) | I _D | 7.0 | A _{DC} |
| Continuous drain current (T _C =100°C) | I _D | 5.6 | A _{DC} |
| Supply voltage | V _{CC} | 30 | V |
| Analog input voltage range | V _{FB} | -0.3 to V _{SD} | V |
| Total power dissipation | P _D (wt H/S) | 135 | W |
| | Derating | 1.1 | W/°C |
| Operating temperature | T _{OPR} | -25 to +85 | °C |
| Storage temperature | T _{STG} | -55 to +150 | °C |

NOTES:

1. T_j=25°C to 150°C
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L=24mH, starting T_j=25°C
4. L=13uH, starting T_j=25°C

ELECTRICAL CHARACTERISTICS (SFET part)

(Ta=25°C unless otherwise specified)

| Characteristic | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|--------------|---|------|------|------|----------|
| Drain-source breakdown voltage | BV_{DSS} | $V_{GS}=0V, I_D=50\mu A$ | 650 | – | – | V |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=\text{Max.}, \text{Rating}, V_{GS}=0V$ | – | – | 200 | μA |
| | | $V_{DS}=0.8\text{Max.}, \text{Rating}, V_{GS}=0V, T_C=125^\circ C$ | – | – | 500 | μA |
| Static drain-source on resistance ^(note) | $R_{DS(ON)}$ | $V_{GS}=10V, I_D=4.0A$ | – | 1.25 | 1.6 | Ω |
| Forward transconductance ^(note) | gfs | $V_{DS}=15V, I_D=4.0A$ | 3.0 | – | – | S |
| Input capacitance | C_{iss} | $V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ | – | 1600 | – | pF |
| Output capacitance | C_{oss} | | – | 310 | – | |
| Reverse transfer capacitance | C_{rss} | | – | 120 | – | |
| Turn on delay time | td(on) | $V_{DD}=0.5BV_{DSS}, I_D=7.0A$ (MOSFET switching time are essentially independent of operating temperature) | – | 25 | – | nS |
| Rise time | tr | | – | 55 | – | |
| Turn off delay time | td(off) | | – | 80 | – | |
| Fall time | tf | | – | 50 | – | |
| Total gate charge (gate-source+gate-drain) | Qg | $V_{GS}=10V, I_D=7.0A, V_{DS}=0.5BV_{DSS}$ (MOSFET switching time are essentially independent of operating temperature) | – | – | 72 | nC |
| Gate-source charge | Qgs | | – | 9.3 | – | |
| Gate-drain (Miller) charge | Qgd | | – | 29.3 | – | |

NOTE: Pulse test: Pulse width $\leq 300\mu S$, duty cycle $\leq 2\%$

ELECTRICAL CHARACTERISTICS (Control part)

(Ta=25°C unless otherwise specified)

| Characteristic | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|--|---------------------|---|------|------|------|------|
| SENSE FET SECTION | | | | | | |
| Drain to PKG Breakdown voltage | BVpkg | 60Hz AC, Ta=25°C | 3500 | – | – | V |
| Drain to Source Breakdown voltage | BVdss | Vdrain=650V, Ta=25°C | 650 | – | – | V |
| Drain to Source Leakage current | Idss | Vdrain=650V, Ta=25°C | – | – | 200 | μA |
| OSCILLATOR SECTION | | | | | | |
| Initial Frequency | F _{OSC} | – | 18 | 20 | 22 | KHz |
| Voltage Stability | F _{STABLE} | 12≤V _{CC} ≤23V | 0 | 1 | 3 | % |
| Temperature Stability ^{note 2} | ΔF _{OSC} | -25°C≤Ta≤85°C | 0 | ±5 | ±10 | % |
| Maximum Duty Cycle | D _{MAX} | – | 92 | 95 | 98 | % |
| Minimum Duty Cycle | D _{MIN} | – | – | – | 0 | % |
| UVLO SECTION | | | | | | |
| Start Threshold Voltage | V _{START} | V _{FB} =GND | 14 | 15 | 16 | V |
| Stop Threshold Voltage | V _{STOP} | V _{FB} =GND | 8 | 9 | 10 | V |
| FEEDBACK SECTION | | | | | | |
| Feedback Source Current | I _{FB} | V _{FB} =GND | 0.7 | 0.9 | 1.1 | mA |
| Shutdown Feedback Voltage | V _{SD} | V _{fb} >6.9V | 6.9 | 7.5 | 8.1 | V |
| Shutdown Delay Current | I _{DELAY} | V _{FB} =5V | 4 | 5 | 6 | μA |
| PROTECTION SECTION | | | | | | |
| Over Current Protection | V _{OVP} | V _{sync} ≥11V | 11 | 12 | 13 | V |
| Over Current Latch Voltage ^{note 2} | V _{OCL} | – | 0.9 | 1.0 | 1.1 | V |
| Thermal shutdown Temp. | TSD | – | 140 | 160 | – | °C |
| SYNC SECTION | | | | | | |
| Normal Sync High Threshold Voltage | V _{NSH} | V _{CC} =16V, V _{fb} =5V | 4.0 | 4.6 | 5.2 | V |
| Normal Sync Low Threshold Voltage | V _{NSL} | V _{CC} =16V, V _{fb} =5V | 2.3 | 2.6 | 2.9 | V |
| Burst High Threshold Voltage | V _{BSH} | V _{CC} =10.5V, V _{fb} =0V | 3.2 | 3.6 | 4.0 | V |
| Burst Low Threshold Voltage | V _{BSL} | V _{CC} =10.5V, V _{fb} =0V | 1.1 | 1.3 | 1.5 | V |

ELECTRICAL CHARACTERISTICS (Continued)

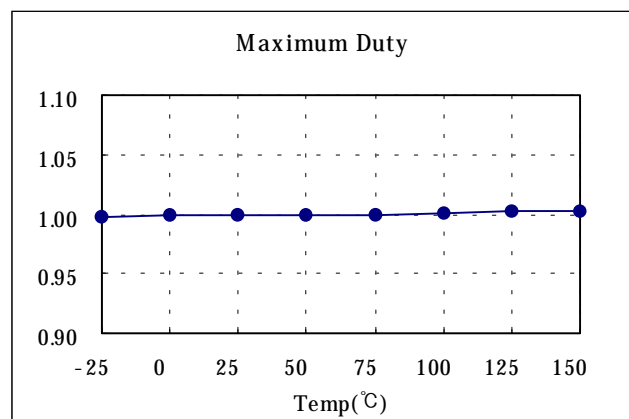
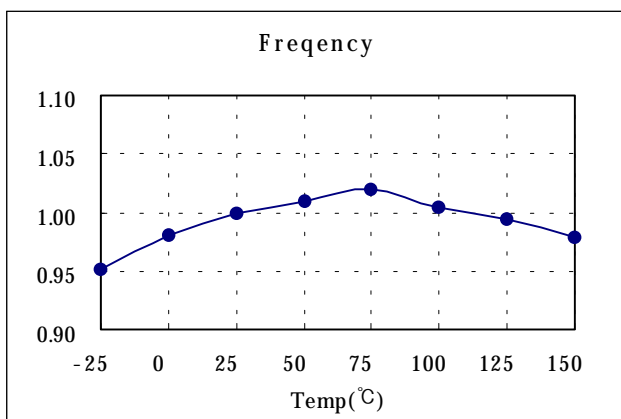
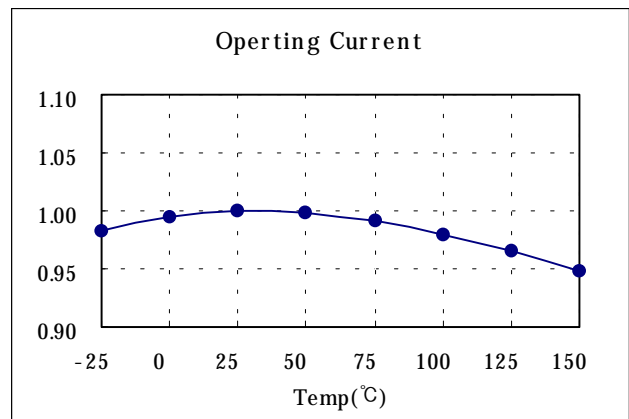
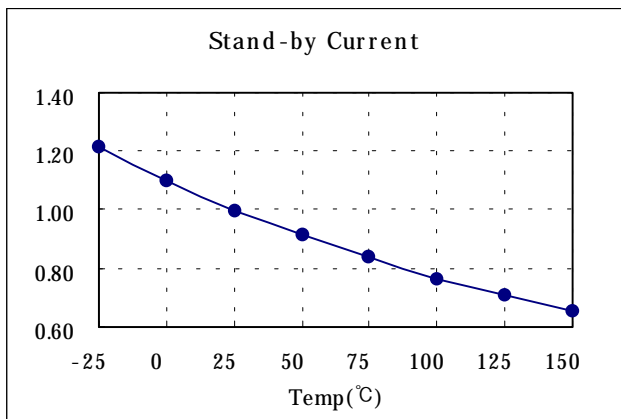
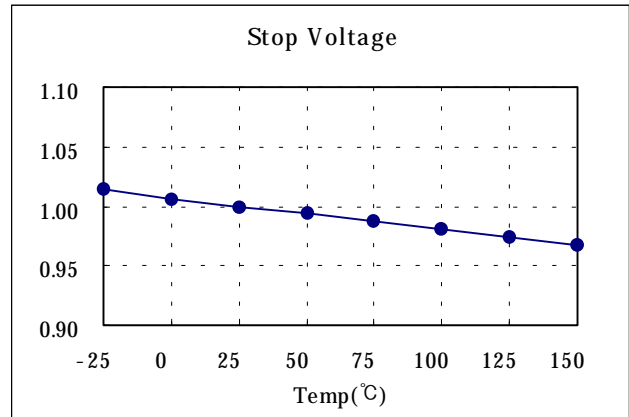
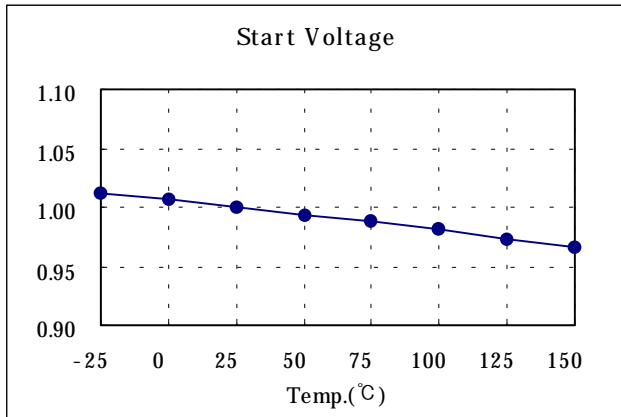
(Ta=25°C unless otherwise specified)

| Characteristic | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|--|----------------------|---|------|------|------|------|
| BURST MODE SECTION | | | | | | |
| Burst mode Low Threshold Voltage | V _{BURL} | V _{fb} =0V | 10.4 | 11.0 | 11.6 | V |
| Burst mode High Threshold Voltage | V _{BURH} | V _{fb} =0V | 11.4 | 12.0 | 12.6 | V |
| Burst mode Enable Feedback voltage | V _{BEN} | V _{CC} =10.5V | 0.7 | 1.0 | 1.3 | V |
| Burst mode Peak Current Limit | I _{BU_PK} | V _{CC} =10.5V | 0.65 | 0.85 | 1.0 | V |
| PRIMARY SIDE REGULATION SECTION | | | | | | |
| Primary Regulation Threshold Voltage | V _{PR} | I _{fb} =700μA, V _{fb} =4V | 32.0 | 32.5 | 33.0 | V |
| Primary Regulation Transconductance | G _{PR} | – | 2.0 | 2.6 | – | mA/V |
| CURRENT LIMIT (SELF-PROTECTION) SECTION | | | | | | |
| Peak Current Limit ^{note 3} | I _{PK} | – | 4.4 | 5.0 | 5.6 | A |
| START UP CURRENT | | | | | | |
| Start up Current | I _{START} | V _{fb} =GND, V _{CC} =14V | – | 0.1 | 0.2 | mA |
| Operatig Supply Current ^{noet 1} | I _{OP} | V _{fb} =GND, V _{CC} =16V | – | 10 | 18 | mA |
| | I _{OP(MIN)} | V _{fb} =GND, V _{CC} =12V | | | | |
| | I _{OP(MAX)} | V _{fb} =GND, V _{CC} =28V | | | | |

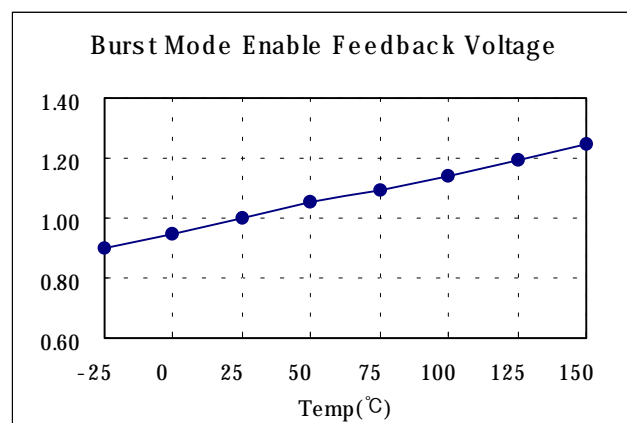
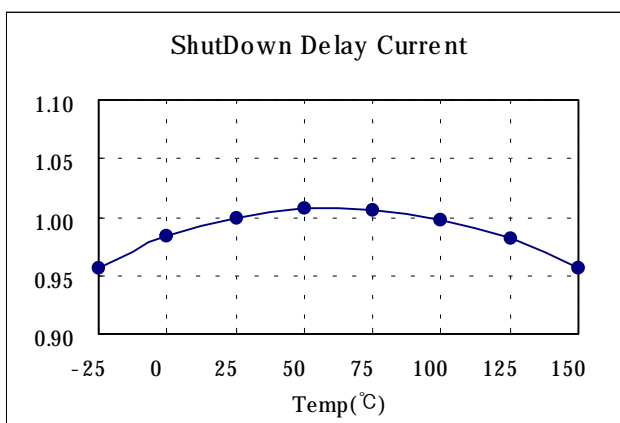
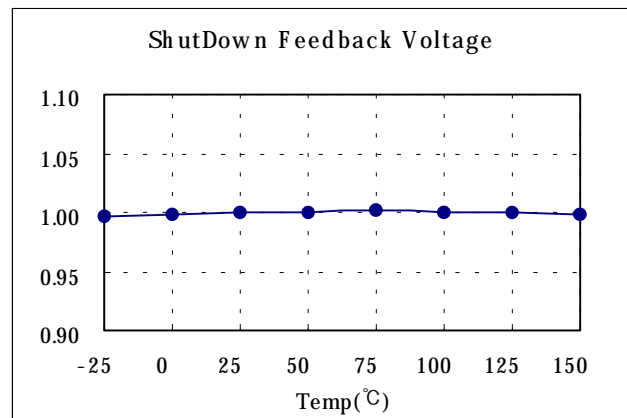
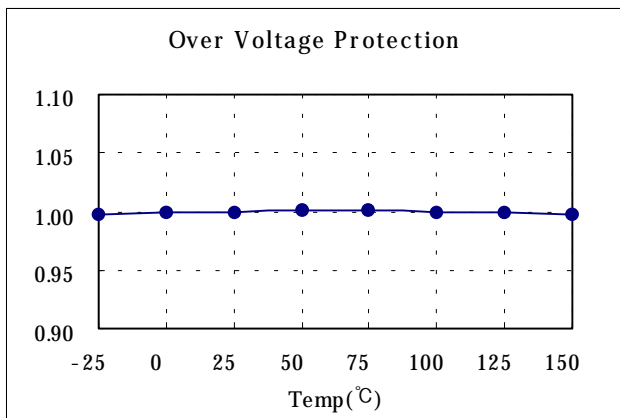
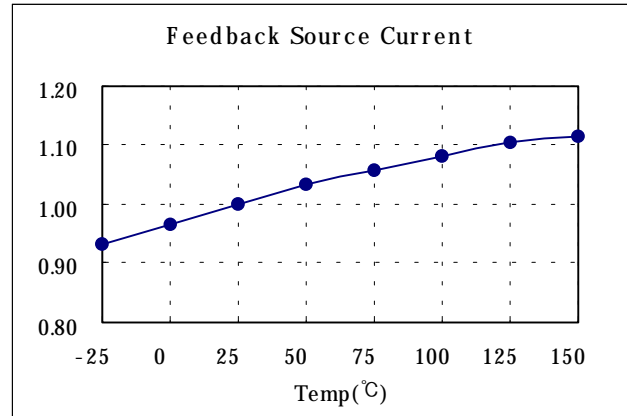
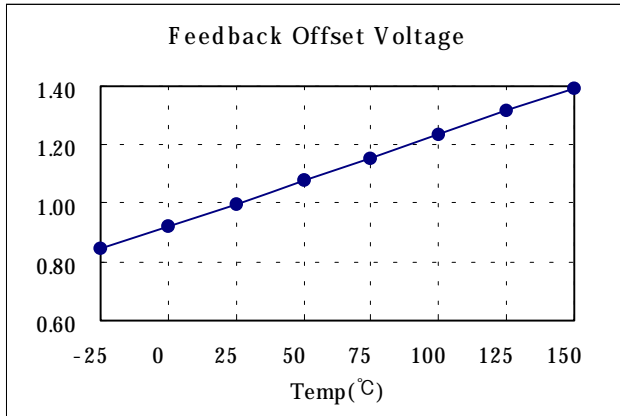
NOTE:

1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. These parameters indicate inductor current

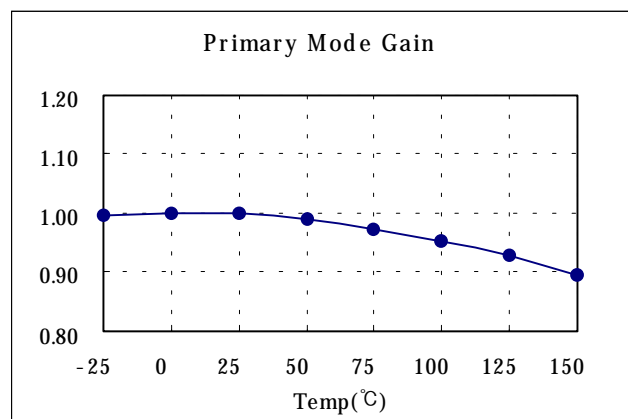
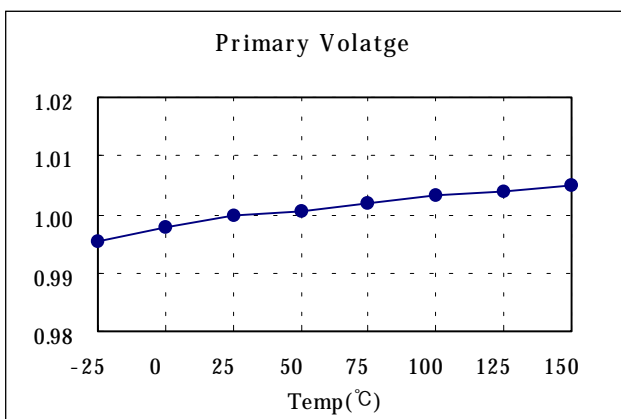
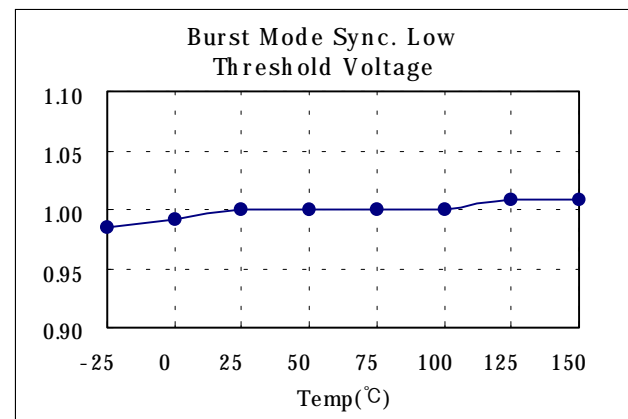
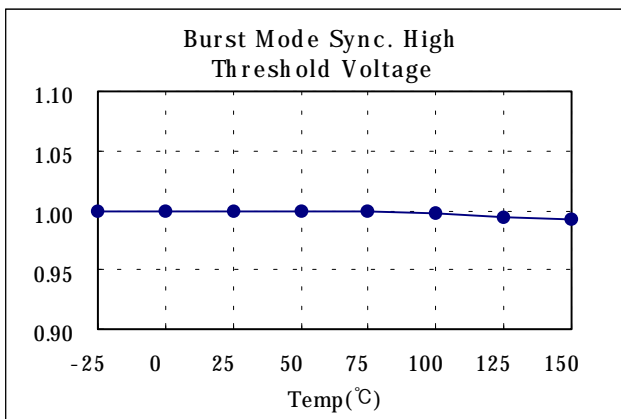
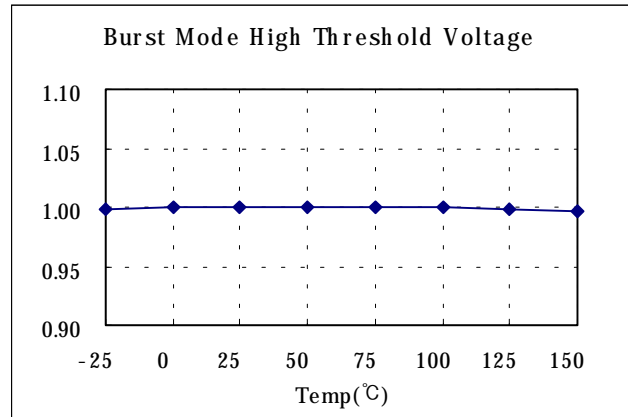
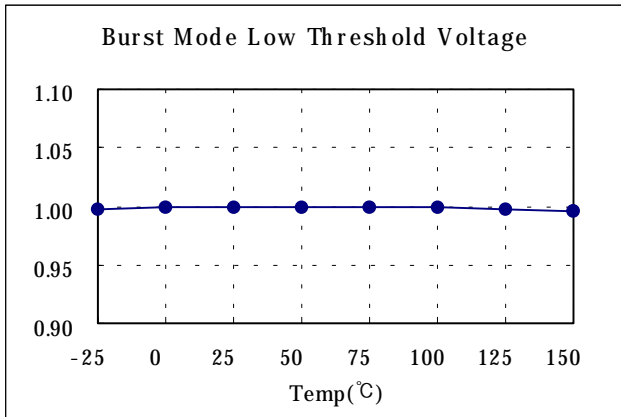
TYPICAL PERFORMANCE CHARACTERISTICS



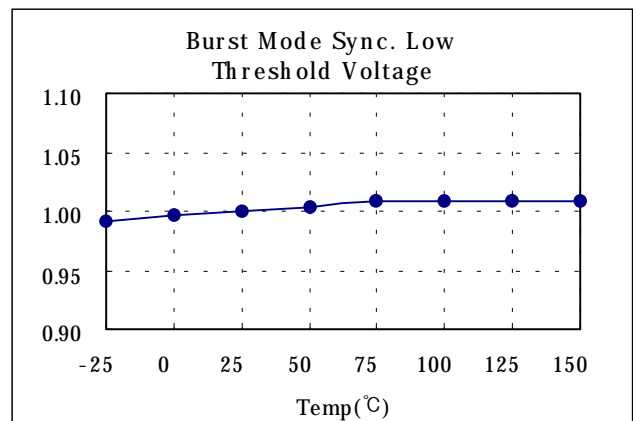
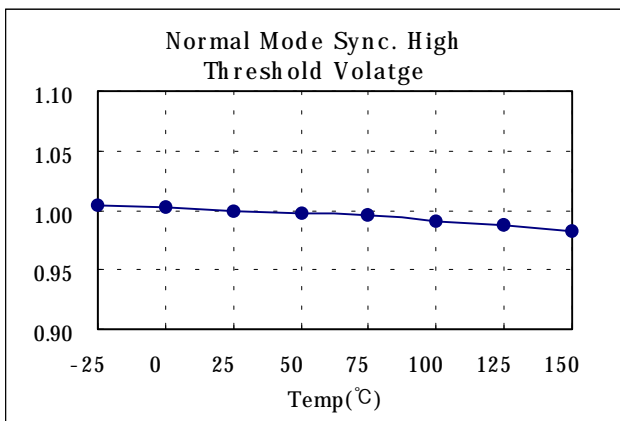
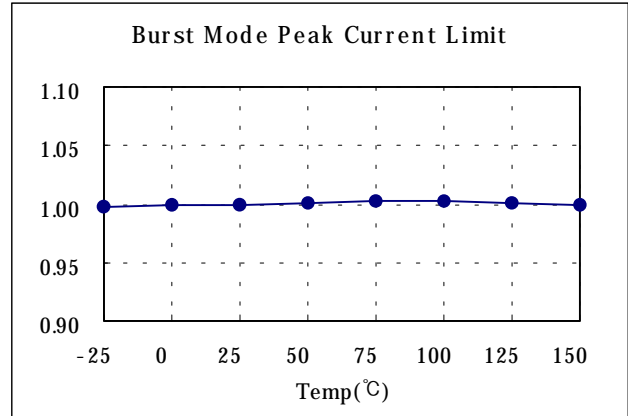
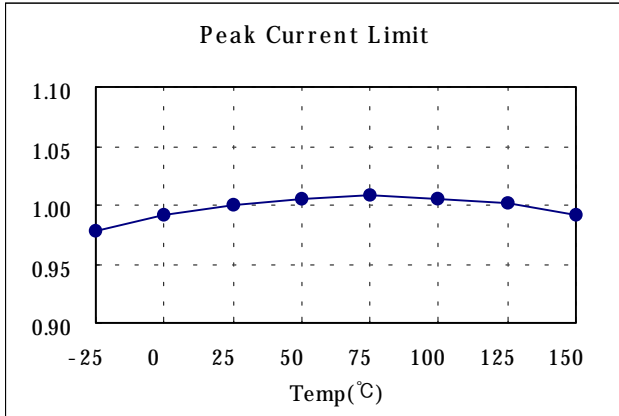
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



LIFE SUPPORT POLICY

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