Advanced Power MOSFET

SSP60N06

FEATURES

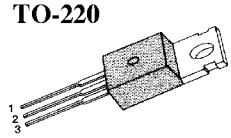
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 ¥ A (Max.) @ V_{DS} = 60V
- Lower $R_{DS(ON)}$: 0.015¥ (Typ.)

BV_{DSS} = 60 V

$R_{DS(on)}$ = 0.018¥

I_D = 60 A

TO-220



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current (T_C=25¡)	60	A
	Continuous Drain Current (T_C=100¡)	42	
I_{DM}	Drain Current-Pulsed ¤	240	A
V_{GS}	Gate-to-Source Voltage	¡ 20	V
E_{AS}	Single Pulsed Avalanche Energy ¤ Ł	216	mJ
I_{AR}	Avalanche Current ¤	60	A
E_{AR}	Repetitive Avalanche Energy ¤	19	mJ
dv/dt	Peak Diode Recovery dv/dt ¤ Ø	5.5	V/ns
P_D	Total Power Dissipation (T_C=25¡)	190	W
	Linear Derating Factor	1.25	W/¡
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	¡
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8£ ßfrom case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{¥ JC}$	Junction-to-Case	--	0.8	¡ /W
$R_{¥ CS}$	Case-to-Sink	0.5	--	
$R_{¥ JA}$	Junction-to-Ambient	--	62.5	

SAMSUNG ELECTRONICS

Electrical Characteristics (T_C=25¡ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	60	--	--	V	V_{GS}=0V,I_D=250¥ A
¥ BV/¥ T_J	Breakdown Voltage Temp. Coeff.	--	0.032	--	V/¡	I_D=250¥ A ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V,I_D=250¥ A
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-20V
I_{DSS}	Drain-to-Source Leakage Current	--	--	250	¥ A	V_{DS}=60V
		--	--	1000		V_{DS}=48V,T_C=150¡
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.018	$	V_{GS}=10V,I_D=30A ¤ E
g_{fs}	Forward Transconductance	20	--	--	S	V_{DS}=30V,I_D=30A ¤ E
C_{iss}	Input Capacitance	--	3500	--	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	1020	--		
C_{rss}	Reverse Transfer Capacitance	--	170	--		
$t_{d(on)}$	Turn-On Delay Time	--	20	35	ns	V_{DD}=25V,I_D=60A, R_G=6.0$ ***See Fig 13*** ¤ E ¤ °
t_r	Rise Time	--	10	25		
$t_{d(off)}$	Turn-Off Delay Time	--	45	60		
t_f	Fall Time	--	45	60		
Q_g	Total Gate Charge	--	--	120	nC	V_{DS}=48V,V_{GS}=10V, I_D=60A ***See Fig 6 & Fig 12*** ¤ E ¤ °
Q_{gs}	Gate-Source Charge	--	20	--		
Q_{gd}	Gate-Drain(£ Miller£) Charge	--	30	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	60	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ¤	--	--	240		
V_{SD}	Diode Forward Voltage ¤ E	--	--	2.0	V	T_J=25¡ ,I_S=60A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	160	--	ns	T_J=25¡ ,I_F=60A
Q_{rr}	Reverse Recovery Charge	--	0.15	--	¥ C	di_F/dt=100A/¥ s ¤ E

Notes ;

¤ Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

¤ £L=0.5mH, I_{AS}=60A, V_{DD}=30V, R_G=25$, Starting T_J=25¡

¤ ØI_{SD}¡ 60A, di/dt¡ 100A/¥ s, V_{DD}¡ BV_{DSS}, Starting T_J=25¡

¤ EPulse Test : Pulse Width = 250¥ s, Duty Cycle ¡ 2%

¤ °Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

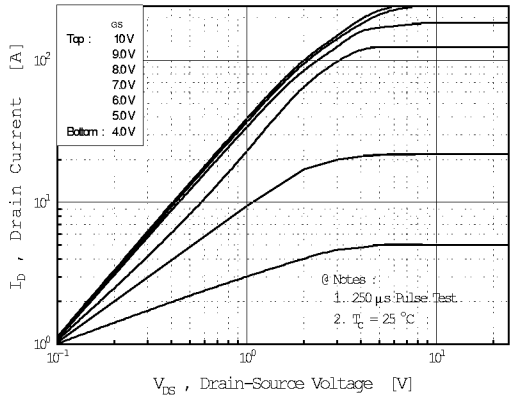


Fig 2. Transfer Characteristics

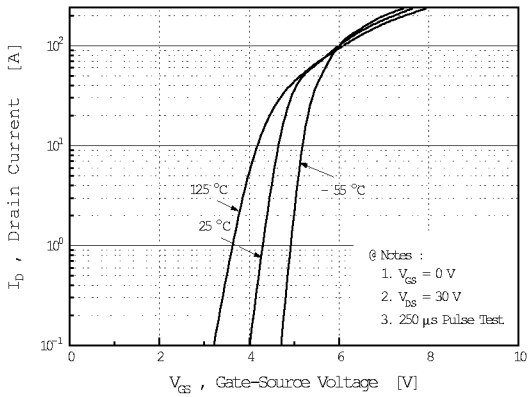


Fig 3. On-Resistance vs. Drain Current

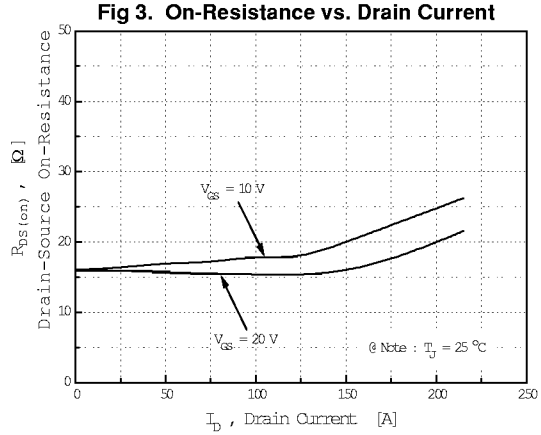


Fig 4. Source-Drain Diode Forward Voltage

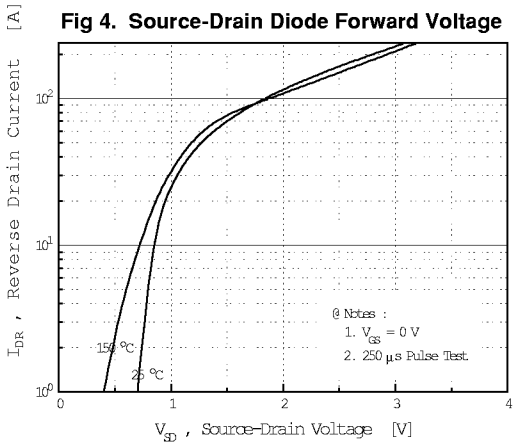


Fig 5. Capacitance vs. Drain-Source Voltage

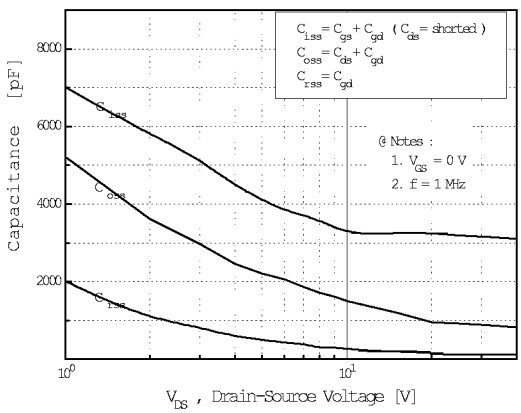


Fig 6. Gate Charge vs. Gate-Source Voltage

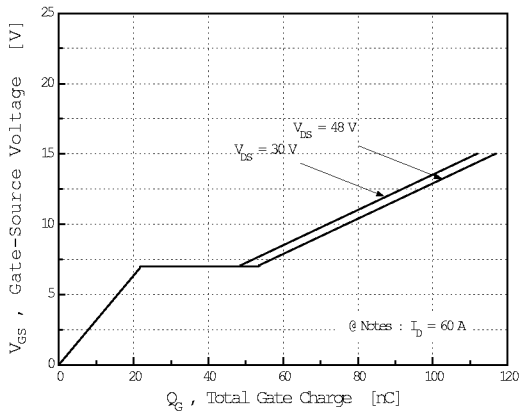


Fig 7. Breakdown Voltage vs. Temperature

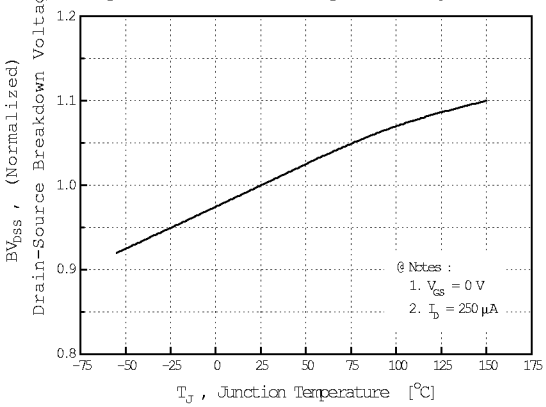


Fig 8. On-Resistance vs. Temperature

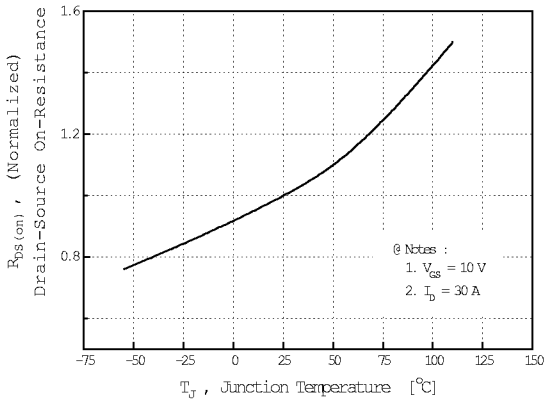


Fig 9. Max. Safe Operating Area

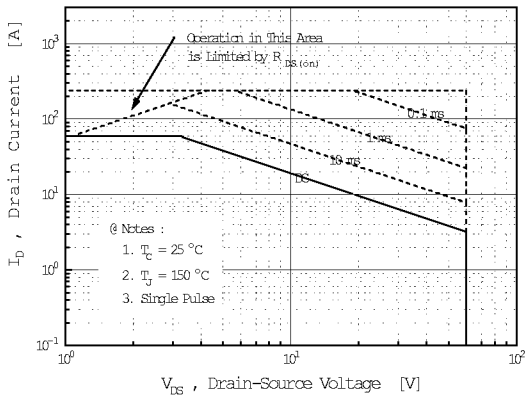


Fig 10. Max. Drain Current vs. Case Temperature

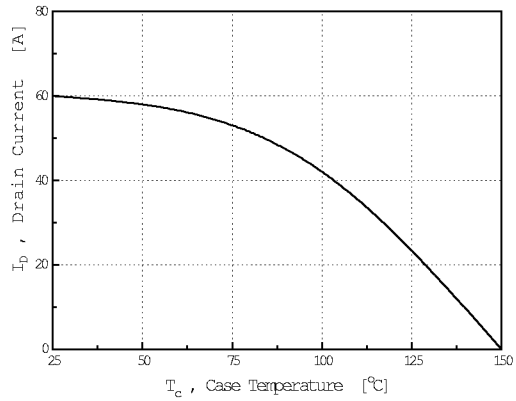


Fig 11. Thermal Response

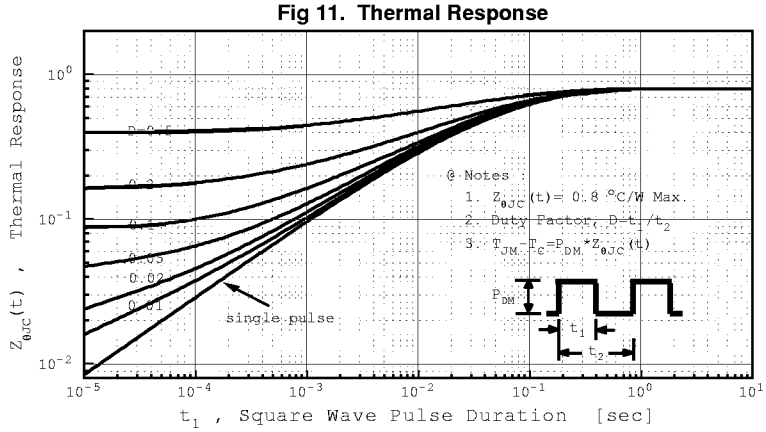


Fig 12. Gate Charge Test Circuit & Waveform

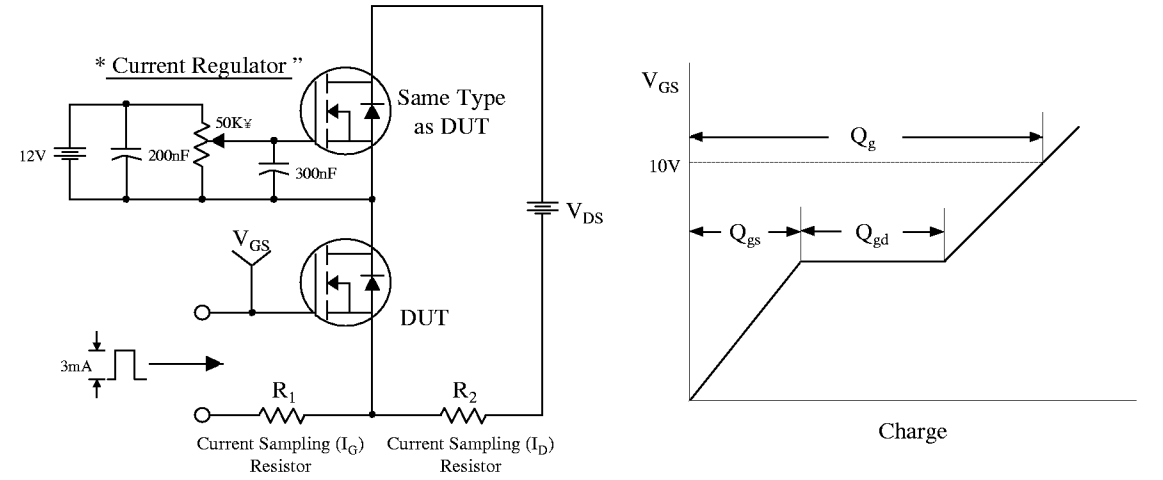


Fig 13. Resistive Switching Test Circuit & Waveforms

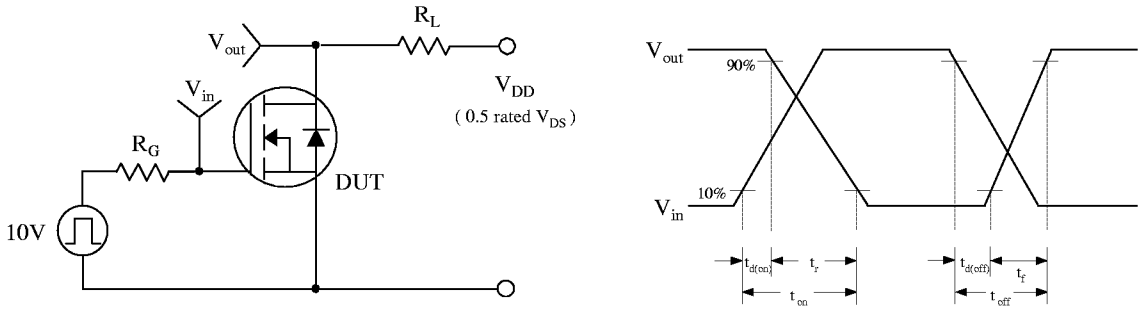


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

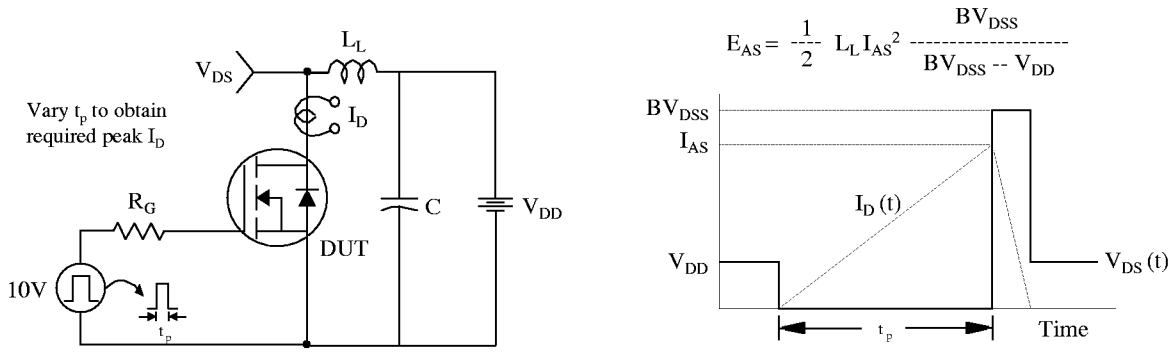


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms